ESD
CIRCUITS AND DEVICES

STEVEN H. VOLDMAN

ESD

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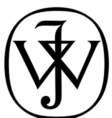

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About the Author

Dr. Steven H. Voldman received his B. S. in Engineering Science from the University of Buffalo (1979); M.S. EE (1981) and Electrical Engineer Degree (1982) from M.I.T.; MS Engineering Physics (1986) and Ph.D. EE (1991) from the University of Vermont under IBM Resident Study Fellow program. At M.I.T., he worked as a member of the M.I.T. Plasma Fusion center, and the High Voltage Research Laboratory (HVRL). At IBM, as a reliability/device engineer, his work included pioneering work in bipolar/CMOS SRAM alpha particle and cosmic ray SER simulation, MOSFET gate-induced drain leakage (GIDL) mechanism, hot electron, epitaxy/well design, CMOS latchup, and ESD. Since 1986, he was responsible for defining the IBM ESD/latchup strategy for CMOS, SOI, BiCMOS and RF CMOS, and SiGe technologies. He has authored ESD and latchup publications in the area of MOSFET scaling, device simulation, copper, low-k, MR heads, CMOS, SOI, SiGe and SiGeC technology. Voldman served as SEMATECH ESD Working Group Chairman (1996–2000), ESD Association Technical Program Chair (2000), Vice Chairman (2001), General Chairman 2002, and ESDA Board of Directors (1998–2006), International Reliability Physics Symposium ESD/Latchup Sub-Committee Chairman (2002–2006), International Physical and Failure Analysis (IPFA) Symposium ESD Sub-Committee Chairman (2003–2005), ESD Association Standard Development Chairman on Transmission Line Pulse Testing (2000–2006), ESD International Committee on Education (ICE) Asian University Liason and "ESD on Campus" program founder, and serves in the ISQED Committee, Taiwan ESD Conference (T-ESDC) Technical Program Committee (Hsinchu, Taiwan), and the International Conference on Electromagnetic Compability (ICEMAC, Taipei, Taiwan). Voldman has provided ESD lectures for universities (e.g., M.I.T. Lecture Series, Taiwan National Chiao-Tung University (NCTU), and Singapore Nanyang Technical University (NTU)). He is a recipient of over 136 U.S. patents, over 100 publications, and recently wrote a textbook on ESD entitled *ESD: Physics and Devices* (John Wiley and Sons, Ltd) as well as contributing to the text "*Silicon Germanium: Modeling, Technology and Simulation,*" and providing talks on patenting and invention. He has been highlighted in *EE Times, Intellectual Property Law and Business* and authored the first article on ESD phenomena for the October 2002 edition of *Scientific American* entitled "*Lightning Rods for Nano-electronics*," and *Pour La Science, Le Scienze, and Swiat Nauk* International editions. In 2003, Dr. Voldman was accepted as the first IEEE Fellow for ESD phenomena in semiconductors for "contributions to electrostatic discharge protection in CMOS, SOI, and SiGe technologies."

Preface

Electrostatic discharge (ESD) phenomena have been known to mankind since the Greek Empire when Thales of Miletus, one of the Seven Sages of Greece, noticed the attraction of strands of hay to amber, leading to the coining of the word "electron." In the 17th century, Gilbert and Cabeo addressed the attractive and repulsive nature of electricity. In the 18th century, a rapid increase of interest occurred for scientists in the understanding of electrical physics—Gray, du Fay, Nollet, Musschenbroeck, Franklin, Watson, Aepinus, Canton, Priestley, Cavendish, Galvani, Coulomb, Volta, Poisson, Faraday—and continued into the 19th century—Laplace, Gauss, Oersted, Ampere, Davy, Ohm, Green, Ostrogradsky, Henry, Lord Kelvin, Joule, Neumann, Weber, Thomson, Kirchoff, Stokes, Helmholtz, and Maxwell. It was the discoveries made in the 1820s by Oersted, Ampere, Davy, and Ohm that began the basic understanding of electrical circuits.

Electrical discharge and the guiding of electrical discharge (e.g., lightning) was of interest to Benjamin Franklin in the 1700s, with the invention of the lightning rod. The lightning rod was mankind's first effort to guide the electrical discharge current of a lightning strike in a direction that would not harm structures. Today, in semiconductor chips, it is the role of the ESD protection networks to guide the current through a semiconductor chip to prevent the failure of circuits and the semiconductor chip. In that sense, ESD protection serves the role of lightning rods for nano-structures; the October 2002 Scientific American article on ESD protection entitled "*Lightning Rods for Nano-electronics*" was truly an appropriate analogy. The role of the semiconductor engineer and ESD design engineer is to fulfill this same objective of guiding the current in a place that does not harm the circuitry—but on a much more smaller scale and in a significantly more complex environment than a lightning bolt and a church steeple.

But today, the focus is on ESD protection in semiconductor chips and electronic chip design.

This is the second book in the ESD Series. The first book in the John Wiley and Sons, Ltd series on ESD protection, entitled *ESD: Physics and Devices*, will serve as a companion book to this text. As stated in the Foreword of *ESD: Physics and Devices*, not only there is a quest for the scientific understanding of ESD, but also there is a struggle in the way that the subject is taught and presented. At this time, there is only one university course in the world that teaches a semester course of this fast rising discipline of ESD phenomenon in semiconductor components – in National Chiao-Tung University in Hsin-chu City, Taiwan. Educational texts worthy of teaching at a university level are needed to teach and educate

engineers for ESD protection of components as well as professionals that are developing ESD devices, circuits, and implementation strategies. To date, ESD is taught in individual lectures, short courses, and tutorials. The teaching of a single lecture on ESD is inadequate to provide educational learning on ESD and ESD engineering; the teaching of a single lecture only trivializes the magnitude of the ESD discipline. Today, there are ESD books, but they are not structured for formal undergraduate or graduate courses suited for physicists, mathematicians, material science majors, or electrical engineering from a generalist perspective which would draw a wide interest across the materials and semiconductor community; the goal of the book *ESD: Physics and Devices* was an attempt to address this.

While the first book *ESD: Physics and Devices* was targeted for the semiconductor device physicist, the circuit designer, the semiconductor process engineer, the material scientist, the chemist, the physicist, the mathematician, the semiconductor manager, and the ESD engineer, a second book is needed to address the details of the ESD job ahead for the professional ESD engineer and the circuit design teams: the design team head designer, the semiconductor chip floor-plan engineer, the power bus design engineer, the I/O design team, the receiver circuit engineer, the off-chip (OCD) driver engineer, the phase lock loop (PLL) engineer, the packaging engineer, the analog team, the radio frequency (RF) design team, the modeling team, the device extraction team, the design rule checking team, the verification team, the kit release team, the ESD kit release team, the graphic technician, the ESD test engineer, quality, reliability, field application engineering, and foundry customers. For the circuit designer and the circuit design team, a text is needed to arm the circuit designer to achieve his objectives effectively. Today, there is only one book *Basic ESD and I/O Design* by S. Dabral and T. Maloney which is an excellent text for the I/O designer. But, to train an ESD engineer, a book is needed which goes much deeper into the ESD circuits and ESD response of I/O circuits.

The cross-discipline nature of the ESD phenomena makes it a difficult subject to teach unless it is taught from a cross-discipline perspective or as a series of disciplines which are woven together carefully to build the understanding from first principles. This same dilemma occurred in the early 1960s in the teaching of integrated semiconductor electronics. The Semiconductor Electronic Education Committee (SEEC) was formed to address how to teach an engineer integrated electronics in a world that separated the teaching of solid state physics, devices, and circuits. It was stated in the Foreword of the SEEC series: "the development of micro-miniaturization of electronic circuits has blurred the dividing line between the 'device' and the 'circuit' and thus has made it increasingly important for us to understand deeply the relationship between internal physics and structure of a device, and its potentialities for circuit performance." It was at this junction that the initiative to establish a series of semiconductor books was taken, which integrated the understanding from the fundamentals of semiconductor physics to circuits in a coherent fashion where each book built on the prior book with a bottom-up approach. In the ESD discipline, this same dilemma holds true.

This motivated me to move forward on the concept of not a single book, but a book series on electrostatic discharge phenomena. The objective of the book series is to establish an educational framework to establish an ESD discipline based on integration of physics, devices and circuits—from the bottom upward—for a wide audience, not just ESD engineers and ESD designers.

From this motivation, the first book *ESD: Physics and Devices* addressed the solid state physics, electro-thermal physics, discharge phenomena, stability theory, ESD electro-thermal

models, and semiconductor device equations. Concepts, such as current constriction, ballasting, and the language of ESD, were introduced. The book segmented the semiconductor devices into the specific regions so as to provide a generalist approach. The book continued with specifics in the area of CMOS, silicon on insulator (SOI), silicon germanium (SiGe), silicon germanium carbon (SiGeC), and future devices such as strained silicon, FINFETs, and carbon nano-tubes.

In this book, *ESD: Devices and Circuits*, a balance is established between a generalist approach and practical implementation to make it applicable to semiconductor chip design. As in the first text, an understanding of the bridge between the microscopic and the macroscopic phenomena is important; one must bridge from the single contact hole to the package; the scale ranges from the device, the circuit, the package, to the system. This traverses both spatial and temporal processes. In the understanding of the time response and the ESD phenomena, the device response, the circuit response, and the semiconductor chip response are important. In the understanding of the spatial response, the distribution effects of the current and voltage are also critical to the understanding of ESD phenomena.

In the semiconductor industry, it is important for circuit designers also to understand the "ESD problem." The days of the ESD engineer as "semiconductor alchemist" are quickly disappearing; brute force methods are too much risk, and for "on-the-job ESD training" there is no time left. In the semiconductor industry, it is still the objective to run the business, get out the designs, and ship products; in this process, there is no time for ESD mistakes or ESD-induced schedule delays or ESD-induced yield loss. Today, there is a higher necessity to educate the circuit design teams in ESD design, since failure is not an option.

In this textbook, *ESD: Devices and Circuits*, a first goal is to teach what is the essential objectives of ESD design. It is common misunderstanding what the goal of the ESD protection network is.

A second goal is to teach how ESD design practices are different from standard circuit design. In other words, how is this design practice different from all other design practices? ESD design practices involve coupling, decoupling, buffering, ballasting, triggering, shunting, and distributing; a goal of this book is to demystify the magic and show the bag of tricks in the tool box that are commonly used. So, a goal is to teach a new method of design—ESD design—which consists of coupling solutions, decoupling solutions, buffering, ballasting, and a large collection of creative techniques.

A third goal is to show that there are many ways to achieve good ESD protection through circuit design practices. A famous Chinese expression is "It does not matter if it is a white cat, or a black cat, as long as it catches mice." With ESD design, there are many ways to achieve the goals, which make the profession full-of-room for creative solutions. A goal of this book is to educate the reader to a point that they can evaluate the pros and cons depending on what his objective is.

A fourth goal is to show that there is not one method but many methods to achieve good ESD results. Good ESD results can be achieved through semiconductor process choices, through the circuit topology choice, or both. It is a common misunderstanding that ESD results are a function of only the semiconductor process. It is also common that the ESD engineer only addresses the ESD networks, and does not look at the circuits. This is a common problem today in the way that the semiconductor foundry–customer relationship is being addressed; the circuit designers are not showing the foundry the circuits, but expect it to solve or assure good ESD protection.

A fifth goal is to show how to design ESD networks. Some of the early chapters focus on design aspects down to the contact, and work up to the full-scale structure. One of the objectives is to focus on the design aspects and how they are different from standard design and design layout. These sections are relevant to both the ESD circuit and the I/O circuit.

A sixth goal is to show how to design better I/O circuits (e.g., not the ESD networks) and expose circuit designers to new circuits that can have ESD concerns. In this book, we are going to focus on how to improve the OCD circuit, receivers, differential receivers, and other circuits. One of the objectives is to teach how to provide more robust ESD networks *without* performance impacts. My first lesson in circuit design showed that to achieve an objective for reliability does not always mean a performance degradation; if you are creative, you can improve the performance or find a way not to impact the performance. My personal goal as an ESD engineer was to find circuit solutions that did not impact the performance, but improved the ESD protection. In this goal, some circuit inventions will be shown to demonstrate this concept.

A seventh goal is to show examples from bulk CMOS technology, silicon on insulator (SOI) technology, silicon germanium (SiGe) technology, silicon germanium carbon (SiGeC) technology, and gallium arsenide (GaAs) technology. Although a CMOS engineer may never work in the other technologies such as SOI, it is valuable to see how the technologies influence the ESD results, circuit designs, and solutions. Hence, it was a goal and objective to include circuit chapters in the other technologies to reinforce the ESD design practices and principles.

An eighth goal is to expose the reader to the patent art in the ESD field. A significant amount of activity in the ESD field can be found by reading the patent art. As a result, a number of patents are referenced which are either first in the field, relevant in the discussions of interest, or teach methods and methodologies.

The second book in this series, *ESD: Circuits and Devices*, will contain the following:

Chapter 1 introduces the reader to think about the role of resistance, capacitance, and inductance in the ESD design of semiconductor chips. Given resistance, capacitance, and inductance, which is the most important? Under what circumstances? Under what time constants? Device, circuit, and chip-level effects exist during ESD events. What are the ESD metrics on a device level? How would they differ on a circuit level? . . . and, what is the important ESD metrics on the ESD chip level? The question of how the voltage and current distribute within the device, the circuit, and the semiconductor chip or system is addressed. What are the current loops? What is the path of current flow in an ESD event, and what are the most important parameters? How does one analyze the current flow through the current loop? . . . and how does the current flow through the system? An "ESD Ohm's Law" will be highlighted as a quick simple solution for quick circuit design "sizings" for evaluation of success or failure. The spatial distribution within the device, circuit, or chip is discussed. Lumped versus distributed circuits will be reviewed. Additionally, ESD metrics and ESD business strategy will be discussed.

Chapter 2 will be an elementary high-level perspective of how to "floor plan" a semiconductor chip, taking into regard the essential elements to achieve good ESD protection. Additionally, the chapter will discuss electrical and spatial connectivity. It is common working with ESD engineers and circuit designers that they are not thinking about whether the issue is a spatial issue or an electrical issue. From a top-down perspective, good ESD protection begins with a design team when it is built-in to the high-level floor plan prior to the semiconductor chip definition. This will serve as a brief introduction to ESD devices,

guard rings, pads, ESD input circuits, ESD power clamps, peripheral I/O versus array I/O footprint issues, and all the items to construct a good ESD strategy for ESD protection. Hence, there is a relationship between the electrical connectivity, the spatial connectivity, and the floor planning and integration of a single chip or system-on-chip (SOC) integration.

Chapter 3 begins the discussion of the design and layout of semiconductor devices. The chapter will focus on the ESD design of metal oxide semiconductor field effect transistors (MOSFET). In ESD design of MOSFET structures, all the physical dimensions and spacings have a role in the ESD operation; channel length, channel width, and contact spacing (contact-to-contact, contact-to-gate, contact to diffusion edge, and the ‘‘last’’ edge contact). Wiring a MOSFET for the optimum ESD protection is an art form in itself. The effect of broadside wiring, ‘‘parallel,’’ and ‘‘anti-parallel’’ wiring design addresses MOSFET wiring optimization as well as reinforcing the issue of the current and voltage distribution within a semiconductor device, as discussed in Chapter 1. The discussion continues to address the design layout and ESD issues for the ‘‘multi-finger MOSFET.’’ The multi-finger MOSFET issue addresses how the current and voltage distributes within a given MOSFET layout between a plurality of MOSFET fingers. Additionally, the chapter will address the issue of a plurality of MOSFETs in series or the series ‘‘cascode’’ MOSFET. The chapter will close on the issue of the ESD scaling issues of MOSFETs.

Chapter 4 focuses on the ESD design and layout of diode elements. The chapter will address diode elements typically found in CMOS and BiCMOS technology. These consist of LOCOS and STI-defined elements, as discussed in the first textbook *ESD: Physics and Devices*: p^+/n-well diodes, n^+/p^- substrate diodes, n-well/p^- substrate diodes, polysilicon-bound diodes, and trench-bound diode elements. The physical dimensions and spacings of the diode elements and how they influence ESD operation will be the key focus of the chapter. In the p^+/n-well diode element, the issues of width effect, perimeter-to-area ratio, diode end effects, lateral ballasting, contacts, and wiring configurations are addressed. As in the MOSFET, the voltage and current distribution within the physical structure influences the ESD efficiency and how much area is utilized for ESD protection; this influences the ESD metric for the device. As in Chapter 3, the multi-finger p^+/n-well diode issue is addressed. Likewise, the physics, layout, and design of a plurality of p^+/n-well diodes in series are discussed. These will be referred to as ‘‘diode strings.’’ In this discussion, the issues of area ratio of successive stages, diode sharing, and different design architectures will be discussed. Triple-well ‘‘diode string’’ implementations will also be discussed.

Chapter 5 will discuss the ESD design and layout of SOI ESD elements. First, we will discuss the SOI polysilicon-bound gated-diode structure, also known as the lateral unipolar bipolar transistor (Lubistor). Second, we will discuss the dynamic threshold MOS (DTMOS) body- and gate-coupled diode ESD element. The SOI buried resistor (BR) element will also be discussed, as well as the unique issues associated with these elements for SOI technology.

In Chapter 6, the focus switches to semiconductor OCD circuit design and ESD issues. Various types of CMOS OCD circuit types will be discussed from asymmetric and symmetric CMOS, TTL, Gunning transceiver logic (GTL), open-drain, HSTL, and SSTL OCDs. Additionally, MVI drivers will be discussed. These include series stacked MOSFET pull-ups and pull-down CMOS OCDs, as well as self-biased n-well OCDs. Universal OCD circuits and the ESD implications will also be discussed. Additionally, programmable impedance OCDs networks will be discussed, as well as the ESD implications that they establish.

Chapter 7 will discuss semiconductor receiver circuits and ESD issues, Starting with a receiver and a single inverter followed by successively more complicated networks. ESD issues with full-pass transmission gates (TG), half-pass TG, and finally TG and feedback ‘‘keeper’’ networks. Solutions to address the receiver issues, with the introduction of the CMOS receiver with modified keeper networks, will also be introduced. Zero-threshold voltage half-pass TG receivers, pseudo-zero threshold voltage receivers, and the unique ESD issues will also be highlighted. CMOS receiver networks with feedback elements, such as Schmitt trigger networks and ESD issues, will be discussed. The issue of HBM and CDM solutions and integration with the receiver network will be also discussed. For effective receiver design, one must integrate the HBM and CDM solutions that are naturally integrated as not to impact receiver performance.

Chapter 8 focuses on SOI circuits. In this chapter, SOI ESD devices for receiver and OCD networks are discussed. SOI ESD double-diode designs, SOI ESD diode-strings, and SOI ESD MOSFET design will be shown. SOI ESD failure mechanisms will be discussed, and solutions to alleviate SOI ESD design failures will be reviewed. A new SOI double-diode gate-isolated ESD network design and method will be discussed. Additionally, SOI failure mechanisms in receiver network in half-pass TG, SOI BR resistors, and other elements will be discussed. Additionally, special networks, such as fuse circuitry and other issues, will be highlighted.

Chapter 9 addresses ESD power clamp circuits. ESD power clamps are used between the power supply rails to lower the chip impedance during ESD events. This chapter addresses CMOS, bipolar, and BiCMOS ESD power clamps, which are triggered by voltage conditions or frequency discrimination. The chapter will first discuss CMOS ESD power clamps that are commonly used in the semiconductor industry; these include grounded-gate NMOS clamps, gate-coupled MOSFETs, RC-triggered MOSFETs, substrate-triggered MOSFET ESD power clamps, and gate- and substrate-coupled MOSFET power clamps. Additionally, RC-triggered MOSFETs for mixed-voltage applications will be discussed. ESD power clamps for bipolar technology, suitable for silicon, silicon germanium, silicon germanium carbon, gallium arsenide, and indium phosphide technologies, will be discussed. The bipolar classes of power clamps discussed include both forward-bias and reverse-bias breakdown trigger networks as well as capacitively triggered networks; these include diode string trigger networks, Zener-breakdown triggered power clamps, and BV_{CEO}-breakdown-triggered power clamps. Triple-well ESD power clamps will also be discussed.

In this text book, I weave between theoretical, analytical, experimental, and practical considerations. The topics change from ESD layout, to circuit theory, to ESD phenomena, to floor plans, to space, and to time, changing scope, and scale. At times, I provide great analytical details, and then in some sections, teach by example of practical implementations. This is done intentionally. One must realize this is the nature of the ESD engineer, and the nature of the semiconductor industry.

Enjoy the text, and enjoy the subject matter of ESD. There is still so much more to learn.

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SRAMs, bulk CMOS and SOI microprocessors, ASIC development, and today in the field of mixed signal RF CMOS and RF BiCMOS Silicon Germanium semiconductor chips. The ESD circuit learning was driven by the creative interaction of one semiconductor device engineer and a very large global circuit design community whose products became the opportunity to demonstrate ESD success or ESD failure. I would like to thank the circuit designers, I/O teams, ESD test laboratory, and failure analysis engineers where together we learned the interaction and issues of ESD in semiconductor chips—Roy Flaker (bipolar and CMOS SRAM), Jack Gersbach (bipolar SRAM), Russel Houghton (SRAM), Jeffery Chu (SRAM), Richard Parent (4Mb-DRAM), Howard Kalter (16-Mb DRAM), H. S. Lee (CMOS SRAM), David Pricer, Thomas Maffit (16-Mb DRAM), Jeffery Dreibelbis (16-Mb DRAM), Charles Drake (16-Mb DRAM), David Hui (CMOS Server Division I/O), Daniel Dreps (CMOS ASIC, and CPU), Robert Williams (CMOS AS-400 CPU), Daniel Young (CMOS AS-400 CPU), John Bialas (PowerPC 601+), Roger Gregor (CMOS ASICs), Harold Pilo (CMOS SRAM), Geordie Braceras (CMOS SRAM), John Connors (CMOS SRAM), Tony Correale (PowerPC Embedded Controllers), Douglas Stout (ASIC I/O), Ron Piro (ASIC I/O), Jeffery Sloan (ASIC), James Pequignot (ASIC), Francis Chan (ASIC), Sam Ray (Disk Drive), Stephen Ames (Optical Interconnect), Lloyd Walls (Austin CPU), Anthony Bonnaccio (Bipolar Specials), and others. Outside of IBM, I am indebted to circuit designers and the microprocessors teams whom I had an opportunity to work with: Motorola/IBM PowerPC 602, 603, 604, 620, 640 teams (lead: Gianfranco Gerosa), AMD K6 team (lead: Don Draper and Stephen Beebe), the Digital Alpha team (lead: Larry Baer), the Compaq Alpha team (lead: Warren Anderson), NEXGEN x386 and x486 teams (lead: Don Draper), the TRANSMETA Scorpion, and Tarantula microprocessor teams (lead: Mark Johnson), IDT microprocessors, Sun microprocessors (lead: Avi Leibenmensch), and the Cyrix x86 teams in development of floor planning, circuits, and ESD devices. In the ESD laboratory, I would like to thank Vaughn Gross, Christine Blakemore, Rebecca Ryan, Josee Coutinho, Matt Hausmann, Ernie Goodrich, and Richard Serafin for HBM, MM, and TLP testing support. For years of ESD test site and design support, I would like to thank Joann Howard of IBM. I would like to thank the IBM failure analysis team for years of diagnosing ESD failures to assist in the ESD learning process on SEM, TEM, EMMI, AFM, and PICA tools: James Never, Peter Czahor, Ted Regula, Jim Pecozzi, David Vallet, Ted Levin, Phil Kaszuba, Dick Ross, and all the others. In the semiconductor development, I would also like to thank peers and co-workers in the Bipolar, CMOS, and Silicon Germanium teams: Michael Hargrove, James Slinkman, Stephen Furkay, Jeffery B. Johnson, Stephen Geissler, Toshi Furukawa, Jim Nakos, Jim Adkisson, Terry Hook, and Chris Long. I would like to thank my managers Richard Ross, John Hiltebeitel, Jim McNichol, Mark Hakey, Jim Dunn, and Stephen St. Onge in the support of my ESD and latchup work. I was fortunate for the last 23 years to have the advice and counsel of many IBM engineers and scientists. I was very fortunate to interact and have as semiconductor mentors and guidance from my first years at IBM: Ron Troutman, Wendell Noble, Badih El-Kareh, Ed Nowak, Eric Adler, George Sai-Halasz, Tak Ning, Denny Tang, Robert Dennard, Matt Wordeman, Jack Y.-C. Sun, John Aitken, Paul Bakeman, Andre LeBlanc, Andre Forcier, Bruno Aimi, Charles Stapper, and Peter Cottrell. For publication support, I would like to thank Dorie Gentes of IBM Technical Communications for 20 years of publication editing and support. Additionally, I would like to thank the IBM Burlington patent legal team for years of support and teaching about ESD patents.

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B''H
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1 Electrostatic Discharge

1.1 ELECTRICITY AND ELECTROSTATICS DISCHARGE

1.1.1 Electricity and Electrostatics

In the field of electricity, electrostatics, and circuit theory, there are many discoveries and accomplishments that have lead to the foundation of the field of electrostatic discharge (ESD) phenomenon. Below is a chronological list of key events that moved the field of electrostatics forward:

- 600 B.C. Thales of Miletus discovers electrostatic attraction.
- 1600 A.D. William Gilbert proposes the ''electric fluid'' model.
- 1620 A.D. Niccolo Cabeo discusses ''attractive'' and ''repulsive'' phenomena.
- 1729 A.D. Stephen Gray demonstrates ''electricity'' can be transferred by wires.
- 1733 A.D. Charles Francois du Fay discusses two kinds of electricity—''resinous'' and ''vitreous.''
- 1749 A.D. Abbey Jean-Antoine Nollet invents the two-fluid model of electricity.
- 1745 A.D. Pieter Van Musschenbroeck invents the Leyden jar, or the capacitor.
- 1747 A.D. Benjamin Franklin proposes single fluid model, with ''positive'' and ''negative'' charge.
- 1748 A.D. Sir William Watson develops the first ''glow discharge.''
- 1759 A.D. Francis Ulrich Theodore Aepinus discusses ''charging by induction.''
- 1766 A.D. Joseph Priestley deduces the electric force follows an inverse square law.
- 1775 A.D. Henry Cavendish invents the concept of capacitance and resistance.

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- 1785 A.D. Charles Augustin Coulomb verifies the inverse square law relationship.
- 1812 A.D. Simeon Denis Poisson demonstrates that charge resides on the surface of a conductor.
- 1821 A.D. Humphrey Davy establishes the geometrical and thermal effects of resistance.
- 1826 A.D. Ohm develops the relationship between potential, resistance, and current.
- 1837 A.D. Michael Faraday discovers the concept of dielectric constants in materials.
- 1841 A.D. James Prescott Joule shows relationship of electrical current and thermal heating.
- 1848 A.D. Gustav Kirchoff extends the concept of Ohm's law.
- 1873 A.D. James Clerk Maxwell publishes the work *Treatise of Electricity and Magnetism.*
- 1889 A.D. Paschen establishes a relationship explaining the electrical breakdown of gases.
- 1906 A.D. Toepler establishes a relationship for arc resistance in a discharge process.
- 1915 A.D. Townsend explains avalanche phenomena in materials.

1.1.2 Electrostatic Discharge

In the field of ESD, accomplishments to advance the field of electrostatic discharge phenomena are in the form of development of experimental discovery, analytical models, introduction of new semiconductor devices and circuits, test equipment, as well as the development of ESD standards. Below is a short chronological list of key events that moved the field of ESD:

- 1968 A.D. D. Wunsch and R. R. Bell introduces the power-to-failure electro-thermal model in the thermal diffusion time constant regime [1].
- 1970 A.D. D. Tasca develops the power-to-failure electro-thermal model in the adiabatic and steady-state time constant regime [2].
- 1971 A.D. Vlasov and Sinkevitch develops a physical model for electro-thermal failure of semiconductor devices [3].
- 1972 A.D. W. D. Brown evaluates semiconductor devices under high-amplitude current conditions [4].
- 1981 A.D. J. Smith and W. R. Littau develops an electro-thermal model for resistors in the thermal diffusion time regime [5].
- 1981 A.D. Enlow, Alexander, Pierce, and Mason addresses the statistical variation of the power-to-failure of bipolar transistors due to semiconductor manufacturing process, and ESD event variations [6–8].
- 1983 A.D. M. Ash evaluates the non-linear nature of the power threshold and the temperature dependence of the physical parameters establishing the Ash relationship [9].

- 1983 A.D. V. I. Arkihpov, E. R. Astvatsaturyan, V. I. Godovosyn, and A. I. Rudenko derives the cylindrical nature of the electro-current constriction [10].
- 1985 A.D. T. J. Maloney and N. Khurana discusses transmission line pulse (TLP) testing as a method for semiconductor *I–V* characterization and modeling [11].
- 1989 A.D. Dwyer, Franklin, and Campbell extends the Wunsch-Bell model to address three-dimensional effects [12].
- 1989 A.D. R. Renninger, M. Jon, D. Lin, T. Diep, and T. Welser introduces the first field-induced charged device model (CDM) device simulator [13].
- 1989 A.D. T. Polgreen and P. Chatterjee explain non-uniform current flow in silicided multi-finger MOSFETs [14].
- 1992 A.D. M. Hargrove and S. Voldman quantify CMOS ESD networks in the first CMOS shallow trench isolation (STI) technology [15].
- 1992 A.D. S. Voldman discovers the effect of MeV implanted retrograde well dose on ESD robustness [16].
- 1993 A.D. D. Lin publishes the first paper on the effect of MOSFET dielectric and junction breakdown scaling on on-chip ESD protection [17].
- 1993 A.D. S. Voldman publishes the first paper on the influence on MOSFET constant electric field scaling theory on ESD robustness [16]. A "Constant ESD scaling" theory is developed under the constraint of maintaining ESD robustness as technology is scaled [16].
- 1993 A.D. ESD Association releases the human body model (HBM) standard for semiconductor component testing [18].
- 1993 A.D. H. Geiser introduces the very fast transmission line pulse (VF-TLP) ESD test system [19].
- 1994 A.D. A. Ameresekera and C. Duvvury publishes on the influence of MOSFET scaling trends on ESD robustness [20].
- 1994 A.D. ESD Association releases the machine model (MM) standard for semiconductor component testing [21].
- 1995 A.D. A. Wallash releases the first publication on ESD failure mechanisms in magneto-resistor (MR) recording heads [22]. The significance of the work was the first indication of ESD concerns in the magnetic recording and disk drive industry.
- 1995 A.D. SEMATECH initiates ESD Working Group to address ESD strategic planning. The SEMATECH effort addresses ESD technology benchmarking, ESD technology roadmap and test equipment, ESDA and JEDEC ESD specification alignment, and TLP test standard development.
- 1996 A.D. K. Banerjee develops Ti/Al/Ti interconnect model, extending the work of D. Tasca to modern CMOS interconnects [23].
- 1997 A.D. S. Voldman publishes first experimental measurements of ESD in copper (Cu) interconnects, and the comparison to aluminum (Al) interconnects. This work addresses

the influence of CMOS interconnect scaling on ESD robustness, and the evolutionary changes from aluminum to copper interconnects [24].

- 1997 A.D. ESD Association Device Testing Standards Committee releases first charged device model (CDM) Standard [25].
- 1997 A.D. J. Barth introduces the first commercial transmission line pulse (TLP) device simulator. The introduction of commercial systems has lead to the acceptance of the TLP methodology for ESD sensitivity testing of semiconductors.
- 1998 A.D. SEMATECH Quality and Reliability ESD Working Group initiates transmission line pulse (TLP) standards effort.
- 2000 A.D. S. Voldman and P. Juliano published the first ESD measurements in Silicon Germanium (SiGe) technology [26]. The significance of this work is the beginning of the focus of ESD in radio frequency (RF) technology.
- 2002 A.D. R. Gibson and J. Kinnear initiate the S20.20 ESD Control Certification Program. The significance of this effort is the focus on international certification of ESD control programs.
- 2003 A.D. Oryx Instruments and Thermo KeyTek, introduces commercial very fast transmission line pulse (VF-TLP) systems. The significance of this work is the introduction of VF-TLP systems as a standard testing methodology for future ESD testing.
- 2004 A.D. ESD Association Device Testing Standards Committee initiates the transmission line pulse (TLP) Standard Practice document [27]. The significance of this work is the acceptance of TLP as a standard testing methodology in the semiconductor industry.

1.1.3 Key ESD Patents, Inventions, and Innovations

In the field of ESD protection, there are many patents, inventions, and innovations that stimulated growth of ESD circuits as well as improved the ESD robustness of circuits themselves. ESD circuit inventions are important in providing innovations and techniques that improve the ESD robustness of semiconductor chips. Interest in ESD patenting of ESD protection networks began in the 1970s, with a continued growth in patent activity, invention, and innovations. Below is a chronological list of key innovations that moved the field of ESD protection forward in the area of ESD circuits. In some cases, no patent for the invention was pursued. Many of the patents chosen in this listing consist of the ESD design practices and subjects and topics which will be discussed in the text. Starting from the 1970s, here is a listing of key circuit innovations and those which will be referred to in the future chapters:

- 1970 A.D. M. Fischer (IBM). Resistor-thick oxide FET gate protection device for thin oxide FETs. *IBM Technology Disclosure Bulletin* **13** (5): 1272–1273. This introduced the use of a gate-coupled ‘‘thick oxide’’ field effect transistor and a series resistor element. This invention discloses the concept of using a thick oxide insulated gate field effect transistor (IGFET) to protect a thin oxide IGFET [28].

- 1971 A.D. Boss *et al.* (IBM). ESD network with capacitor divider and half-pass transmission gate. *IBM Technology Disclosure Bulletin.* This introduced the concept of using a capacitive divider across a half-pass transmission gate to reduce the gate oxide stress [29].

- 1971 A.D. M. Lenzlinger (RCA). ESD distributed diode/resistor double-diode network. *RCA Corporation, CD 4013*. Publication: "Gate Protection of MIS Devices", M. Lenzlinger, *IEEE Transactions on Electron Device* **ED-18** (4): 1971. This publication discloses the concept of a double-diode ESD network as well as a distributed diode-resistor transmission line for the diode to V_{DD} [30].

- 1973 A.D. G. W. Steudel (RCA). Input transient protection for complimentary field effect transistor integrated circuit device. *U.S. Patent No. 3,712,995*, January 23, 1973. The patent shows a distributed double-diode ESD network with diode/resistor distributed network, but with the reverse polarity [31].

- 1974 A.D. T. Enomoto and H. Morita (Mitsubishi). Semiconductor device. *U.S. Patent No. 3,819,952*, June 25, 1974. The patent shows the use of a first-stage gate-coupled thick oxide insulated gate field effect transistor (IGFET), a series resistor element (prior to the IGFET drain), and a IGFET source resistor element. This first stage is followed by a second-stage thin oxide IGFET whose gate is coupled to the first-stage IGFET source node. The network introduces the concept of a first- and second-stage ESD network, gate-coupling, series resistor options, as well introduces a de-biasing resistor at the source of the first stage [32].

- 1979 A.D. C. Bertin (IBM). Over-voltage protective device and circuits for insulated gate transistors. *U.S. Patent No. 4,139,935*, February 20, 1979. This patent by Claude Bertin was the first process patent that produced a metallurgical junction with a lower breakdown voltage using junction "tailoring" where the breakdown element was to serve as a "gate tie down" or protection network for MOSFET gate oxides [33].

- 1983 A.D. N. Sasaki (Fujitsu). Semiconductor integrated circuit device providing a protection circuit. *U.S. Patent No. 4,423,431*. December 27, 1983. Sasaki introduces the idea of use of a series resistor, and thin oxide transistor as a protection network. The network also introduces gate-coupled thin oxide and a resistor in series with the capacitor. This is the first network that is using gate-coupled thin oxide devices with a resistor on the gate electrode to ground, in a single-stage implementation [34].

- 1983 A.D. L. Avery (RCA). Integrated circuit protection device. *U.S. Patent No. 4,400,711*. August 23, 1983. This patent used a MOSFET in the regenerative feedback loop of a *pnpn* silicon-controlled rectifier (SCR) for ESD protection applications [35].

- 1989 A.D. C. Duvvury and R. Rountree (Texas Instruments). Output buffer with improved ESD protection. *U.S. Patent No. 4,855,620*, August 8, 1989. This patent is the first patent to discuss the optimization of output buffers for ESD protection improvements [36].

- 1990 A.D. R. Rountree (Texas Instruments). Circuit structure with enhanced electrostatic discharge protection. *U.S. Patent No. 4,939,616*, July 3, 1990. This patent discusses the formation of a low-voltage trigger *pnpn* silicon-controlled rectifier (SCR) using an $n+$ diffusion that extends outside of the *n*-well region to form a lower breakdown voltage and

lateral *npn* element. This innovation was important to produce low-voltage trigger SCRs as technology began to scale [37].

- 1992 A.D. A. Graham (Gazelle). Structure for providing electrostatic discharge protection. *U.S. Patent No. 5,124,877*, June 23, 1992. This patent introduces the concept of a diode string as well as a "ESD discharge reference rail." Today, ESD diode strings are commonly used, as well as the discharge rail concept [38].
- 1993 A.D. W. Miller (National Semiconductor). Electrostatic discharge detection and clamp control circuit. *U.S. Patent No. 5,255,146*, October 19, 1993. This patent was the first patent RC-triggered ESD power clamp network to address the presence of "detection circuits" which respond to the ESD pulse. This is the first patent that addresses the usage of an RC network which is chosen to be responsive to the ESD pulse network [39].
- 1993 A.D. R. Merrill (National Semiconductor). Electrostatic discharge protection for integrated circuits. *U.S. Patent No. 5,239,440*, August 24, 1993. This innovation utilized the RC-discriminator network, inverter logic, and logic circuitry that is parallel to the pre-drive circuitry, and turns on the I/O off-chip driver (OCD) output stage during ESD events [40].
- 1993 A.D. Kirsch, G. Gerosa, and S. Voldman (Motorola and IBM). Snubber-clamped ESD diode string network. This network introduced a diode string as a mixed-voltage interface network and solved the reverse-Darlington amplification using a "Snubber" diode element. Implemented into the PowerPC microprocessor and embedded controller family. This was applied to advanced microprocessors for mixed-voltage applications [41].
- 1994 A.D. D. Puar (Cirrus Logic). Shunt circuit for electrostatic discharge protection. *U.S. Patent No. 5,287,241*, February 15, 1994. This introduced the first RC-triggered *p*-channel MOSFET-based ESD power clamp network [42].
- 1994 A.D. J. Pianka (AT&T). ESD protection of output buffers. *U.S. Patent No. 5,345,357*, September 6, 1994. Development of RC-trigger and gate coupling circuit elements for activation of the output of an *n*-channel MOSFET pull-up and pull-down off-chip driver (OCD). This ESD technique is especially valuable for small computer system interface (SCSI) chips, since only *n*-channel output transistors are used as the pull-up and pull-down elements [43].
- 1996 A.D. T. J. Maloney (Intel). Electrostatic discharge protection circuits using biased and terminated PNP transistor chains. *U.S. Patent No. 5,530,612*, June 25, 1996. Maloney's patent application was a second ESD circuit application to address the leakage amplification in diode string ESD networks. This was applied to advanced microprocessors for mixed-voltage applications [44].
- 1997 A.D. S. Voldman, S. Geissler, and E. Nowak (IBM). Semiconductor diode with silicide films and trench isolation. *U.S. Patent No. 5,629,544*, May 13, 1997. This is the first patent that addresses four items: first, it addresses ESD diode structures constructed in shallow trench isolation; second, it addresses STI pull-down effects; it addresses the lateral polysilicon-bound gated ESD *p–n* diodes; and fourth, the silicon-on-insulator (SOI) lateral ESD gated diode structures [45].

- 1997 A.D. D. Krakauer, K. Mistry, S. Butler, and H. Partovi, (Digital Corp). Self-referencing modulation circuit for CMOS integrated circuit electrostatic discharge protection clamps. *U.S. Patent No. 5,617,283*, April 1, 1997. This was the first ESD application using MOSFETs to establish a MOSFET gate-modulation network. This was applied to microprocessor applications [46].

- 1997 A.D. S. Voldman (IBM). Power sequence-independent electrostatic discharge protection circuits. *U.S. Patent No. 5,610,791*, March 11, 1997. This patent is the first patent to address sequencing issues in a multiple-rail power supply chip. The ESD protection circuitry is power sequence-independent thereby eliminating any restrictions on the sequencing of power as applied to, and removed from, the different power supply rails of the IC chip [47].

- 1997 A.D. S. Voldman (IBM). Voltage regulator bypass circuit. *U.S. Patent No. 5,625,280*, April 29, 1997. This patent was the first to address ESD implementations for ESD protection of voltage regulators which are integrated between peripheral I/O and core power rails. This was important for DRAM, SRAM, and ASIC applications with core regulation, mixed-voltage power, and low-voltage core voltages [48].

- 1998 A.D. F. Assaderaghi, L. Hsu, J. Mandelman, G. Shahidi, and S. Voldman (IBM). Silicon-on-insulator body-coupled gated diode for electrostatic discharge (ESD) and analog applications. *U.S. Patent No. 5,811,857*, September 22, 1998. This invention discusses the first body- and gate-coupled silicon on insulator (SOI) ESD network applying dynamic threshold MOS (DTMOS) concepts to ESD networks [49].

- 1999 A.D. J. Chen, L. Li, T. Vrotsos, and C. Duvvury. PNP-driven NMOS ESD protection circuits. *U.S. Patent No. 5,982,217*, November 9, 1999. This circuit innovation uses a *pnp* element to improve the ESD robustness of a MOSFET ESD device. The emitter of a *pnp* transistor and the drain of protection NMOS device are connected to an I/O pad. The collector of the *pnp* transistor and the gate of the protection NMOS transistor are connected to ground through a resistor [50].

- 1999 A.D. S. Voldman (IBM). Modified keeper half-latch receiver circuit. *U.S. Patent No. 5,894,230*, April 13, 1999. This patent addressed ESD issues with CMOS receiver circuits which utilized *p*-channel MOSFET feedback networks, which demonstrated ESD problems in V_{DD} reference test modes. This was very important in achieving ESD robustness in receiver networks for applications below 0.5-μm CMOS technologies [51]. This network was implemented into CMOS microprocessors, CMOS logic, memory, and ASIC applications.

- 1999 A.D. S. Voldman (IBM). Electrostatic discharge protection circuits for mixed-voltage interface and multi-rail disconnected power grid applications. *U.S. Patent No. 5,945,713*, August 31, 1999**.** This patent addresses two concepts: the first concept is for an ESD diode network for a multiple power supplies and separated ground rails, as well as a second circuit is a self-bias well sequence-independent input node ESD circuit. The first network was integrated into CMOS DRAM designs, and the second ESD network was implemented into both CMOS microprocessors, servers, and ASIC I/O libraries. The self-bias well sequence-independent circuit was implemented into sequence-independent I/O libraries, which required the ability to lower the power supply voltage when the input pins are positive [52].

- 2000 A.D. M. D. Ker (ITRI, Taiwan). Substrate-triggering electrostatic discharge protection circuit for deep-submicron integrated circuits. *U.S. Patent No. 6,072,219*, June 6, 2000. The patent is the first patent to address substrate triggered ESD protection networks [53].
- 2000 A.D. S. Voldman and D. Hui (IBM). Switchable active clamp network. *U.S. Patent No. 6,075,399*, June 13, 2000. This application demonstrates the first "active clamp" network that is suitable for ESD protection in triple well and silicon-on-insulator (SOI) technology that utilizes body-coupling techniques [54].
- 2001 A.D. R. Mashak, R. Williams, D. Hui, and S. Voldman (IBM). Active clamp network for multiple voltages. *U.S. Patent No. 6,229,372*, May 8, 2001. This invention is the first active clamp network used to provide active clamping and ESD protection that utilizes MOSFET body-coupling techniques in a multiple-voltage power supply environments [55].
- 2002 A.D. S. Voldman and S. Ames (IBM). Modified current mirror circuit for BiCMOS applications. *U.S. Patent No. 6,404,275*, June 11, 2002. The invention is the first to address the problem of current mirror circuits on input pads, and develops new current mirror circuits to improve the ESD robustness [56].
- 2003 A.D. M. D. Ker, K. K. Hung, and T. H. Tang (UMC). Silicon-on-insulator diodes and ESD protection circuits. *U.S. Patent No. 6,649, 944*, November 18, 2003. This is the first patent of an SOI ESD lateral gated diode $p+/p-/n-/n+$ network which uses both well implants, and removes the gate structure for improved ESD protection levels [57].
- 2003 A.D. S. Voldman, A. Botula, and D. Hui. Electrostatic discharge power clamp circuit. *U.S. Patent No. 6,549,061*, April 15, 2003. This is the first silicon germanium (SiGe) ESD power clamp network for mixed-voltage and mixed-signal applications using high frequency, and high-breakdown SiGe HBT devices [58]. The significance of the invention is the utilization of the natural scaling of the breakdown voltages of a SiGe HBT device.
- 2003 A.D. S. Voldman. SOI voltage-tolerant body-coupled pass transistors. *U.S. Patent No. 6,628,159*, September 30, 2003. This patent is the first patent to address the ESD failure mechanisms of a SOI half-pass transmission gate (e.g., pass transistor) using body-coupling techniques [59].
- 2003 A.D. K. Verhaege, M. Mergens, C. Russ, J. Armer, and P. Jozwiak. Multi-finger current ballasting ESD protection circuit and interleaved ballasting for ESD sensitive circuits. *U.S. Patent No. 6,583,972*, June 24, 2003. This patent addresses the concept of using gate-coupling from one MOSFET finger to another in a "domino" fashion.

1.1.4 Table of ESD Defect Mechanisms

Semiconductor device and circuit failure occurs from both electro-thermal or electrical breakdown mechanisms. The ESD failure mechanisms will be a function of the technology type, semiconductor device type, the ESD event type, the polarity of the ESD event, and the

Table 1.1 ESD failure mechanisms in CMOS semiconductor devices

Bulk CMOS Device	Test type	Polarity	Reference	Failure mechanism
p^+/n-Well Diode	HBM	Positive	V_{DD}	p^+ diffusion to n^+n-well contact under STI region
p^+/n-Well Diode	HBM	Positive	V_{SS}	p^+ anode salicide under contacts
N^+/P^- substrate	HBM	Negative	V_{SS}	Salicide failure under n^+ contacts
n-well/P^- substrate	HBM	Negative	V_{SS}	n^+ contacts
			V_{DD}	n-well to n-well under STI region
n-Channel MOSFET	HBM	Positive	V_{SS}	MOSFET source to drain failure
				MOSFET Drain-to-Gate Failure
	CDM		V_{SS}	MOSFET Gate Dielectric Pin-hole
			V_{SS}	MOSFET Gate to Drain Failures
p-Channel MOSFET	HBM	Negative	V_{SS}	MOSFET Source-to-Drain
	CDM		V_{DD}	MOSFET Well to Drain Failure
n^+ Resistor	HBM	Positive	V_{SS}	N^+ Contact/Salicide film failure
n-Well resistor	HBM	Positive	V_{SS}	N^+/N-well contacts and salicide film
Buried resistor (BR)	HBM	Positive	V_{SS}	Resistor Input Contact Salicide
				BR Input to BR Gate Dielectric Failure
		Negative	V_{SS}	BR Input Contact Salicide

grounded reference source. In Table 1.1, examples of ESD failure mechanisms are shown for bulk CMOS semiconductor device elements whether used in ESD networks or circuits.

In a silicon-on-insulator (SOI) technology, ESD failure mechanisms can be significantly different than those observed in bulk CMOS. The substrate region is physically separated from the semiconductor devices using a buried oxide (BOX) region. The existence of the BOX region changes the failure modes and mechanisms significantly. Table 1.2 shows SOI ESD failure mechanisms.

In Table 1.3, ESD failure mechanisms in bipolar technology are shown. In bipolar technology, and in bipolar complimentary MOS (BiCMOS), the bipolar emitter base region is the most sensitive structural feature of the bipolar transistor. Low-level ESD failures typically occur in the emitter–base junction due to thermal second breakdown. Additionally, bipolar collector-to-emitter, base-to-collector, and collector-to-substrate failures can occur but at higher voltage conditions.

Table 1.2 ESD failure mechanisms in silicon-on-insulator (SOI) technology

Silicon-on-insulator Device	Test type	Polarity	Reference	Failure mechanism
Lateral SOI p^+/n^+ gated diode	HBM	Positive	V_{DD}	(1) p^+ Diffusion to n^+ n-well contact under polysilicon gate (2) Polysilicon gate to drain failure
	HBM	Negative	V_{SS}	p^+ Diffusion to n^+ n-well contact under polysilicon gate
	CDM		V_{SS}	Polysilicon gate to drain failure
SOI buried resistor element	HBM	Negative	V_{SS}	BR input to BR gate failure
SOI wafers	CDM	Positive	V_{SS}	(1) Buried oxide (2) Metal bus

Table 1.3 ESD failure mechanisms of silicon, silicon germanium, and silicon germanium carbon bipolar elements

Bipolar Device	Test type	Polarity	Reference	Failure mechanism
NPN	HBM	Positive	V_{SS}	(1) Emitter–base junction (2) Collector-to-emitter failure
		Negative	V_{SS}	(1) Emitter–base junction (2) Collector-to-substrate failure

Passive elements used in CMOS, RF CMOS, BiCMOS, and RF BiCMOS include base–collector junction varactors, hyper–abrupt junction varactors, metal-insulator-metal (MIM) capacitors, and inductors. Passive elements can undergo ESD failure depending on the location within the circuit or chip. Passive elements can serve as ESD elements or circuit network elements. Table 1.4 shows a listing of ESD failure mechanisms.

Table 1.4 ESD failure mechanisms in Passive elements

Passives Device	Test type	Polarity	Reference	Failure mechanism
Base–collector varactor	HBM	Positive		Base–collector junction
Hyper–abrupt varactor	HBM	Positive		Base–collector junction
MIM capacitor	HBM	Positive		Gate dielectric
Inductors	HBM	Positive		(1) Inductor coil underpass (2) Inductor coil (3) Inductor-to-substrate dielectric failure

Table 1.5 ESD failures in gallium arsenide elements

GaAs Device	Test type	Polarity	Reference	Failure mechanism
MESFET	HBM	Positive		(1) Gate-to-drain
				(2) Gate-to-source
				(3) Metallurgy
		Negative		(4) Gate-to-drain
				(5) Gate-to-source
				(6) Metallurgy
HBT	HBM	Positive		(7) Emitter–base
		Negative		(8) Emitter–base

Table 1.5 shows a listing of ESD failure mechanisms in gallium arsenide products. In the table, GaAs MESFET failures are shown. GaAs failure mechanisms occur in the GaAs device, from the physical GaAs films, and the interconnect materials (e.g., AuNiGe films). GaAs heterojunction bipolar transistors (HBT) are sensitive in the emitter–base region similar to the silicon bipolar transistor. Additionally, passive elements are also vulnerable to ESD events. Below is a list of some GaAs failure mechanisms.

ESD failures occur in structures that are needed for semiconductor chip design. Table 1.6 is a summary of the failure mechanisms. ESD failure mechanisms can occur from ‘‘no connect pads,’’ floating pads, sense pads, metal bussing, programmable power pads, decoupling capacitors, and other integration elements. Table 1.6 provides a list of different type of failure mechanisms that occur in a semiconductor chip.

Table 1.7 shows a listing of common circuit elements in CMOS design and BiCMOS design. The listing includes off-chip drivers (OCD), receivers, phase-lock loop, active clamp networks, decoupling capacitors, and other common circuit components. These will be discussed in the text.

Table 1.6 ESD failure mechanism in semiconductor chip architecture

Structures Device	Test type	Polarity	Reference	Failure mechanism
No connect pads	HBM	Positive/negative		(1) ILD cracking
				(2) Metal extrusion
Floating pads	HBM	Positive/negative		(1) ILD cracking
				(2) Metal extrusion
VDD sense pads	HBM	Positive		(1) Metal interconnect failure
				(2) ILD cracking
				(3) Metal extrusion
Programmable VDD pads	HBM	Positive/negative		(1) *n*-Channel MOSFET
Metal bus	HBM	Positive		(1) Metal melting
				(2) ILD cracking
				(3) Melted ILD
Decoupling capacitor	HBM	Positive		Gate dielectric

Table 1.7 ESD failure mechanisms in common circuit networks

Circuits Circuit type	Test type	Polarity	Reference	Failure mechanism
CMOS OCD	HBM	Positive	V_{SS}	*n*-Channel MOSFET pull-down
Programmable impedance OCD	HBM	Positive	V_{SS}	*n*-Channel pull-down MOSFET (smallest fingers)
CMOS GTL OCD	HBM	Positive/Negative	V_{SS}, V_{DD}	*n*-Channel MOSFET
CMOS HSTL OCD	HBM	Positive	V_{SS}	*n*-Channel MOSFET
CMOS receiver	HBM	Positive	V_{SS}	*n*-Channel MOSFET gate dielectric
	CDM		V_{SS}	*n*-Channel MOSFET gate dielectric
CMOS receiver with half-pass TG	HBM		V_{SS}	*n*-Channel MOSFET gate dielectric
CMOS receiver with half-pass TG and PFET keeper	HBM	Positive	V_{DD}	*n*-Channel half-pass and PFET keeper failure
CMOS receivers zero-VT half-pass TG	HBM	Positive	V_{SS}	(1) Zero VT half-pass MOSFET source-to-drain failure
SOI CMOS receiver with half-pass TG	CDM	Positive	N/A	(1) SOI half-pass TG gate-to-diffusion (on pad side)
Bipolar differential receiver	HBM	Positive	Pin-to-pin	Emitter-base of npn on ground reference
Voltage regulators	HBM	Positive	V_{SS}	Regulator MOSFET source-to-drain failure
CMOS PLL	HBM	Positive	V_{SS}	(1) Decoupling capacitor (2) PLL diode elements
CMOS Schmitt trigger				*n*-Channel MOSFET feedback element
CMOS current mirror	HBM	Positive	V_{SS}	*n*-Channel MOSFET source-to-drain of current mirror
Bipolar current mirror	HBM	Positive	V_{SS}	Base–emitter junction of current mirror
CMOS active clamp network	HBM	All	All	*n*-Channel MOSFET source-to-drain failure
CMOS fuse networks	HBM	Positive	V_{SS}	*n*-Channel MOSFET source to drain
D-K flip-flops	HBM			MOSFET gate structure
Decoupling capacitor circuit	HBM	Positive		Gate dielectric

1.2 FUNDAMENTAL CONCEPTS OF ESD DESIGN

1.2.1 Concepts of ESD Design

Fundamental concepts and objectives exist in the ESD design of semiconductor devices, circuits, and systems. The key questions to ask about ESD design are the following:

- What is it that makes ESD design unique?
- How is it distinct from standard circuit design practices?

Another way of stating this is—How is ESD design practices different from all other design practices?

A first unique design objective is to prevent any physical element in the system from latent or permanent damage that impacts the functionality, reliability, or quality from ESD events. A corollary to this is to prevent latent or permanent damage below a desired current or voltage magnitude. This is the first objective of ESD design. What else makes ‘‘ESD design’’ unique? Here are some of the distinctions and differences:

- *Device Response to External Events*: Design of devices and circuits to respond to (and not to respond to) unique current waveforms (e.g., current magnitude and time constants) associated with external environments.
- *Alternate Current Loops*: Establishment of alternative current loops or current paths which activate during high-current or high-voltage events.
- *Switches*: Establishment of ‘‘switches’’ that initiate during high current or voltage events.
- *Decoupling of Current Paths*: Decoupling of sensitive current paths.
- *Decoupling of Feedback Loops*: Decouple of loops that initiate pinning during off condition or ESD test modes.
- *Decoupling of Power Rails*: Decoupling of electrical connections to grounded references and power supplies.
- *Local and Global Distribution*: Local and global distribution of electrical and thermal phenomena in devices, circuits, and systems.
- *Usage of Parasitic Elements*: Utilization and avoidance of parasitic element in the design practice.
- *Buffering*: Utilization of current and voltage buffering of sensitive devices, circuits, or sub-circuits.
- *Ballasting*: Introduction of resistance to redistribute current within a single element or a plurality of elements.
- *Unused Sections of a Semiconductor Device, Circuit or Chip Function*: Utilize ‘‘unused’’ segments of a semiconductor device for ESD protection, which was not utilized for functional applications.

- *Impedance Matching between Floating and Non-Floating Networks*: Matching of conditions during testing to allow matching between networks.
- *Unconnected Structures*: Addressing structures not containing electrical connections to the power grid or circuitry.
- *Utilization of "Dummy Structures and Dummy Circuits"*: Use of "dummy structures" as a means to provide linewidth matching.
- *Non-scalable Source*: The ESD event does not scale, while the devices are scaled each technology generation.
- *Area Efficiency*: Focus on area efficiency to utilize all of the physical device area for ESD protection.

1.2.2 Device Response to External Events

On the first issue of preventing any physical element in the system from latent or permanent damage that impacts the functionality, reliability, or quality from ESD events, there is significant misunderstanding. It is a belief of many engineers that the objective of the ESD networks is to carry all of the ESD current, as well as be the first element to undergo failure. It is also a belief that it does not matter if the ESD structure undergoes failure. These statements are not accurate understanding of the objective of ESD design. The role of the ESD network is to increase the ESD robustness of the complete product or application. The "failure criteria" is based on the functional, reliability, or quality objective of the electrical component.

In ESD design, the ESD devices as well as the circuits which are to be protected can be designed to respond to (and not to respond to) unique ESD current waveforms. In standard circuit design, digital circuits are designed to switch from logic state levels, rising or falling edges. Circuits can store information or mix different logical states. ESD networks typically are designed to respond to specific ESD pulses. These networks are unique in that they address the current magnitude, frequency, polarity, and location of the ESD events. Hence, in ESD design, the ESD networks are designed and tuned to respond to the various ESD events. In ESD design, different stages or segments of the network can also be designed to respond to different events. For example, some stages of a network can respond to human body model (HBM) and machine model (MM) events, while other segments respond to the charged device model (CDM) event. These ESD events differ in current magnitude, polarity, time constant, as well as the location of the current source. Hence, the ESD circuit is optimized to respond and address different aspects of ESD events that circuits may be subjected to. Additionally, circuits can be modified to be less sensitive to ESD events using ESD circuit techniques. As a result, the understanding of the material, device, circuit, and system physical time constants is critical in ESD design.

1.2.3 Alternate Current Loops

A unique issue is the establishment of alternative current loops or current paths which activate during high current or voltage events. By establishing alternative current loops, or secondary paths, the ESD current can be redirected to prevent over-voltage of sensitive

circuits. In peripheral circuit design, this concept is used for overshoot and undershoot phenomenon. In peripheral circuit design, both passive and active ‘‘clamping’’ is used to eliminate over-voltage of circuit networks; this practice is most akin to the ESD methodology. As a result, in order to have an effective ESD design strategy, this current loop must respond to the ESD event and have a low impedance. A distinction from peripheral circuit methodology of clamping is the current magnitude; ESD events have significantly higher currents than the overshoot and undershoot phenomenon experienced in peripheral circuit design. Hence, the ‘‘ESD current loop’’ must achieve a similar objective, but must have lower impedance.

1.2.4 Switches

On the issue of establishment of ‘‘switches’’ that initiate during high current or voltage events, the uniqueness factor is that these are at time either passive or activated by the ESD event itself. A unique feature of ESD design is that it must be active during unpowered states. Whereas in peripheral circuit design, passive and active clamps are typically utilized in powered states. Hence, the ‘‘switches’’ used to sway the current into the ESD current loop are initiated passively, or are initiated by the ESD event itself. Hence, the ESD event serves as the current and voltage source to initiate the circuit. These switches lead to ‘‘current robbing’’ and the transfer of the majority of the current from the sensitive circuit to the alternative current loop. Although today there is some interest in ESD design in powered states, the majority of testing, and design practices assume an unpowered design. As a result, the ESD design must use ‘‘switches’’ or ‘‘triggers’’ that initiate passively (e.g., a diode element), or actively (e.g., a frequency-triggered ESD network). A design objective is to provide the lowest voltage trigger allowable in the application space. Hence, a key ESD design objective is to utilize low-voltage trigger elements that serve as a means to transfer the current away from the sensitive circuit to alternative current paths. A large part of effective ESD design is the construction of these switches or trigger elements.

1.2.5 Decoupling of Current Paths

An additional design method is the decoupling of elements in the ESD current path. Circuit elements can be introduced which lead to the avoidance of current flow to those physical elements. The addition of ‘‘ESD decoupling switches’’ can be used to decouple sensitive circuits as well to avoid the current flow to these networks or sections of a semiconductor chip. ESD decoupling elements can be used to allow elements to undergo open or floating states during ESD events. This can be achieved within the ESD network, or within the architecture of a semiconductor chip.

Decoupling of sensitive elements or decoupling of current loops can be initiated by the addition of elements that allow the current loop to ‘‘open’’ during ESD events. During ESD testing, power rails and ground rails are set as references. The decoupling of nodes, elements, or current loops relative to the grounded reference prevents over-voltage states in devices, and eliminates current paths. These decoupling elements can avoid ‘‘pinning’’ of electrical nodes. Hence, integration of devices, circuits elements, or circuit function that introduce decoupling electrical connections to ground references and power supplies references, is a key unique ESD design practice.

1.2.6 Decoupling of Feedback Loops

Feedback loops can lead to unique ESD failures and lower ESD results significantly. The decoupling of nodes, elements, or current loops relative to the grounded reference prevents over-voltage states in devices, and eliminates current paths initiated by the feedback elements. These decoupling elements can avoid "pinning" of electrical nodes. Hence, integration of devices, circuits elements, or circuit function that introduce decoupling electrical connections to ground references, and power supplies references of the feedback elements during ESD testing is also a key unique ESD design practice.

1.2.7 Decoupling of Power Rails

Electrical coupling of sensitive nodes to the power supply rails can lead to ESD failure. The electrical coupling of nodes to the power supply rails, ground rails or chip substrate can lead to ESD failure. Semiconductor elements whose nodes are connected to the power supply can establish current paths, constrain electrical potential, establish "pinning" of nodes and circuits, or undergo electrical overstress. A key ESD design practice is establishing methods to electrically decouple from power rails to avoid electrical overstress of electrical nodes and components, as well as eliminate undesirable current paths.

1.2.8 Local and Global Distribution

To provide an effective ESD design strategy, the ESD design practices must focus on the local and global distribution of electrical and thermal phenomena in devices, circuits, and systems. Locally, good current distribution lowers the current density in physical elements. As the current distribution improves, the local self-heating can be reduced; this increases the margin to thermal breakdown. As the current distributes, the effectiveness of the device helps improving the utilization of the total area of the ESD network or circuit element. On a circuit and system level, the distribution of the ESD current within the network or system, lowers the effective impedance, and lowers the voltage condition within the ESD current loop. The ESD events are transient events; the physical time constants of the devices, circuits, and system are critical in the understanding, modeling, and simulation of the effectiveness of the elements in the system. A key design practice of ESD devices and circuits is the desire to distribute the current to provide improved design utilization to achieve higher ESD robustness.

1.2.9 Usage of Parasitic Elements

ESD networks are concerned with parasitic devices inherent in the standard devices, or exist between adjacent structures or devices. ESD design either utilizes or avoids activation of these parasitic elements in the ESD implementations. Utilization of parasitic elements is a common ESD design practice for ESD operation. For example, MOSFET structures in wells form parasitic lateral or vertical bipolar transistors with their corresponding wells or substrate regions. Diodes in the substrate can also form lateral bipolar devices with adjacent well regions or devices. Diodes within isolation regions, such as a well, dual-well, or triple-

well isolation, can utilize the parasitic elements for the ESD protection scheme. These can include both vertical and lateral parasitic elements inherently within the standard devices and within the technology. It is not common to use these parasitic elements in standard circuit design, whereas for ESD design it is very prevalent to utilize the parasitic devices and is part of the ESD design practice and art.

1.2.10 Buffering

In ESD design, it is also a common practice to establish current and voltage buffering of sensitive devices, circuits, sub-circuits, chip level core regions, or voltage islands. This can also be done to provide isolation between radio frequency (RF), analog, and digital segments of a semiconductor chip. A design practice is to increase the impedance in the path of the sensitive circuit either by placement of high-impedance elements, establishing ‘‘off’’ states of elements, voltage and current dividing networks, resistor ballasting, or initiating elements in high-impedance states.

1.2.11 Ballasting

Resistive, capacitive, or inductive ballasting can be introduced to redistribute current or voltage within a single element or a plurality of elements, circuit, or chip segment. The usage within a semiconductor device element allows for redistribution within a device to avoid electro-thermal current constriction, and poor area utilization of a protection network or circuit element. The usage of ballasting allows to redistribute the source current from the ESD event to avoid thermal heating or electrical overstress within the semiconductor network or chip. Ballasting can be introduced into semiconductor device structures using the following ESD design methods:

- Semiconductor process implant design choices (e.g., sheet resistance, profile, dose, and energy).
- Semiconductor material choice (e.g., titanium vs. cobalt).
- Use of multiple material phase states (e.g., C49 and C54 titanium phase states).
- Silicide removal in the direction of current flow.
- Silicide removal lateral to the direction of current flow.
- Introduction of resistor elements (e.g., *n*-diffusion, *p*-diffusion, *n*-well, polysilicon film, tungsten local interconnect, and wire resistors).
- Introduction of elements with positive or negative temperature coefficient of resistance (TCR).
- Segmentation by introduction of isolation regions.
- Segmentation by introduction of lateral high-resistance regions in the semiconductor device.
- Segmentation by introduction of high-resistance regions in the well or substrate regions.

1.2.12 Unused Sections of a Semiconductor Device, Circuit, or Chip Function

In ESD design, it is common to utilize ‘‘unused’’ segments of a semiconductor device for ESD protection, which was not utilized for functional applications. For example, in a ‘‘gate array’’ design practice, elements are not connected for functional usage. An ESD design practice is to use them for ESD protection purposes.

1.2.13 Impedance Matching Between Floating and Non-Floating Networks

In ESD design, it is common to utilize the ‘‘unused’’ segments of a semiconductor device for ESD protection and impedance match the network segments for ESD operation; this matching of conditions during ESD testing allows for current sharing during matching between networks and common triggering voltage conditions.

1.2.14 Unconnected Structures

In semiconductor chips, there are many structures which are electrically not connected to other circuitry or power grids which are vulnerable to ESD damage. In functional designs, these are not a concern. But in ESD design practice, these unconnected structures are locations of potential charging and dielectric breakdown. Hence in ESD design, unique solutions are required.

1.2.15 Utilization of Dummy Structures and Dummy Circuits

In the ESD design practice it is not uncommon to utilize dummy structures or dummy circuits which serve the purpose to provide better current uniformity or distribution effects; this concepts span from usage of dummy MOSFET polysilicon gate fingers to dummy inverter circuits.

1.2.16 Non-Scalable Source Events

Another key issue is that the ESD event is a non-scalable event. Each generation, the size of devices are scaled to smaller dimensions. The ESD design practice must address the constant source input current and the physical scaling of the structures. A unique ESD scaling theory and strategy must be initiated to address this issue.

1.2.17 Area Efficiency

As in power electronic applications, the area of efficiency of a device, or network for redistribution of the ESD current is a key ESD design metric. Area efficiency of a device, network, or chip is important issue in ESD design.

1.3 TIME CONSTANTS

Time is an important variable in the understanding of ESD phenomena and ESD design. Time influences the physical phenomenon that is involved, the response of the material, and the response of the semiconductor device, circuit, or chip to the time-dependent ESD phenomena. Time affects the range of the distribution and propagation of the signal, and its distribution through the physical system. Given a physical system, a characteristic length and a characteristic time can be established to explain a physical system. Hence, it is important to understand the time scales, and time constants to comprehend the interaction. As a result, a time constant approach is chosen as a way to introduce the subject of ESD phenomena.

1.3.1 Characteristic Times

1.3.2 Electrostatic and Magnetostatic Time Constants

Given a physical system, a characteristic length and a characteristic time can be established to explain a physical system. Let us define a scale of characteristic length l and characteristic dynamical time τ. Electrical phenomenon involves both electrical and magnetic fields. The electric and magnetic fields are coupled through Maxwell's equations. Three important time constants allow us to understand the validity of the electrical phenomenon. The three physical time constants of interest are the charge relaxation time, τ_e, the magnetic diffusion time, τ_m, and the electromagnetic wave transit time, τ_{em} [61].

1.3.2.1 Charge relaxation time

Let us define the charge relaxation time, τ_e

$$\tau_e = \frac{\varepsilon}{\sigma}$$

The charge relaxation time is the physical *RC* time of the medium. It determines how fast a medium responds to an electrical transient state. For example, it determines how well a material screens an electric field from within a medium. This is more apparent when the physical dimensions are added to the time constant.

$$\tau_e = \frac{\varepsilon}{\sigma} = \varepsilon\rho = \left(\frac{\varepsilon A}{l}\right)\left(\frac{\rho l}{A}\right) = RC$$

1.3.2.2 Magnetic diffusion time

The magnetic diffusion time, τ_m, is

$$\tau_m = \mu\sigma\ell^2$$

The magnetic diffusion time is the *L/R* time of the medium. This is a time constant associated with how a medium responds to a magnetic transient state. This is more apparent when put in the following form,

$$\tau_{\mathrm{m}} = \mu\sigma\ell^2 = \frac{\mu}{\rho}l^2 = \frac{\left(\frac{\mu l^3}{A}\right)}{\left(\frac{\rho l}{A}\right)} = \frac{L}{R}$$

1.3.2.3 Electromagnetic wave transit time

The electromagnetic wave transit time, τ_{em}, is the time it takes for an electromagnetic plane wave to propagate a distance l

$$\tau_{\mathrm{em}} = \frac{l}{c}$$

where c is the speed of light in a medium. The speed of light in a medium can be expressed as

$$c = \frac{1}{\sqrt{\mu\varepsilon}}$$

From this we can express the electromagnetic transit time as

$$\tau_{\mathrm{em}} = \ell\sqrt{\mu\varepsilon} = \sqrt{(\mu\sigma\ell^2)\left(\frac{\varepsilon}{\sigma}\right)}$$

The electromagnetic transit time, τ_{em} , can then be expressed as [61],

$$\tau_{\mathrm{em}} = \sqrt{\tau_{\mathrm{e}}\tau_{\mathrm{m}}}$$

In this form, the electromagnetic transit time is the arithmetic mean of the magnetic diffusion time and the charge relaxation time. Note that putting in the macroscopic dimensions, we can express this as

$$\tau_{\mathrm{em}} = \sqrt{\tau_{\mathrm{e}}\tau_{\mathrm{m}}} = \sqrt{(RC)\left(\frac{L}{R}\right)} = \sqrt{LC}$$

In this form, the electromagnetic wave transit time is the square root of the inductance and the capacitance.

Let us define an additional parameter β_τ

$$\beta_\tau = \frac{\tau_{\mathrm{em}}}{\tau}$$

where the parameter is the ratio of the electromagnetic transit time to the characteristic time. For Maxwell's equations to reduce to the electro-quasistatic (EQS) assumption, the magnetic diffusion time must be less than the charge relaxation time and the characteristic

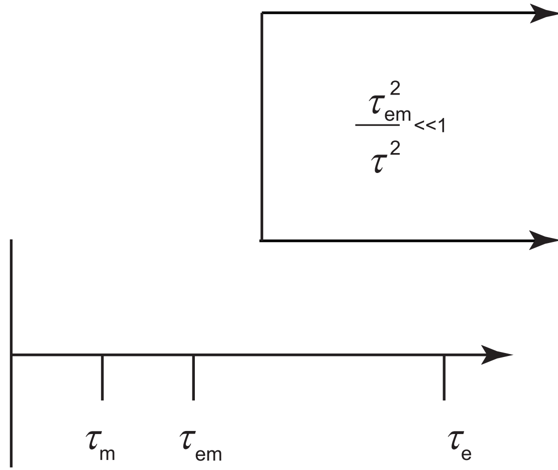

Figure 1.1 Electro-quasistatic time constant hierarchy

time τ must be much greater than the electromagnetic transit time. Figure 1.1 shows the electro-quasistatic time constant hierarchy.

In the majority of ESD concerns which is of interest in the scope of the text, electrostatics and electro-quasistatics are valid. The characteristic time scale of an ESD pulse will be of the order of a nanosecond to tens of nanoseconds, which is significantly longer than the electromagnetic transit time of a semiconductor device, circuit, or chip. For semiconductor, the substrate materials are such that the charge relaxation time is longer than the magnetic diffusion time as a result of the magnetic permittivity values and electrical permittivity. As the analysis addresses electrical interconnects, packaging, and transmission line pulse systems, the characteristic time approaches the electromagnetic transit time. In the analysis of ESD events involving the arc discharge, both current phenomena and electromagnetic emissions are present of a TE, TM, and TEM form.

For Maxwell's equations to reduce to the magneto-quasistatic (MQS) assumption, the charge relaxation time must be less than the magnetic diffusion time and the characteristic time τ must be much greater than the electromagnetic transit time. In most ESD problems, the analysis does not involve the MQS analysis. But, there are some cases, such as magnetic recording media, magnetic memory, and MRAMs, where the MQS assumption is valid.

1.3.3 Thermal Time Constants

ESD phenomena is both electrical and thermal in nature. The time regimes of thermal analysis is divided into three regimes, based on the thermal diffusion time. These regimes are known as the adiabatic time regime, the thermal diffusion time regime, and the steady-state regime. These regimes directly follow from the assumption of the relative time scales compared to the thermal diffusion; this directly follows from the solution of the partial differential equation known as the thermal diffusion equation.

1.3.3.1 Heat capacity

Heat capacity of a medium is the ability of a medium to store energy. The heat capacity of the system is expressed as the product of the mass density, ρ, the specific heat, c_p, and temperature T

$$C_p \Delta T = \rho c_p \Delta T$$

1.3.3.2 Thermal diffusion

Thermal transport occurs as a result of a gradient in the temperature field. Thermal conduction occurs as a result of thermal diffusion.

1.3.3.3 Heat transport equation

ESD phenomena involves both electrical and thermal phenomena. The temperature field in a medium can be determined from the differential equation of heat conduction. The temperature at any point in the medium can be quantified by understanding the energy balance in a given region. The energy-balance equation for an infinitesimal volume is determined by the sum of the net rate of heat entering the volume, and the rate of energy generation in the volume, which is equal to the rate of increase of the internal energy in the volume. The net rate of heat entering the infinitesimal volume is equal to the heat flowing into the volume and the heat flowing out of the volume. The sum of the differential heat flow in all directions determines the net rate of heating in the volume. This term is the divergence of the heat flux. The rate of energy generation in the volume is associated with the generation sources in the infinitesimal. The rate of increase in the internal energy is associated with the increase in the heat capacity of the system. The energy balance equation in this form is also known as the heat equation, or the partial differential equation of heat conduction [62],

$$\frac{\partial}{\partial x}\left(k\frac{\partial T}{\partial x}\right) + \frac{\partial}{\partial y}\left(k\frac{\partial T}{\partial y}\right) + \frac{\partial}{\partial z}\left(k\frac{\partial T}{\partial z}\right) + g = \rho c_p \frac{\partial T}{\partial t}$$

In the case that the thermal conductivity, k, is position and temperature independent, the thermal conductivity variable can be separated from the heat flux term. In this case, the partial differential equation of heat conduction can be normalized. The heat flux term can be simplified as the Laplacian of temperature and expressed as

$$\nabla^2 T + \left(\frac{g}{k}\right) = \frac{1}{\alpha}\frac{\partial T}{\partial t}$$

In this form, the thermal diffusivity is defined as

$$\alpha = \frac{k}{\rho c_p}$$

This equation in this form is important for quantifying the ESD event in the location where the heat generation is occurring. This is typically in the region of electrical current

fluence or electrical current generation. For example, heat is generated in the source, drain, and channel of a MOSFET as a result of Joule heating.

Given that there is no internal generation of heat sources inside the medium, the partial differential equation of heat conduction can be simplified to the Fourier equation, also known as the diffusion equation.

$$\nabla^2 T = \frac{1}{\alpha}\frac{\partial T}{\partial t}$$

The Fourier equation is also known as the parabolic equation since it is a differential equation which is first order in time and second order in space. For ESD analysis, this equation is applied in regions where there are no sources of thermal generation, yet whose temperature field is being influenced by heat flux or temperature gradients inside the regions or on its boundaries.

For steady-state processes, the partial differential equation of heat conduction simplifies to

$$\nabla^2 T + \left(\frac{g}{k}\right) = 0$$

For the case of a uniform thermal conductivity (space and time), the partial differential equation of heat conduction reduces to the Poisson equation with temperature as the field variable. The Poisson equation is valuable for analysis of self-heating processes which are steady state. In the case that there is no internal generation, uniform thermal conductivity, and no heat generation, the Poisson equation simplifies to the Laplace equation

$$\nabla^2 T = 0$$

1.3.4 Thermal Physics Time Constants

From the partial differential equation of heat conduction, a characteristic time associated with thermal diffusion is the thermal diffusion time, τ_T,

$$\tau_T = \frac{\ell^2}{\alpha}$$

where α is the thermal diffusivity, $\alpha = k/\rho c_p$ and l is the characteristic length [61]. Given an oscillatory steady-state thermal excitation which has an angular frequency, ω, where the spatial wavelength is much shorter than other physical characteristic lengths, a thermal skin depth can be defined as [61]

$$\delta = \sqrt{\frac{2\alpha}{\omega}}$$

1.3.4.1 Adiabatic, thermal diffusion time scale and steady state

ESD phenomenon in semiconductors concerns itself with events where the time scale of the applied pulse and response of the medium, circuit, and systems are of primary interest.

The hierarchy of characteristic times must be established to understand the physical phenomenon and the relationship of the ESD event characteristic times. The characteristic time of the ESD event relative to the electromagnetic wave transit time, the charge relaxation

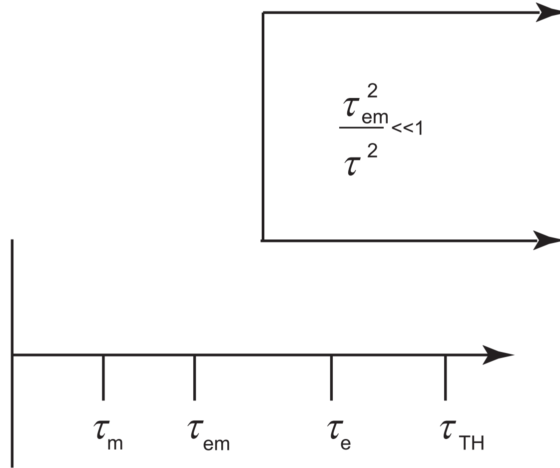

Figure 1.2 Electro-quasistatic and thermal time constant hierarchy

time, the magnetic diffusion time, and the thermal diffusion time are important to understand the physical response.

In semiconductors such as silicon, the hierarchy of characteristic times follow the EQS assumption. Figure 1.2 shows the electro-quasistatic and thermal time constant hierarchy.

For an EQS assumption, the magnetic diffusion time is shorter than the electromagnetic transit time. The ordering of characteristic times are the magnetic diffusion time, the electromagnetic transit time, and then the charge relaxation time. Additionally, the time region of interest is such that the electromagnetic transit time is significantly smaller than the characteristic time of the pulse (e.g., $\beta \ll 1$). The ordering of these characteristic times must be true to insure validity of the EQS assumption. To address the issue of thermal transport, there are three regions of interest within this hierarchy of characteristic times. When the characteristic pulse time, τ, is much shorter than the thermal diffusion time, the thermal transport due to conduction is negligent. This is the ''adiabatic assumption.'' As the characteristic pulse time, τ, is of the same order of magnitude as the thermal diffusion time, the hierarchy of the time scales is such that $\tau \sim O$ [1]. This will be referred to as the ''thermal diffusion regime assumption.'' As the characteristic pulse time is significantly longer than the thermal diffusion time, the solution approaches a steady-state response known as the ''steady-state assumption.''

1.3.5 Semiconductor Device Time Constants

1.3.5.1 Depletion region transit time

For the diode depletion region transit time, the time it takes to traverse the depletion width is a width of the depletion region divided by the drift velocity of the carrier,

$$\tau_t = \frac{W_d}{v_d}$$

where the depletion width can be expressed as a function of the doping concentration on both sides of the metallurgical junction [63],

$$W_{\mathrm{d}} = \left[\frac{2\varepsilon kT}{q2}\ln\left\{\frac{N_{\mathrm{A}}N_{\mathrm{D}}}{n_i^2}\right\}\left(\frac{1}{N_{\mathrm{A}}}+\frac{1}{N_{\mathrm{D}}}\right)\right]^{\frac{1}{2}}$$

and the drift velocity can be expressed as the product of the mobility times the peak electric field,

$$v_{\mathrm{d}} = \mu|E|$$

The peak electric field in the junction can be expressed as a function of the voltage across the depletion region, and the doping concentrations,

$$\left|E_{\mathrm{peak}}\right| = \frac{q}{\varepsilon}N_{\mathrm{A}}\left[\frac{2\varepsilon(V_0+Vr)}{q}\left\{\frac{N_{\mathrm{D}}}{N_{\mathrm{A}}(N_{\mathrm{D}}+N_{\mathrm{A}})}\right\}\right]^{\frac{1}{2}}$$

This time constant is important in that it is a key time constant when a diode element is used as an ESD element, or a switching element. This is of greater concern in addressing high-speed ESD phenomena such as the charged device model (CDM) events.

1.3.5.2 Silicon diode storage delay time

In the switching of a silicon diode, stored charge in the base region can limit the diode speed. The diode storage delay time can be expressed as [63],

$$\tau_{\mathrm{sd}} = \tau_{\mathrm{p}}\left[\mathrm{erf}^{-1}\left(\frac{I_f}{I_f+I_r}\right)\right]$$

which is the product of the recombination time of a p^+n diode, and the inverse error function of the ratio of the forward and reverse currents. Note that this time constant is a function of the current in a semiconductor device, and can be limiting during fast ESD events.

1.3.5.3 Bipolar base transit time

The bipolar base transit time is the time for a carrier to diffuse across the base region. This is equal to the base width divided by the diffusion velocity; this can be expressed as a function of the base width and the diffusion coefficient,

$$\tau_t = \frac{W_{\mathrm{B}}^2}{2D}$$

where W_{B} is the base width, and D is the diffusion coefficient. This time constant is important for the understanding of the time response of a bipolar transistor.

1.3.5.4 Bipolar turn-on transient time

For the turn-on transient of a bipolar transistor, the time constant is a function of the recombination time, the base current, and collector current [63]

$$\tau_{S} = \tau_{p} \ln\left[\frac{1}{1 - \frac{I_{C}}{\beta I_{B}}}\right]$$

1.3.5.5 Bipolar turn-off transient time

For the turn-off transient time of a bipolar transistor, the time constant is a function of the recombination time, the base current, and collector current [63]

$$\tau_{S} = \tau_{p} \ln\left[\frac{\beta I_{B}}{I_{C}}\right]$$

1.3.5.6 Bipolar emitter transition capacitance charging time

In a bipolar transistor, there is a finite "*RC*" time for the response of the emitter. The response of the emitter is a function of the emitter resistance, r_{E}, and the associated emitter capacitance at zero bias voltage [63]

$$\tau_{E} \approx r_{E} C_{TE} \cong \frac{4V}{I_{E}} C_{TE}(0)$$

with emitter resistance equal to the thermal voltage divided by the emitter current

$$r_{E} = \frac{kT}{qI_{E}}$$

and the capacitance is the dielectric constant divided by the depletion width (at zero volts)

$$C_{TE}(0) = \frac{\varepsilon}{W_{d}}$$

$$W_{d} = \left[\frac{2\varepsilon kT}{q2} \ln\left\{\frac{N_{A} N_{D}}{n_{i}^{2}}\right\}\left(\frac{1}{N_{A}} + \frac{1}{N_{D}}\right)\right]^{\frac{1}{2}}$$

1.3.5.7 Bipolar collector capacitance charging time

The bipolar collector capacitance charging time is analogously similar to the emitter capacitance charging time. The bipolar collector charging time is associated with the collector resistance (e.g., sub-collector resistance) and the collector capacitance. This can be expressed as

$$\tau_{C} \approx r_{sc} C_{TC}$$

1.3.5.8 Silicon controlled rectifier (SCR) time response

Silicon controlled rectifiers (SCR) are used as ESD protection circuits on input nodes and power supplies. The time response of the SCR circuit is the sum of the base transit times across the *pnp* and *npn* bipolar transistor elements

$$\tau_{pnpn} = \tau_{pnp} + \tau_{npn}$$

where for the *pnp* bipolar device, the base transit time is

$$\tau_{pnp} = \frac{\left(W_{\mathrm{B}}^2\right)}{2D_n}$$

and for the *npn* bipolar device, the base transit time is

$$\tau_{npn} = \frac{\left(W_{\mathrm{B}}^2\right)}{2D_p}$$

1.3.5.9 MOSFET transit time

The MOSFET device has characteristic time constants associated with the transport of the carriers from the MOSFET drain to the source. The MOSFET channel transit time is equal to the MOSFET effective channel length, L_{eff}, divided by the carrier drift velocity, v_{d}, in the channel

$$\tau_{\mathrm{t}} = \frac{L_{\mathrm{eff}}}{v_{\mathrm{d}}}$$

The carrier drift velocity is equal to the product of the electron mobility and saturation electric field.

$$v_{\mathrm{d}} = \mu E_{\mathrm{sat}}$$

where the saturation electric field, E_{sat}, is equal to the MOSFET source-to-drain voltage divided by the MOSFET effective channel length, L_{eff}. The MOSFET source-to-drain transit time can be expressed as the

$$\tau_{\mathrm{t}} = \frac{L_{\mathrm{eff}}^2}{\mu V_0}$$

1.3.5.10 MOSFET drain charging time

The MOSFET drain charging time is the time it takes to charge up the drain node of a MOSFET. This is important in ESD networks in that for the MOSFET snapback voltage, there is a finite time for the MOSFET drain to rise. The MOSFET drain rise time is equal to the MOSFET drain resistance and the MOSFET drain capacitance. The drain resistance is a

function of the MOSFET drain sheet resistance, the MOSFET width, and the number of MOSFET fingers. The MOSFET drain capacitance is a function of the MOSFET channel width, the number of MOSFET fingers, and the MOSFET drain junction capacitance per unit area.

$$\tau_D \approx r_d C_D$$

This time constant is important in understanding the drain response during ESD events when a MOSFET structure is used as an ESD element, or in ESD MOSFET drain-coupling networks.

1.3.5.11 MOSFET gate charging time

The MOSFET gate charging time is the time it takes to charge the MOSFET gate electrode. This will be a function of the MOSFET gate resistance and the MOSFET gate-to-channel capacitance. The gate resistance is a function of the polysilicon MOSFET gate sheet resistance, the MOSFET channel length, the MOSFET width, and the number of MOSFET fingers. The MOSFET gate capacitance is a function of the MOSFET channel length, MOSFET channel width, the number of MOSFET fingers, and the gate capacitance per unit area

$$\tau_G \approx r_g C_G$$

1.3.5.12 MOSFET parasitic bipolar response time

During ESD events, the parasitic bipolar transistor plays a role in the response of a MOSFET transistor. The MOSFET bipolar base transit time is the time for a carrier to diffuse across the MOSFET drain to the MOSFET source, in the channel region. This is equal to the MOSFET channel length divided by the diffusion velocity in the MOSFET channel region; this can be expressed as a function of the MOSFET channel length, L_{eff}, and the diffusion coefficient, D, in the MOSFET channel region

$$\tau_t = \frac{L_{eff}^2}{2D}$$

This time constant is important in the understanding of the response of a MOSFET during fast ESD events.

1.3.6 Circuit Time Constants

1.3.6.1 Pad capacitance

In the analysis of the ESD response, the capacitance of the pad acts as a load in the ESD analysis. The pad capacitance influences the *RC* time of the network

$$C_{load} = C_{pad}$$

1.3.6.2 Half-pass transmission gates (TG)

The understanding of the time delays of the half-pass transmission gates is key to the response to receiver networks. Additionally, the time delays are also associated with the CMOS inverter propagation delay times.

1.3.6.3 n-Channel half-pass transistor charging time constant

The time delay in charging a output capacitance load, C_{out}, with a transmission gate voltage equal to V_{DD}, has a n-channel half-pass transmission gate charging time [64] of

$$\tau_{\text{ch}} = \frac{2C_{\text{out}}}{\mu_n C_{\text{ox}} \frac{W}{L} (V_{\text{DD}} - V_{\text{T}n})}$$

where the output voltage through the half-pass transmission gate can be expressed as [64]

$$V_{\text{out}}(t) = (V_{\text{DD}} - V_{\text{T}n}) \left[\frac{(t/\tau_{\text{ch}})}{1 + (t/\tau_{\text{ch}})} \right]$$

1.3.6.4 Half-pass transistor transmission gate discharge time constant

The half-pass transistor transmission gate discharge time constant to pass a logical "0" has a discharge time constant equal to

$$\tau_{\text{dis}} = \frac{C_{\text{out}}}{\mu_n C_{\text{ox}} \frac{W}{L} (V_{\text{DD}} - V_{\text{T}n})}$$

where the voltage at the output of the half-pass transistor has the form [64]

$$V_{\text{out}}(t) = (V_{\text{DD}} - V_{\text{T}n}) \left[\frac{2\exp(-t/\tau_{\text{dis}})}{1 + \exp(-t/\tau_{\text{dis}})} \right]$$

1.3.6.5 p-Channel half-pass transistor charging time constant

For the case of the p-channel half-pass transistor transmission gate, the charging and discharging time constants are analogous but opposite in form. For transmission of a logical "1"

$$V_{\text{out}}(t) = V_{\text{DD}} - \left(V_{\text{DD}} - V_{\text{T}p}\right) \left[\frac{2\exp(-t/\tau_{\text{ch}})}{1 + \exp(-t/\tau_{\text{ch}})} \right]$$

where

$$\tau_{\text{ch}} = \frac{C_{\text{out}}}{\mu_p C_{\text{ox}} \frac{W}{L} \left(V_{\text{DD}} - |V_{\text{T}p}|\right)}$$

For transmission of a logical "0," the discharge event can be expressed where the output voltage through the half-pass transmission gate can be expressed as [64]

$$V_{\text{out}}(t) = |V_{\text{T}p}| + \left(V_{\text{DD}} - |V_{\text{T}p}|\right)\left[\frac{(t/\tau_{\text{ch}})}{1 + (V_{\text{DD}} - |V_{\text{T}P}|)\,(2t/\tau_{\text{ch}})}\right]$$

1.3.6.6 Inverter propagation delay time constants

The propagation time constants associated with an inverter has the same nature as the time constants associated with the half-pass transmission gates. In an inverter, the charging and discharging of the load occurs through the p-channel MOSFET or the n-channel MOSFET identical to the half-pass transistor.

1.3.6.7 High-to-low and low-to-high transition time

The high-to-low transition time can be defined as a function of the charging and discharging times of an half-pass transmission gate (V_0 is 10% transition point of V_{DD}, or 0.1 V_{DD}) [64]

$$t_{\text{HL}} = \tau_n\left[\frac{2(V_{\text{T}n} - V_0)}{V_{\text{DD}} - V_{\text{T}n}} + \ln\left(\frac{2(V_{\text{DD}} - V_{\text{T}n})}{V_0} - 1\right)\right]$$

where

$$\tau_n = R_n C_{\text{out}}$$

$$R_n = \frac{1}{\mu_n C_{\text{ox}} \frac{W}{L}(V_{\text{DD}} - V_{\text{T}n})}$$

and

$$t_{\text{LH}} = \tau_p\left[\frac{2\left(|V_{\text{T}p}| - V_0\right)}{V_{\text{DD}} - |V_{\text{T}p}|} + \ln\left(\frac{2\left(V_{\text{DD}} - |V_{\text{T}p}|\right)}{V_0} - 1\right)\right]$$

where

$$\tau_p = R_p C_{\text{out}}$$

$$R_p = \frac{1}{\mu_p C_{\text{ox}} \frac{W}{L}\left(V_{\text{DD}} - |V_{\text{T}p}|\right)}$$

1.3.6.8 Inverter propagation delay time

The CMOS inverter propagation delay time can be represented as [64]

$$t_{\text{P}} = \frac{1}{2}[t_{\text{HL}} + t_{\text{LH}}]$$

1.3.6.9 Series n-channel MOSFETs discharge delay time

Given a set of *n*-channel transistors in a series configuration, the transistors serve as a series of half-pass transistors. The transistors each have a corresponding diffusion capacitance from the MOSFET source and drain diffusion; each MOSFET channel region serves as the series resistance element. To evaluate the delay time constant for a series-connected MOSFETs this can be treated as a lumped *RC* transmission line or *RC* ladder network. A simplified solution for *N* transistors in a series configuration, the delay time can be estimated as the superposition of time constants [64]

$$t_{\mathrm{D}} \cong \sum_{i=0}^{N-1} \tau_i$$

For each time constant in the expression, the ith element in the *RC* ladder network is the product of the ith capacitor element and the summation of all the resistances to the ith element,

$$\tau_i = \left(\sum_{j=0}^{i} R_j \right) C_i$$

where for *n*-channel MOSFET devices

$$R_j = \frac{1}{\mu_{nj} C_{\mathrm{ox}} \frac{W_j}{L_j} (V_{\mathrm{DD}} - V_{\mathrm{T}n})}$$

1.3.6.10 Series p-channel MOSFETs charge delay time

Given a set of *p*-channel transistors in a series configuration, the transistors serve as a series of half-pass transistors. The transistors each have a corresponding diffusion capacitance from the MOSFET source and drain diffusion; each MOSFET channel region serves as the series resistance element. As in the *n*-channel case, to evaluate the delay time constant for a series connected MOSFET, this can be treated as a lumped *RC* transmission line, or *RC* ladder network. A simplified solution for *N* transistors in a series configuration, the delay time can be estimated as the superposition of time constants [64]

$$t_{\mathrm{D}} \cong \sum_{i=0}^{N-1} \tau_i$$

For each time constant in the expression, the *i*th element in the *RC* ladder network is the product of the *i*th capacitor element and the summation of all the resistances to the *i*th element

$$\tau_i = \left(\sum_{j=0}^{i} R_j \right) C_i$$

where

$$R_j = \frac{1}{\mu_{pj} C_{\mathrm{ox}} \frac{W_j}{L_j} \left(V_{\mathrm{DD}} - |V_{\mathrm{T}p}| \right)}$$

1.3.7 Chip Level Time Constants

On the semiconductor chip level, the critical chip time constants of interest to ESD protection is the global time constants and the package level time constants:

- Peripheral I/O power bus time constant.
- Core chip power grid time constant.
- Substrate time constant.
- Package level time constants.

1.3.7.1 Peripheral I/O power bus time constant

During ESD events, the current flows through the ESD network to the power bus. Along the power bus is a plurality of peripheral circuit books. The peripheral circuits contain pads, ESD networks, and the receiver or transmitter books. The peripheral power bus extends over these circuits in a regular spacing. Hence, we can represent the power bus time constant as a RC ladder network. The incremental resistor element is the bus resistance between adjacent peripheral I/O cells, and the incremental capacitance element is the loading of the individual peripheral circuits books, and the bus capacitance. The incremental bus resistance is

$$R_{\mathrm{bus}} = \left(\frac{\rho}{t_{\mathrm{film}}} \right) \frac{L}{W_{\mathrm{bus}}}$$

where L is the spacing between adjacent I/O cells, W_{bus} is the bus width. The incremental capacitance is the incremental bus capacitance term and the book capacitance

$$C = C_{\mathrm{bus}} + C_{\mathrm{book}}$$

and incremental capacitance

$$C_{\mathrm{bus}} = \varepsilon_{\mathrm{eff}} \frac{L W_{\mathrm{bus}}}{d}$$

The number of external pins can be estimated from the number of circuits in the semiconductor chip according to Rent's Rule [65]

$$N_{\mathrm{p}} = K_{\mathrm{p}} N_{\mathrm{g}}^{\beta}$$

where N_{p} is the number of external pins, N_{g} is the number of total gates, and K_{p} and β are proportionality constants [65]. From the knowledge of the chip size and the number of circuits, the number of pins along the bus can be estimated.

1.3.7.2 Core chip time constant

The response time of the core chip is a function of the total chip capacitance. The chip capacitance is proportional to the number of circuits and the capacitance per internal circuit.

From Rent's Rule, knowing the number of I/O pins, we can estimate the number of internal circuits.

$$N_g = \left(\frac{N_p}{K_p}\right)^{\frac{1}{\beta}}$$

From this expression, knowing a capacitance of a typical inverter circuit, the loading effect on the power grid can be estimated. Assume the loading capacitance of a typical network is C_g, an estimate of the total circuit capacitance loading can be expressed as

$$(C_g)_T = C_g N_g = C_g \left(\frac{N_p}{K_p}\right)^{\frac{1}{\beta}}$$

The total chip capacitance can also include the decoupling capacitors that are added to increase the total chip capacitance [65].

$$C_{chip} = C_{decap} + (C_g)_T = C_{decap} + C_g \left(\frac{N_p}{K_p}\right)^{\frac{1}{\beta}}$$

In evaluation of the chip response, the resistance and the capacitance both play a role. The estimate of the resistance is a function of the architecture and chip design methodology. Hence, there is an *RC* time associated with the chip response.

1.3.7.3 Substrate time constants

The response of the chip substrate also plays a role in ESD phenomenon. On a global level, the substrate time constant is a function of the substrate resistance and the substrate contact density. From Rent's Rule, we can project the number of substrate contacts in the core of the chip from the knowledge of the internal number of circuits. Knowing the number of internal gates, we can assume that there is a substrate contact for some proportionality constant for every circuit. This is a valid assumption, since for latchup it is required to have a local substrate contact within a given distance from all circuits, assuming some proportionality constant, α

$$(N_{sx})_{Core} = \alpha N_g$$

The spacing of the substrate contact relative to the circuit and the size of the average internal circuit will lead to the defining of the proportionality constant. Additionally, for the peripheral circuits, we can assume each I/O circuit has a substrate contact

$$(N_{sx})_{I/O} = K_p N_g^{\beta}$$

The incremental resistance between substrate contacts will be a function of the chip area, the contact-to-contact spacings, and the substrate resistance. This network will form a two-dimensional resistance grid. Hence the substrate network will primarily be a time constant associated with a resistance network. The resistance distribution will respond as a resistance–conductance (*RG*) transmission line. For the substrate, the capacitance formed between the substrate and the package has a role in the capacitance coupling during a charged device model (CDM).

1.3.7.4 Package time constants

In ESD events, packages have an influence on HBM, MM, and CDM events. The package can be modeled as a capacitor–inductor lumped parameter. A typical package model will consist of a π-network, consisting of a first shunt capacitor, a series inductor, and a second shunt capacitor element. In some package designs, the lead frames and wire bond also serve as a series inductors elements. At high frequencies or packages with high inductance, the package can influence the ESD event waveform and the circuit response.

1.3.8 ESD Time Constants

1.3.8.1 ESD time constants

To understand physical phenomena, and particularly ESD phenomenon, it is necessary to quantify the scale in both space and time. ESD phenomena involves microscopic to macroscopic scales. ESD phenomena involves electrical and thermal transport on the scale of nanometers, circuits and electronics on the scale of micrometers, semiconductor chip designs on the scale of millimeters, and systems on the scale of meters. The time scales of interest range from picoseconds (ps) to microseconds (μs). Electrical currents of interest range from milliamps (mA) to tens of amperes (A). The voltage range of interest varies from volts (V) to kilovolts (kV). Temperatures vary from room temperature to melting temperatures of thousands of degrees Kelvin. It is the vast ranges of time, space, currents, voltages, and temperature as well as its transition from the microscopic to the macroscopic which makes ESD phenomenon difficult to model, simulate, and quantify.

To comprehend ESD phenomenon and establish validity of analytical developments, it is important to be able to understand what phenomenon is important. By analyzing the physical equations from a time constant approach, equations and understanding can be made both rigorous as well as improve logical clarity.

1.3.8.2 ESD events

To understand the role of ESD events and the physical environments, it is important to quantify the characteristic times of an ESD event. ESD events are represented as circuit equivalent models. Figure 1.3 contains the ESD time constant hierarchy.

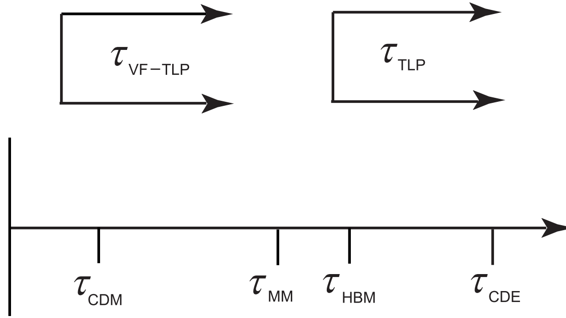

Figure 1.3 Electrostatic discharge (ESD) time constant hierarchy

1.3.8.3 Human body model characteristic time

A fundamental model used in the ESD industry is known as the HBM pulse [18,66–68]. The model was intended to represent the interaction of the electrical discharge from a human being, who is charged, with a component or object. The model assumes that the human being is the initial condition. The charged source then touches a component or object using a finger. The physical contact between the charged human being and the component or object allows for current transfer between the human being and the object. A characteristic time of the HBM is associated with the electrical components used to emulate the human being. In the HBM standard, the circuit component to simulate the charged human being is a 100 pF capacitor in series with a 1500 Ω resistor. This network has a characteristic rise time and decay time. The characteristic decay time is associated with the time of the network

$$\tau_{\mathrm{HBM}} = R_{\mathrm{HBM}} C_{\mathrm{HBM}}$$

where R_{HBM} is the series resistor and C_{HBM} is the charged capacitor. This is a characteristic time of the charged source. A more accurate understanding of the waveform and time constant is needed to evaluate the circuit response. The RC time constant only addresses the decay time of the waveform, and does not quantify the rise time. A more accurate representation of the HBM event addresses the series inductance. Roozendaal treated the HBM waveform as a lumped *RLC* network consisting of the source capacitor, a series inductor, and series resistor [69]. The current as a function of time from the HBM event can be expressed as a double exponential waveform

$$I(t) = \frac{V_{\mathrm{C}}}{R}\left(1 - \exp\left\{-\frac{R}{L}t\right\}\right)\exp\left(-\frac{t}{RC}\right)$$

The addition of the inductor introduces an *L/R* time constant into the HBM waveform expression. This can also be expressed in as a hyperbolic form as the solution of the *RLC* network

$$I(t) = V_{\mathrm{C}} C \frac{\omega_{\mathrm{o}}^2}{\sqrt{\left(\left(\frac{R}{2L}\right)^2 - \omega_{\mathrm{o}}^2\right)}} \frac{V_{\mathrm{C}}}{R}\left(\exp\left\{-\frac{R}{2L}t\right\}\right)\sinh\left(t\sqrt{\left(\frac{R}{2L}\right)^2 - \omega_{\mathrm{o}}^2}\right)$$

where the resonant frequency is

$$\omega_o = \frac{1}{\sqrt{LC}}$$

For the HBM pulse waveform, the $R/2L$ time constant is greater than the LC resonant time constant. The rise time is dominated by this time constant, where

$$t_r \cong \frac{2L}{R}$$

The inductance in the HBM simulators are in the range of 5–10 μH, leading to rise times of the order of 17–22 ns [66–68].

1.3.8.4 Machine model characteristic time

Another fundamental model used in the ESD industry is known as the machine model (MM) pulse [21,70–73]. The model was intended to represent the interaction of the electrical discharge from a conductive source, which is charged, with a component or object. The model assumes that the ''machine'' is charged as the initial condition. The charged source then touches a component or object. In this model, an arc discharge is assumed to occur between the source and the component or object allowing for current transfer between the charged object and the component or object. A characteristic time of the machine model is associated with the electrical components used to emulate the discharge process. In the MM standard, the circuit component is a 200 pF capacitor with no resistive component. An arc discharge fundamentally has a resistance on the order of 10–25 Ω. The characteristic decay time is associated with the time of the network

$$\tau_{MM} = R_{MM}C_{MM}$$

where R is the arc discharge resistor and C is the charged capacitor. This is a characteristic time of the charged source.

The simplified expression does not address the waveform observed from test simulators. The MM waveform contains both oscillation and an exponential decay. The current waveform as a function of time for the simulated MM pulse is [69]

$$I(t) = V_C\sqrt{\frac{C}{L}}\left(\sin\left\{\frac{t}{\sqrt{LC}}\right\}\right)\left(\exp\left\{-\frac{R}{L}t\right\}\right)$$

In this form, it is apparent that the waveform peak is a function of the initial voltage on the source capacitor. The oscillatory nature of the MM waveform is a function of the LC time constant. The damping factor is a function of the R/L time constant; as the R/L time constant increases, the current waveform decays at a faster rate.

1.3.8.5 Charged device model characteristic time

The CDM represents an ESD interaction between a chip and a discharging means where the chip is pre-charged. The charging process can be initiated by direct charging or field-induced

charging. The discharge process is initiated as contact is initiated between the charged device and the discharging means [25,74–76].

1.3.8.6 Charged cable model characteristic time

Another fundamental model used in the ESD industry is known as the charged cable model or cable model pulse. The model was intended to represent the interaction, the electrical discharge of a charged cable, discharging to a chip, card or system. To initiate the charging process, a transmission line or cable is dragged on a floor leading to tribo-electric charging. The model assumes that the cable is charged as the initial condition. The charged cable source then touches a component or object. A characteristic time of the cable model is associated with the electrical components used to emulate the discharge process. In the charged cable model, the cable acts as a capacitor element. The characteristic decay time is associated with the time of the network

$$\tau_{\mathrm{CCM}} = R_{\mathrm{CCM}} C_{\mathrm{CCM}}$$

where R is the discharge resistor and C is the charged cable. The capacitance used for this model is 1000 pF. In early development times, this model was treated as an RC response model, where a very large capacitor represented the cable.

1.3.8.7 Cable discharge event (CDE) model

In recent years, this model has evolved into the cable discharge event (CDE) model [77–82]. In early development, this was a concern for large system cables. System level engineers are required to improve system-level performance while maintaining the quality and reliability. ESD and electromagnetic emissions (EMI) are a concern in systems. System level standards and system engineers have long known that charged cables can also introduce system-level concerns. Charge accumulation on unterminated twisted pair (UTP) cables occur through both tribo-electric charging and induction charging. In the case of tribo-electrification, in a UTP cable can be dragged along a floor. A positive charge is established on the outside surface of the insulating film. The positive charge on the outside of the cable attracts negative charge in the twisted pair leads across the dielectric region. When the negative charge is induced near the outside positive charge, positive charge is induced in the electrical conductor at the ends of the cable. As the cable is plugged into a connector, electrical arcing will occur leading to a charging of the unterminated twisted pair (note: the twisted pair was neutral to this point). If a cable is introduced into a strong electric field, induction charging will occur. When the electric field is removed the cable remains charged until a discharge event from grounding occurs. With the integration of wide area networks (WAN), and local area network (LAN), the Ethernet is playing a larger role [77–82]. When a charged twisted pair cable connects to an Ethernet port with a lower electrical potential, cable discharge events can occur in LAN systems. In the past, standards (e.g., IEEE 802.3 Section 14.7.2) have noted the potential for CDE processes in LAN cables. Additionally, the introduction of Category 5 and Category 6 cables have significantly low leakage across the dielectric. As a result, when a tribo-electric charge is established, the conductance of the insulator is so low

that the induced charge can maintain for long time scales (e.g., 24-h period). The CDE produces a rectangular pulse whose pulse width is a function of the length of the cable, L. The pulse width can be expressed as follows:

$$\tau_{CDE} = \frac{2L}{v} = \frac{2L\sqrt{\mu_{eff}\varepsilon_{eff}}}{c_0}$$

1.3.8.8 Charged cassette model characteristic time

The charged cassette model (CCM) is a recent model associated with consumer electronics. In consumer electronics there are many applications where a human plugs a small cartridge or cassette into a electronic socket. These are evident in popular electronic games. In today's electronic world, there are many palm-size electronic components which must be inserted into a system for non-wireless applications. To verify the electronic safety of such equipment, the cassette itself is assumed as a charged source. The ''cassette model'' assumes a small capacitance and negligible resistance. This model is equivalent to a machine model type current source with a much lower capacitor component. The model assumes the resistance of an arc discharge and a capacitance of 10 pF.

1.3.8.9 Transmission line pulse (TLP) model characteristic time

Transmission line pulse (TLP) testing has seen considerable growth in the ESD discipline [83–87]. In this form of ESD testing, a transmission line cable is charged using a voltage source. The TLP system discharges the pulse into the device under test (DUT). The characteristic time of the pulse is associated with the length of the cable.

The pulse width of a TLP is a function of the length of the transmission line and the propagation velocity of the transmission line. The propagation velocity is can be expressed relative to the speed of light, as a function of the effective permittivity and permeability of the transmission line source.

$$\tau_{TLP} = \frac{2L_{TLP}}{v} = \frac{2L_{TLP}\sqrt{\mu_{eff}\varepsilon_{eff}}}{c_o}$$

TLP systems are designed in different configurations. TLP system configurations include current source, time domain reflectometry (TDR), time domain transmission (TDT), and time domain reflectometry and transmission (TDRT) [83]. In all configurations, the source is a transmission line whose characteristic time constant is determined by the length of the transmission line cable. The various TLP configurations influence the system characteristic impedance, the location of the DUT, and the measurement of the transmitted or reflected signals.

For this method, the choice of pulse width is determined by the interest to use TLP testing as a equivalent or substitute method to the HBM methodology. The standard practice today, the TLP cable length is chosen as to provide a TLP pulse width of 100 ns with less than 10 ns rise time [83,87].

1.3.8.10 Very fast transmission line pulse (VF-TLP) model characteristic time

Very fast TLP (VF-TLP) test method is similar to the TLP methodology [88–90]. The interest in VF-TLP testing is driven by the desire to have an understanding semiconductor devices in a time regime similar to the CDM time constant. The characteristic time of interest is again determined by the propagation characteristics of the transmission line cable source and the length of the transmission line cable.

$$\tau_{\text{VF-TLP}} = \frac{2L_{\text{VF-TLP}}}{v} = \frac{2L_{\text{VF-TLP}}\sqrt{\mu_{\text{eff}}\varepsilon_{\text{eff}}}}{c_0}$$

VF-TLP pulse width of interest is a pulse width of less than 5 ns and a sub-1 ns rise time [88–92]. This time regime is well below the thermal diffusion time constant in semiconductor media. The method of the fast time constant limits the acceptable configurations of the VF-TLP system and suitable equipment for measurement.

1.4 CAPACITANCE, RESISTANCE, AND INDUCTANCE AND ESD

1.4.1 The Role of Capacitance

In the understanding of ESD events, it is important to understand the role of capacitance, resistance, and inductance and where it comes into play in the analysis. Capacitance has a role in the capacitive loading effects in networks, timing circuits, as well as charge storage, charge distribution, and displacement current in ESD events. In ESD design, capacitance has a role in the following environments:

- Capacitance loading effects of ESD protection networks for signal pads.
- *RC*-discriminator networks for frequency-dependent trigger networks for signal and power pads.
- Current distribution within an ESD network at high speed and radio frequency (RF) GHz applications.
- Current distribution within a chip power rails and power grid.
- Chip or system impedance (e.g., $Z = 1/j\omega C$).
- *LC* transmission lines for RF applications.

Capacitance loading effects are a concern for receiver networks because it impacts circuit performance objectives. As the application frequency increases, circuit designs desire to lower the ESD input network capacitance loading. For example, in some applications it is desired to maintain a constant reactance, then as the functional frequency increases, the ESD loading capacitance decreases accordingly.

Capacitance also plays a role in trigger networks which tune the *RC* time constant so that the ESD network responds to the ESD pulse. Circuits are designed to respond to the ESD impulse but not to the power-up or functional frequencies, discriminating the response to ESD events instead of functional applications.

For RF applications, the role of the capacitance influences the frequency response of the ESD network as well as its location on a Smith Chart.

Capacitance also plays a role in the way in which current distributes through a semiconductor chip power grid. The capacitance per unit distance of the power bus plays a role in how the current distributes within a semiconductor chip.

Capacitance plays a role in the impedance (or effective impedance) of the whole chip. The chip or system impedance (e.g., $Z = 1/j\omega C$) plays a key role in the ability to displace current across the chip (note: $I = C\,\mathrm{d}V/\mathrm{d}t$). In RF applications, capacitance plays a role in the LC transmission line elements used in RF applications.

Hence, the understanding of lumped and distributed capacitance is fundamental in ESD events. Capacitance is key from the local ESD element, circuits as well as the global capacitance components of a semiconductor chip. It can be observed locally within a semiconductor device, a circuit or globally on a chip level.

1.4.2 The Role of Resistance

Resistance is one of the most important parameter in ESD events. The role of resistance is critical in the voltage and current distribution within a semiconductor device, circuit, or network. The understanding of resistance and the resistance distribution plays a more significant role compared to inductance and capacitance issues. Typically, inductance plays an important role in the effect of lead frames and packages on the ESD response, but play a minor role in the understanding of ESD devices and circuit response in semiconductor chip environments. Capacitance also plays a key role when the RC time of the wiring is of the order of the characteristic time of the event. Hence, the understanding of lumped and distributed resistance systems is fundamental in ESD events. Resistance plays a key role from the local current distribution within a diode structure, a MOSFET structure, off-chip driver circuits, to global current distribution in the metal busses, and the chip substrate.

In ESD design, resistance has a role in the following environments:

- Voltage distribution and on-resistance within an ESD protection structure.
- Voltage distribution and on-resistance within the protected circuit.
- Voltage and current distribution through the power grid.
- Voltage and on-resistance of the ESD power clamps.
- RC-discriminator networks for frequency-dependent trigger networks for signal and power pads.
- Current distribution within an ESD network at high speed and radio frequency (RF) GHz applications.

Resistance plays a fundamental role in the operation of an ESD protection circuit. Voltage distribution and on-resistance within an ESD protection structure is critical in order to provide an effective ESD structure. Additionally, the resistance also plays a role in the Joule heating within the ESD structure.

The voltage distribution and on-resistance within the protected circuit is also critical in the understanding of the failure of an ESD network. The voltage and current distribution

through the power grid is critical in that it influences the peak voltage and current in the system. Resistance also plays a role in the way in which current distributes through a semiconductor chip power grid. The resistance of the power grid also decreases the voltage margin between the ESD current path and the voltage at the protected circuit of interest. These factors can drive the effectiveness of the ESD strategy, and can determine power clamp circuit placement.

In the ESD power clamps, the net resistance also plays a role in the ESD event. The resistance of the power grid also decreases the voltage margin between the ESD current path and the voltage at the protected circuit of interest.

Hence, the understanding of lumped and distributed resistance is fundamental in ESD events. Resistance is key from the local ESD element, circuits as well as the global capacitance components of a semiconductor chip. It can be observed locally within a semiconductor device, a circuit, or globally on a chip level.

1.4.3 The Role of Inductance

In the understanding of ESD events, it is important to understand the role of inductance and where it comes into play in the analysis. Inductance has a lesser role compared to resistance and capacitance effects. Inductance primary role occurs in package lead frames, wire bonds, package pins, and the package itself. In analog and mixed signal (A&MS), RF CMOS, and RF BiCMOS applications, inductors are used in circuits for dc-biasing and blocking, LC transmission lines, LC tank circuits, and other RF circuit applications. In ESD design, inductance has a role in the following environments:

- Packaging lead frames.
- Package wire bonds.
- Package pins.
- RF circuit elements—LC transmission lines.
- RF circuits with dc-biasing.
- RF ESD circuits.

Package lead frames and wire bonds can influence the inductive coupling between power rails and influence circuit response. To reduce the on-chip noise, power rails are reconnected at the package lead frame, or pads, or at the package. In this fashion, the package inductance plays a role in the response of peripheral circuits which have disconnected power and ground rails on the chip.

Inductance is also playing a more critical role with the introduction of inductors and transmission lines as design elements. Inductors are used in dc-biasing networks, LC tank circuits and are being introduced into ESD networks. Inductors are being introduced to provide distributed networks isolated for lowering the effective loading of ESD elements. As a result, the understanding of lumped and distributed LC transmission lines in key to understanding the effect of inductance on ESD events. Hence, the understanding of lumped and distributed inductance is fundamental to ESD understanding in packaging and RF applications.

1.5 RULES OF THUMB AND ESD

1.5.1 ESD Design an "ESD Ohm's Law": A Simple ESD Rule-of-Thumb Design Approach

In the semiconductor industry, the ability to understand the influence of ESD on semiconductor chips is difficult for those who are not semiconductor device engineers or circuit designers. An "ESD Ohm's Law" is needed to provide a simplistic but adequate ESD design practice. A simple rule-of-thumb for analysis was needed for design sizing and estimation. The following ESD Ohm's law rule-of-thumb approach is recommended:

- Determine the voltage of the dielectric breakdown or MOSFET snapback of the circuit that requires protection.
- Find all the turn-on voltages and effective resistances through the chip from the input pad to the chip ground plane substrate and estimate the resistances to the nearest ohm in the "ESD current loop."

1. ESD element.
2. Wire bussing between the signal pad and the nearest ESD power clamp.
3. ESD power clamp.

- In the case of a chip without an ESD power clamp, assume a frequency of the ESD pulse, and a total chip capacitance to evaluate the net impedance (e.g., $Z = 1/j\omega C$ where ω is the ESD pulse of interest). Assume a frequency associated with 100 ns for HBM, 10 ns for MM, and 1 ns for CDM events.
- Assume a 1 A direct current (dc) flowing through the ESD current loop circuit and evaluate the sum of the voltage drops in the "ESD current"

$$V_T = \sum_{i=1}^{i=n} \left[(V_T)_i + I_{ESD}(R)_i \right]$$

where V_T is the total voltage drop, and within the summation, V_T is the turn-on voltage and R is the resistance of the elements in the ESD current loop path. The summation is the sum of all elements in the ESD current loop path (Figure 1.4).

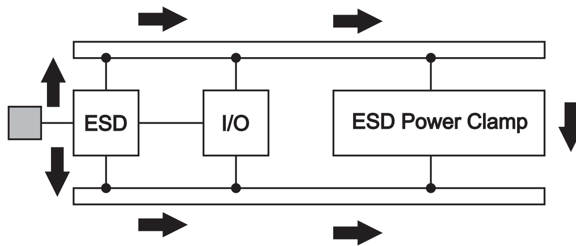

Figure 1.4 ESD current path

- Evaluate the voltage margin between V_T and the failure voltage of the protected circuit, V_f. This determines the voltage margin to failure.

$$V_T - V_f = \left\{ \sum_{i=1}^{i=n} \left[(V_T)_i + I_{ESD}(R)_i \right] \right\} - V_f$$

- If the voltage margin is positive, there is margin prior to circuit failure. If the voltage margin is negative, the protected network will fail prior to distributing 1 A of current.

This simple development is useful as a rule-of-thumb analysis without semiconductor device design tools and circuit simulation. This method will allow a quick understanding of the resistances and turn-on voltages in order to design an effective strategy. From this method, one can have a sense of the size of the ESD element, the bus widths, and the size of the ESD power clamp. Additionally, in many large chips, knowing the chip impedance, one can determine if an ESD power clamp is necessary.

1.6 LUMPED VERSUS DISTRIBUTED ANALYSIS AND ESD

1.6.1 Current and Voltage Distributions

To provide an effective ESD design strategy, the ESD design practices must focus on the local and global distribution of electrical and thermal phenomena in devices, circuits, and systems. In order to shunt the ESD current efficiently and effectively, the distribution of the current is critical in ESD design. As the current distributes, the effectiveness of the device improving the utilization of the total area of the ESD network or circuit element. On a circuit and system level, the distribution of the ESD current within the network or system lowers the effective impedance and the voltage condition within the ESD current loop. A key design practice and focus in ESD development is the distribution effects. The ESD events are transient events; the physical time constants of the devices, circuits, and systems are critical in the understanding, modeling, and simulation of the effectiveness of the elements in the system. A key design practice of ESD devices and circuits is the desire to distribute the current to provide improved design utilization to achieve higher ESD robustness.

1.6.2 Lumped versus Distributed Systems

In the analysis of ESD events, the understanding of the current and voltage distribution within a semiconductor device, a circuit, or a chip is important for modeling, evaluating the efficiency, as well as quantifying the area of the network which is involved in space and in time.

In devices, circuits, interconnects, ESD circuits, and even test equipment, the distribution of voltage and current is key to understanding as well as analysis. In ESD phenomenon, voltage drops occur in the metal wiring pattern of single- and multi-finger elements such as diodes and MOSFETs form distributed current distribution. Off-chip driver (OCD) networks are also sensitive to the current and voltage distribution at these high-current levels. The metal bus of the power rail and the ground rail also has a role in the ESD analysis. The

semiconductor substrate also serves as a lossy distributed region where current is flowing. Additionally, even the test equipment utilize transmission line cables for forming the ESD test in TLP testing and very fast-transmission line pulse (VF-TLP) systems.

In the case of modeling ESD events in devices, circuits, or chips, the question arises of whether the element or network should be treated as a single lumped element, or a distributed element. The decision of treating an element as a lumped element, or a distributed set of elements (e.g., a ladder network or a transmission line) can be quantified as a competition between the rise time of an ESD event and the time of flight through the network.

Let us define the time of flight as

$$\tau = \frac{l}{v}$$

where l is the length of the structure, and v is the propagation velocity.

When some integer number of the time of flight is larger than the ESD event rise time, then the network should be modeled as a ladder network or distributed network. When some integer number of the time of flight is less than the rise time, the network can be treated as a lumped element.

In transmission line theory, a rule-of-thumb used is if the rise time is equal to

$$t_{\mathrm{r}} < 2.5\tau$$

then the structure should be modeled as a ladder network or transmission line [64,93–97]. When the ESD event rise time is significantly slower than the time of flight, the voltage is not uniform. Hence in cases of HBM pulses, whose rise time is 17–22 ns, if the structure is such that the time of flight is approximately 10 ns, the structure should be modeled as a transmission line. In the transmission line theory, the structure can be modeled as a lumped capacitor element if [64,93–97]

$$t_{\mathrm{r}} > 5\tau$$

Hence, when the rise time is greater than five ‘‘bounce’’ times, the system can be treated as a single component element. This analysis is valid for understanding of the voltage distribution in packaging, power grids, and substrates where there is a low-loss component.

In the case of lossy systems, where resistance has a dominant role, the voltage drops in the system also play a significant role in the modeling as a lumped or distributed system. During ESD events, the resistance plays an important role in the power bus, the ESD element, and ESD power clamps.

A good rule-of-thumb for ESD events in the decision of whether the device, circuit, or power grid should be treated as a lumped or distributed system should be as follows:

- When the ESD current through the system introduces voltage drops greater than 0.25 V, the element should be separated into a distributed network.

One reason for this rule-of-thumb is that ESD structures incorporate forward-bias diode elements on the order of 0.7 V. When the voltage drop across the device is greater than 0.25, some sections of the device are forward active, and some are not. In this case, the element should be separated into a resistance-diode ladder network.

A second reason for this rule-of-thumb is the resistance in the power bus are of 0.25–5 Ω. When 1 A of current is forced through the power bus, the voltage drops will be of the order of 0.25–5 V; for the case of 3 A, the results are greater than 1 V drop. At these levels, the input circuit will see a higher voltage on the input node of this magnitude. Hence, the power rail should be segmented into a resistance–conductance (RG) ladder network, or a resistance–capacitance (RC) ladder network.

1.6.3 Distributed Systems: Ladder Network Analysis

In the understanding of distributed networks and ESD protection evaluation, it is important to obtain how the ESD current distributes along a structure. Treating the ESD element as a distributed two-port network, we can treat the input side as the port (1) and the output side as port (2). In the two-port network, we can quantify the impedance distribution between the input port and the output port by treating the network as a ''ladder network'' consisting of impedances along the top of the network (numbered in an odd succession), and as admittances between the top and bottom (numbered in an even succession) [97]. Figure 1.5 shows a ladder network. The ladder network is used in the treatment of analysis for ESD design in MOSFETs [98,99]. The voltage and current can be expressed as

$$V_1(s) = z_{11}(s)I_1(s) + z_{12}(s)I_2(s)$$
$$V_2(s) = z_{21}(s)I_1(s) + z_{22}(s)I_2(s)$$

By applying conditions to the current and voltages at the input and output port, the z-parameters can be solved for. To solve for the impedance term z_{11} of the matrix, we can let the output current to be equal to zero

$$z_{11}(s) = \left.\frac{V_1(s)}{I_1(s)}\right|_{I_2(s)=0}$$

The impedance can be expressed as the sum of first impedance element and the impedance looking into the network (which we will designate alphabetically) [97]

$$z_{11}(s) = Z_1(s) + Z_a(s)$$

with the corresponding admittance

$$Y_a(s) = \frac{1}{Z_a(s)}$$

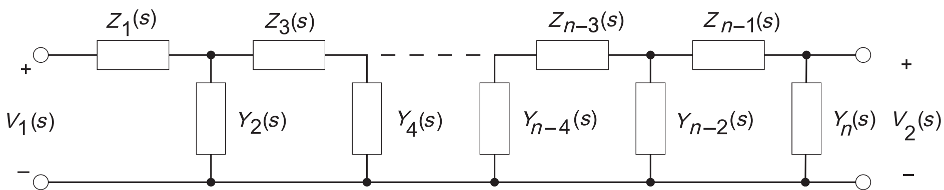

Figure 1.5 Two-port ladder network

The admittance term can be expressed as the sum of the first admittance term and the inverse of the impedance looking in

$$Y_a(s) = Y_2(s) + \frac{1}{Z_b(s)}$$

Substituting this into the impedance term, we can express this as

$$z_{11}(s) = Z_1(s) + \frac{1}{Y_2(s) + \frac{1}{Z_b(s)}}$$

This step can be repeated continuously down the rungs of the ladder network as

$$z_{11}(s) = Z_1(s) + \cfrac{1}{Y_2(s) + \cfrac{1}{Z_3(s) + Z_c(s)}}$$

and

$$z_{11}(s) = Z_1(s) + \cfrac{1}{Y_2(s) + \cfrac{1}{Z_3(s) + \cfrac{1}{Y_4(s) + \cfrac{1}{Z_5(s) + Z_d(s)}}}}$$

and repeated to the last admittance element $Y_n(s)$

$$z_{11}(s) = Z_1(s) + \cfrac{1}{Y_2(s) + \cfrac{1}{Z_3(s) \cfrac{1}{Y_4(s) + \ddots \cfrac{1}{Y_n(s)}}}}$$

In this form, the impedance term is expressed as the Stieljes continued fraction [97]. The solution for the output impedance term z_{22} (s) can be solved in the same manner, but reversing the process.

For ESD analysis of the dc or ac frequency response, the ability to quantify a resistor, a diode, or a MOSFET as a distributed system allows to quantify the ESD efficiency at which an ESD structure or I/O network distributes the ESD current. All the distributed models discussed in ESD analysis are forms of the ladder network but using either different mathematic techniques or boundary assumptions. One of the distinctions is that when the ladder network is traversed, there are voltage drops or “on state” assumptions to connect the two electrodes.

1.6.4 Resistor–Inductor–Capacitor (RLC) Distributed Systems

Resistance, inductance, and capacitance play a role in the voltage and current distribution during ESD events which address inductive components, lossy transmission lines, lead frames, and packaging effects [65].

On a semiconductor device level, typically inductive effects are not an issue unless inductor components are added to the network. In RF CMOS and RF BiCMOS networks, inductors are present as lumped elements. In some ESD networks, the lumped components are used as a plurality of elements to form a multiple lumped-element distributed network. The multiple lumped-element networks take advantage of the transmission line nature of a distributed system. Hence, although they are lumped components, the complete ESD network behaves as a distributed network.

Transmission lines (T-lines) are also formed in RF components as components between the pads and receiver networks. Typically, these are low-resistance components formed using metal films.

Transmission lines are also present in the ESD test systems themselves. TLP systems incorporate transmission lines in the network to initiate and shape the pulse to simulate ESD events.

On a global chip level, inductance plays a role in the power bus, ground bus, wire bonds, package lead frames, and pins. In the analysis of the current distribution during an ESD event, inductive effects can play a role.

The incremental variation also plays a role in the voltage and current response during high-current ESD operation. To analyze the incremental variation from point z to a second point $(z + \mathrm{d}_z)$, assume a resistance term $R(z)\,\mathrm{d}z$ where $R(z)$ is the resistance per unit length over increment $\mathrm{d}z$.

In series with the resistance element, an inductor is added of the form $L(z)\,\mathrm{d}z$ where $L(z)$ is the inductance per unit length over increment $\mathrm{d}z$. Between the top surface and bottom surface of the transmission line, there is a capacitor per unit distance $C(z)\,\mathrm{d}z$. In parallel with the capacitance, a conductance term, $G(z)\,\mathrm{d}z$ is added where $G(z)$ is the conductance per unit length over increment $\mathrm{d}z$ [64].

Forming a two-port network where the input current is $I(z, t)$, and input voltage $V(z, t)$ at input port z, and the output current $I(z + \mathrm{d}_z, t)$ and output voltage $V(z + \mathrm{d}_z, t)$, a coupled set of equation can be formed with differential voltage can be represented as the voltage potential difference across resistance $R(z)\,\mathrm{d}z$ as well as the voltage drop across the incremental inductor $L(z)\mathrm{d}z$ [64]

$$\mathrm{d}V(z,t) = -I(z,t)[R(z)\mathrm{d}z] - [L(z)\mathrm{d}z]\frac{\mathrm{d}I(z,t)}{\mathrm{d}t}$$

and the differential current can be represented as the charge across the capacitor $C(z)$ during increment of time $\mathrm{d}t$, and current through the conductance term [64]

$$\mathrm{d}I(z,t) = -[G(z)\mathrm{d}z]V(z,t) - [C(z)\mathrm{d}z]V(z,t)\mathrm{d}t$$

This can be expressed as a set of coupled differential equations as

$$\frac{\partial V(z,t)}{\partial z} = -R(z)I(z,t) - L(z)\frac{\partial I(z,t)}{\partial t}$$
$$\frac{\partial I(z,t)}{\partial z} = -G(z)V(z,t) - C(z)\frac{\partial V(z,t)}{\partial t}$$

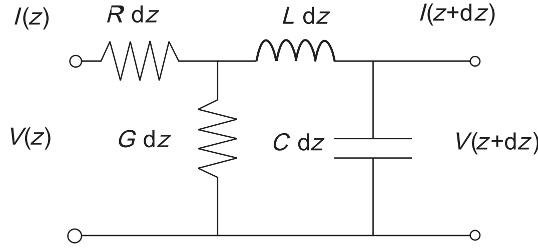

Figure 1.6 Incremental model of RLC distributed system

The above coupled equations are the transmission line equations for an RLC-transmission line. Figure 1.6 shows the RLC incremental model. Taking the partial derivative of the voltage distribution equation with respect to space

$$\frac{\partial}{\partial z}\left\{\frac{\partial V(z,t)}{\partial z}\right\} = \frac{\partial^2 V(z,t)}{\partial z^2} = -\frac{\partial}{\partial z}\left\{R(z)I(z,t) + L(z)\frac{\partial I(z,t)}{\partial t}\right\}$$

where

$$\frac{\partial^2 V(z,t)}{\partial z^2} = -R(z)\frac{\partial}{\partial z}\{I(z,t)\} - L(z)\frac{\partial^2 I(z,t)}{\partial z \partial t}$$

From the coupled equations, we can solve for second term by taking the partial derivative of current with respect to time,

$$\frac{\partial^2 I(z,t)}{\partial t \partial z} = -G(z)\frac{\partial V(z,t)}{\partial t} - C(z)\frac{\partial^2 V(z,t)}{\partial t^2}$$

Substituting into the voltage equation

$$\frac{\partial^2 V(z,t)}{\partial z^2} = R\left[GV(z,t) + C\frac{\partial V(z,t)}{\partial t}\right] + L\left[G\frac{\partial V(z,t)}{\partial t} + C\frac{\partial^2 V(z,t)}{\partial t^2}\right]$$

Grouping the common terms,

$$\frac{\partial^2 V(z,t)}{\partial z^2} - LC\frac{\partial^2 V(z,t)}{\partial t^2} - [RC + LG]\frac{\partial V(z,t)}{\partial t} - RGV(z,t) = 0$$

The above equation is the general expression for an increment where resistance, conductance, capacitance, and inductance are incorporated.

In this case the conductance is much small, and the RC product is much larger than LG, the special case reduces to

$$\frac{\partial^2 V(z,t)}{\partial z^2} - LC\frac{\partial^2 V(z,t)}{\partial t^2} - [RC]\frac{\partial V(z,t)}{\partial t} = 0$$

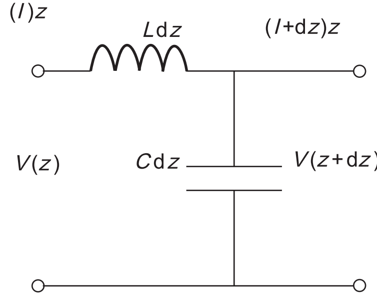

Figure 1.7 Incremental model of inductor-capacitor (LC) distributed system

In this case the conductance is small, but the *RC* product is much smaller than the *LG* product

$$\frac{\partial^2 V(z,t)}{\partial z^2} - LC\frac{\partial^2 V(z,t)}{\partial t^2} - [LG]\frac{\partial V(z,t)}{\partial t} = 0$$

In the case that the conductance and the resistance are small compared to the inductance and capacitance, this reduces to the elliptical equation, also known as the wave equation [62,64]

$$\frac{\partial^2 V(z,t)}{\partial z^2} - LC\frac{\partial^2 V(z,t)}{\partial t^2} = 0$$

Hence, when the resistive and conductance terms tend to zero, the voltage and current distribution follows the form of the wave equation. Figure 1.7 shows the incremental model for the LC network. The wave equation can be put in the form of a velocity times the time expressed as

$$\frac{\partial^2 V(z,t)}{\partial z^2} - \frac{\partial^2 V(z,t)}{\partial (v_{\mathrm{p}}t)^2} = 0$$

where phase velocity is defined as

$$v_{\mathrm{p}} = \frac{1}{\sqrt{LC}}$$

The characteristic impedance of a lossless transmission line is also related to the ratio of the inductance to the capacitance, expressed as

$$Z_0 = \sqrt{\frac{L}{C}}$$

From this analysis, the nature of the voltage and current distribution is a function of the assumptions of the inductance, capacitance, resistance, and conductance terms. From the two limiting cases, of small resistance and conductance terms, the equations will have the

form of a lossy transmission lines. Placing the last term on the RHS

$$\frac{\partial^2 V(z,t)}{\partial z^2} - LC\frac{\partial^2 V(z,t)}{\partial t^2} = [RC]\frac{\partial V(z,t)}{\partial t}$$

and

$$\frac{\partial^2 V(z,t)}{\partial z^2} - LC\frac{\partial^2 V(z,t)}{\partial t^2} = [LG]\frac{\partial V(z,t)}{\partial t}$$

This form is known as the damped wave equation [62,64,93–96].

Note when the term on the RHS is weak, the nature of the system still behaves as a transmission line with loss associated with the resistance and conductance. But when the LC time is small, the system reduces to the equation, which is dispersive in nature. From an ESD perspective, the RC distributed system, and RG distributed system limits are prevalent in both device and chip level response in most cases.

Substitution of the second coupled equation

$$\frac{\partial^2 V(z,t)}{\partial z^2} = -\frac{\partial R(z)}{\partial z}I(z,t) + R(z)C(z)\frac{\partial V(z,t)}{\partial t}$$

Assuming a constant coefficient for the resistance and capacitance, the voltage equation is reduced to a second order partial differential equation in space and time

$$\frac{\partial^2 V(z,t)}{\partial z^2} = RC\frac{\partial V(z,t)}{\partial t}$$

The second order partial differential equation is the parabolic (or diffusion) equation [62,64]. The parabolic equation is first order in time and second order in space. This is referred to as the voltage diffusion equation [64]. Hence, the characteristic time constant of the system is related to the local RC time of the increment. Assuming a step impulse from an ESD event, one can solve for the solution using a Laplace transformation operator L

$$L\left\{\frac{\partial^2 V(z,t)}{\partial z^2} - RC\frac{\partial V(z,t)}{\partial t}\right\} = 0$$

where

$$L\left\{\frac{\partial^2 V(z,t)}{\partial z^2}\right\} = \frac{\partial^2 V(z,s)}{\partial z^2}$$

$$L\left\{RC\frac{\partial V(z,t)}{\partial t}\right\} = RC\{sV(z,s) - V(z,t=0^+)\}$$

Substituting in the Laplace transformed terms into the voltage diffusion equation, the second-order partial differential equation in space and time is reduced to a second-order O[2] differential equation in the variable z,

$$\frac{\mathrm{d}^2 V(z,s)}{\mathrm{d}z^2} - s(RC)V(z,s) = -V(z,0^+)$$

For a second order ordinary differential equation, there are two solutions which can be expressed as a function of voltage coefficients

$$V(z,s) = V^{+} \exp\left\{-z\left(\sqrt{sRC}\right)\right\} + V^{-} \exp\left\{+z\left(\sqrt{sRC}\right)\right\}$$

In this analysis, one of the solutions will increase to infinity. As a result, we can assume that one of the two solutions is not physical. The solution that decays with distance is the physical solution. Assuming a step input voltage at the $V(z=0,t)$ equal to an initial voltage step $V_0\ u(t)$, and from the Laplace transform of a step function (e.g., $1/s$) the solution by inspection can be determined to be

$$V(z,s) = \frac{V_0}{s} \exp\left\{-z\left(\sqrt{sRC}\right)\right\}$$

Using the inverse Laplace transformation, the solution can be expressed as the complimentary error function

$$V(z,t) = V_0 u(t) \operatorname{erfc}\left\{\frac{1}{2}\sqrt{\frac{z^2}{(t/RC)}}\right\}$$

From the current–voltage relationships, solving for the current and taking the partial derivative with respect to position

$$I(z,t) = -\frac{1}{R}\frac{\partial V(z,t)}{\partial z} = -\frac{1}{R}\frac{\partial}{\partial z}\left[V_0 u(t) \operatorname{erfc}\left\{\frac{1}{2}\sqrt{\frac{(RC)z^2}{t}}\right\}\right]$$

Taking the derivative

$$I(z,t) = \frac{V_0}{R}\sqrt{\left(\frac{RC}{\pi t}\right)} u(t) \exp\left[-\frac{z^2}{4(t/RC)}\right]$$

An analogy can be established to semiconductor carrier diffusion or heat diffusion, where there exists a characteristic diffusion length, and diffusivity coefficient for the RC network. This is related to the argument within the error function (and the exponential term). From the above solution, the current decreases according to the product of the inverse of time and an exponential function related to the square of the distance. The magnitude of the exponential term is a function of the ratio of the characteristic time relative to the RC time of the network.

In the distributed RC network, the voltage and current distribution is a function of the time, position, and the characteristic resistance and capacitance of the network. Hence, the spatial and temporal distribution of the voltage and current is a function of the characteristic time constant, *RC*, and the time scale, *t*. In the understanding of current and voltage distribution within an ESD device, or the distribution within a chip, the ratio of the characteristic time to the product of the resistance and capacitance (e.g., RC time constant) is a key ESD design criteria.

1.6.5 Resistor–Capacitor (RC) Distributed Systems

Resistance and capacitance play a fundamental effect on the voltage and current distribution during ESD events. Typically, inductive effects can be ignored when evaluating the voltage and current distribution on a semiconductor chip. Hence, the understanding of lumped and distributed resistance–capacitor systems is fundamental in ESD events. The resistance and capacitance can be observed locally within a semiconductor device, a circuit or globally on a chip level. Even in small devices, metal bussing plays a role in the resistance within the device where metal line widths are small. For example, an ESD diode element can be represented as a anode metal bus with a given resistance per unit micron. Additionally, the diode element can be represented as a capacitor element.

On a semiconductor chip level, although the metal bus widths are large, the distances of interest are on the scale of the semiconductor chip, or distance between input nodes, and power pads. In this case, the wide bus resistance per unit length and the capacitance form a resistance–capacitor (RC) transmission line which can influence the voltage and current distribution during ESD events. As a result, the resistance and the capacitance play a key role from the local response of a single device, to the global response of chip architecture during an ESD event.

The incremental variation plays a role in the voltage and current response during high-current ESD operation. To analyze the incremental variation from point z to a second point $(z + \mathrm{d}z)$, assume a resistance term $R(z)\ \mathrm{d}z$ where $R(z)$ is the resistance per unit length over increment $\mathrm{d}z$. Between the top surface and bottom surface of the transmission line, a capacitor per unit distance $C(z)\ \mathrm{d}z$. Forming a two-port network where the input current is $I(z, t)$, and input voltage $V(z, t)$ at input port z, and the output current $I(z + \mathrm{d}z, t)$ and output voltage $V(z + \mathrm{d}z, t)$ a coupled set of equation can be formed with differential voltage can be represented as the voltage potential difference across resistance $R(z)\ \mathrm{d}z$ [64]

$$\mathrm{d}V(z,t) = -I(z,t)[R(z)\mathrm{d}z]$$

and the differential current can be represented as the charge across the capacitor $C(z)$ during increment of time $\mathrm{d}t$

$$\mathrm{d}I(z,t) = [C(z)\mathrm{d}z]V(z,t)\mathrm{d}t$$

This can be expressed as a set of coupled differential equations as

$$\frac{\partial V(z,t)}{\partial z} = -R(z)I(z,t)$$
$$\frac{\partial I(z,t)}{\partial z} = -C(z)\frac{\partial V(z,t)}{\partial t}$$

The above coupled equations are the transmission line equations for an RC-transmission line.

Taking the partial derivative of the voltage distribution equation with respect to space,

$$\frac{\partial}{\partial z}\left\{\frac{\partial V(z,t)}{\partial z}\right\} = \frac{\partial^2 V(z,t)}{\partial z^2} = -\frac{\partial}{\partial z}\{R(z)I(z,t)\}$$
$$\frac{\partial^2 V(z,t)}{\partial z^2} = -\frac{\partial}{\partial z}\{R(z)I(z,t)\} = -\frac{\partial R(z)}{\partial z}I(z,t) - R(z)\frac{\partial}{\partial z}\{I(z,t)\}$$

Substitution of the second coupled equation

$$\frac{\partial^2 V(z,t)}{\partial z^2} = -\frac{\partial R(z)}{\partial z} I(z,t) + R(z)C(z)\frac{\partial V(z,t)}{\partial t}$$

Assuming a constant coefficient for the resistance and capacitance, the voltage equation is reduced to a second-order partial differential equation in space and time

$$\frac{\partial^2 V(z,t)}{\partial z^2} = RC\frac{\partial V(z,t)}{\partial t}$$

The second order partial differential equation is the parabolic (or diffusion) equation [62,64]. The parabolic equation is first order in time and second order in space. This is referred to as the voltage diffusion equation [64]. Hence, the characteristic time constant of the system is related to the local RC time of the increment.

Assuming a step impulse from an ESD event, one can solve for the solution using a Laplace transformation operator L

$$L\left\{\frac{\partial^2 V(z,t)}{\partial z^2} - RC\frac{\partial V(z,t)}{\partial t}\right\} = 0$$

where

$$L\left\{\frac{\partial^2 V(z,t)}{\partial z^2}\right\} = \frac{\partial^2 V(z,s)}{\partial z^2}$$

$$L\left\{RC\frac{\partial V(z,t)}{\partial t}\right\} = RC\{sV(z,s) - V(z,t=0^+)\}$$

Substituting in the Laplace transformed terms into the voltage diffusion equation, the second-order partial differential equation in space and time is reduced to a second-order differential equation in the variable z

$$\frac{\mathrm{d}^2 V(z,s)}{\mathrm{d}z^2} - s(RC)V(z,s) = -V(z,0^+)$$

For a second-order ordinary differential equation, there are two solutions which can be expressed as a function of a voltage coefficients

$$V(z,s) = V^+ \exp\left\{-z\left(\sqrt{sRC}\right)\right\} + V^- \exp\left\{+z\left(\sqrt{sRC}\right)\right\}$$

In this analysis, one of the solutions will increase to infinity. As a result, we can assume one of the two solutions is not physical. The solution that decays with distance is the physical solution. Assuming a step input voltage at the $V(z=0,t)$ equal to an initial voltage step $V_0\, u(t)$, and from the Laplace transform of a step function (e.g., $1/s$) the solution by inspection can be determined to be

$$V(z,s) = \frac{V_0}{s}\exp\left\{-z\left(\sqrt{sRC}\right)\right\}$$

Using the inverse Laplace transformation, the solution can be expressed as the complementary error function [64]

$$V(z,t) = V_0 u(t)\mathrm{erfc}\left\{\frac{1}{2}\sqrt{\frac{z^2}{(t/RC)}}\right\}$$

From the current–voltage relationships, we can also solve for the current and taking the partial derivative with respect to position

$$I(z,t) = -\frac{1}{R}\frac{\partial V(z,t)}{\partial z} = -\frac{1}{R}\frac{\partial}{\partial z}\left[V_0 u(t)\mathrm{erfc}\left\{\frac{1}{2}\sqrt{\frac{(RC)z^2}{t}}\right\}\right]$$

Taking the derivative, we have

$$I(z,t) = \frac{V_0}{R}\sqrt{\left(\frac{RC}{\pi t}\right)}u(t)\exp\left[-\frac{z^2}{4(t/RC)}\right]$$

An analogy can be established to semiconductor carrier diffusion or heat diffusion, where there exists a characteristic diffusion length and diffusivity coefficient for the RC network. This is related to the argument within the error function (and the exponential term). From the above solution, the current decreases according to the product of the inverse of time and an exponential function related to the square of the distance. The magnitude of the exponential term is a function of the ratio of the characteristic time relative to the RC time of the network.

In the distributed RC network, the voltage and current distribution is a function of the time, position, and the characteristic resistance and capacitance of the network (Figure 1.8). Hence, the spatial and temporal distribution of the voltage and current is a function of the characteristic time constant, *RC*, and the time scale, *t*. In the understanding of current and voltage distribution within an ESD device, or the distribution within a chip, the ratio of the characteristic time to the product of the resistance and capacitance (e.g., RC time constant) is a key ESD design criteria.

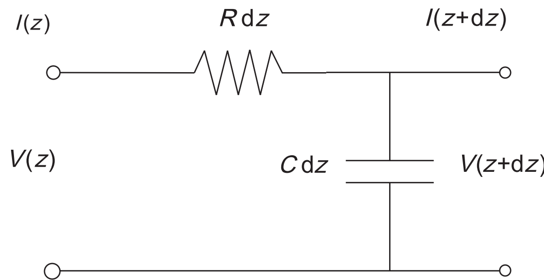

Figure 1.8 Incremental model for resistor–capacitor (RC) distributed system

1.6.6 Resistor–Conductance (RG) Distributed Systems

Resistance is the most important parameter in ESD events. The role of resistance is critical in the voltage and current distribution within a semiconductor device, circuit, or network. The understanding of resistance and resistance distribution plays a more significant role compared to inductance and capacitance issues. Typically, inductance plays an important role in the effect of lead frames and packages on the ESD response, but play a minor role in the understanding of ESD devices and circuit response. Capacitance plays a role when the RC time of the wiring is of the order of the characteristic time of the event. Hence, the understanding of lumped and distributed resistance systems is fundamental in ESD events. Resistance plays a key role from the local current distribution within a diode structure, a MOSFET structure, off-chip driver circuits, to global current distribution in the metal busses, and the chip substrate.

The incremental variation plays a role in the voltage and current response during high-current ESD operation in the resistive network. To analyze the incremental variation from point z to a second point $(z + \mathrm{d}z)$, assume a resistance term $R(z)$ dz where $R(z)$ is the resistance per unit length over increment dz (Figure 1.9). Between the top and bottom surface of the transmission line, a conductance per unit distance $G(z)$ dz. Forming a two-port network where the input current is $I(z, t)$ and input voltage $V(z, t)$ at input port z, and the output current $I(z + \mathrm{d}z, t)$ and output voltage $V(z + \mathrm{d}z, t)$, a coupled set of equation can be formed with differential voltage represented as the voltage potential difference across resistance $R(z)$ dz

$$\mathrm{d}V(z, t) = -I(z, t)[R(z)\mathrm{d}z]$$

and the differential current loss can be represented as the differential current through a conductance term $G(z)$

$$\mathrm{d}I(z, t) = -[G(z)\mathrm{d}z]V(z, t)$$

This can be expressed as a set of coupled differential equations as

$$\frac{\partial V(z, t)}{\partial z} = -R(z)I(z, t)$$
$$\frac{\partial I(z, t)}{\partial z} = -G(z)V(z, t)$$

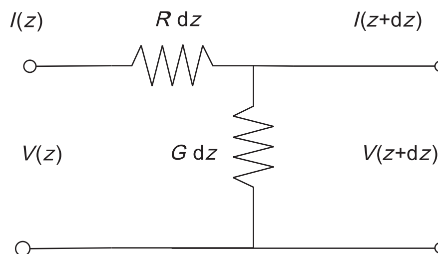

Figure 1.9 Incremental model for the resistor–conductance (RG) distributed model

The above coupled equations are the transmission line equations for an RG-transmission line, where the inductance and capacitance are assumed negligible. Taking the partial derivative of the voltage distribution equation with respect to space

$$\frac{\partial}{\partial z}\left\{\frac{\partial V(z,t)}{\partial z}\right\} = \frac{\partial^2 V(z,t)}{\partial z^2} = -\frac{\partial}{\partial z}\{R(z)I(z,t)\}$$

$$\frac{\partial^2 V(z,t)}{\partial z^2} = -\frac{\partial}{\partial z}\{R(z)I(z,t)\} = -\frac{\partial R(z)}{\partial z}I(z,t) - R(z)\frac{\partial}{\partial z}\{I(z,t)\}$$

Substitution of the second coupled equation

$$\frac{\partial^2 V(z,t)}{\partial z^2} = -\frac{\partial R(z)}{\partial z}I(z,t) + R(z)G(z)V(z,t)$$

Assuming a constant coefficient for the resistance and conductance, the voltage equation is reduced to a second-order partial differential equation in space and time

$$\frac{\partial^2 V(z,t)}{\partial z^2} = R(z)G(z)V(z,t)$$

or expressed in the form

$$\frac{\partial^2 V(z,t)}{\partial z^2} - R(z)G(z)V(z,t) = 0$$

or as an ordinary differential equation

$$\left[\frac{\mathrm{d}^2}{\mathrm{d}z^2} - R(z)G(z)\right]V(z,t) = 0$$

For a second-order ordinary differential equation, there are two solutions which can be expressed as a function of voltage coefficients [64]

$$V(z,t) = V(t)^{+}\exp\left\{-z\left(\sqrt{RG}\right)\right\} + V(t)^{-}\exp\left\{+z\left(\sqrt{RG}\right)\right\}$$

In this analysis, one of the solutions will increase to infinity. As a result, we can assume one of the two solutions is not physical. The solution that decays with distance is the physical solution.

$$V(z,t) = V_0(t)\exp\left\{-z\left(\sqrt{RG}\right)\right\}$$

From the current–voltage relationships, we can also solve for the current and taking the partial derivative with respect to position,

$$I(z,t) = -\frac{1}{R}\frac{\partial V(z,t)}{\partial z} = -\frac{1}{R}\frac{\partial}{\partial z}\left[V_0 u(t)\exp\left\{-z\sqrt{RG}\right\}\right]$$

hence the current can be expressed as

$$I(z,t) = V_0 u(t)\sqrt{RG}\exp\left\{-z\sqrt{RG}\right\}$$

In the analysis of the RG ladder network, as the current and voltage extends down the network, the voltage decreases in an exponential fashion according to the spatial parameter of the arithmetic mean of the incremental resistance and the incremental conductance. As the resistance or the conductance increases, the voltage decay along the transmission line increases. Also note that as the resistance and conductance tend to zero, the voltage approaches a constant value and the current tends to zero.

1.7 ESD METRICS AND FIGURES OF MERIT

ESD metrics and ESD figures of merit (FOM) can be established to provide a means of quantifying and benchmark, the value of the ESD protection strategy. ESD metrics and FOM can be established on a system, chip, circuit, and device level to address the macro-level and micro-level effectiveness of the ESD protection methodology and strategy.

On a chip level, there are measures that provide value add meaning in the quantification of the ESD chip strategy for the given chip design in the semiconductor process. Useful chip-level ESD metrics include the following:

- Chip mean pin power-to-failure.
- Chip pin standard deviation power-to-failure.
- Chip mean pin power-to-failure to ESD specification margin.
- Worst case pin to specification ESD margin.
- Total ESD area to total chip area ratio.

1.7.1 Chip Level ESD Metrics

1.7.1.1 Chip mean pin power-to-failure

Chip mean pin power-to-failure is the mean of the pin power-to-failure distribution within a semiconductor chip. Within a semiconductor chip, the power-to-failure is a function of the semiconductor process, the peripheral circuit library, the ESD input protection networks, and the power grids. The variation within a semiconductor chip is a function of the types of circuits, and types of ESD elements used. The pin-to-pin variation of an identical pin can be associated with semiconductor process variations within a given chip (e.g., photolithography, etch, and film thickness variations), the power bussing, the ESD power clamp placement, and other design-related features. The chip mean power-to-failure is the average peak value where the distribution is centered.

1.7.1.2 Chip pin standard deviation power-to-Failure

The chip pin standard deviation power-to-failure is the standard deviation associated with the pin power-to-failure distribution across a given chip. As stated above, the variation within a semiconductor chip is a function of the types of circuits and types of ESD elements used. The pin-to-pin variation of an identical pin can be associated with semiconductor process variations within a given chip (e.g., photolithography, etch, and film thickness variations), the power bussing, the ESD power clamp placement, and other design-related features. The standard deviation is also influenced in the variety of different size I/O networks that are contained within the chip. The ESD metric can be referenced as the power-to-failure or the variation in the ESD robustness for a given device model (e.g., human body model, machine model).

1.7.1.3 Chip mean pin power-to-failure to ESD specification margin

Chip mean pin power-to-failure (ESD) to power-to-failure (ESD) specification margin is the margin between the actual mean of the power-to-failure pin distribution within a semiconductor chip and the product specification. The importance of this ESD metric is by evaluating the margin of the mean relative to the specification, an understanding of the effectiveness of the ESD design strategy as well as the robustness of the technology can be evaluated. As the ESD robustness of a process technology improves, the mean chip power-to-failure distribution will increase (e.g., for a given fixed ESD design strategy). Additionally, when a better ESD network is utilized, the ESD failure distribution will shift relative to the specification (e.g., for a given fixed semiconductor process technology). This ESD metric is important to evaluate the ESD robustness of a technology, and the effectiveness of the ESD network to protect the circuits within the technology.

1.7.1.4 Worst-case pin power-to-failure to specification ESD margin

The worst-case pin power-to-failure to specification ESD margin is a measure of the difference between the worst-case pin in the ESD pin distribution relative to the defined ESD specification. In the case of the worst-case pin, this may be a function of a given circuit, or can be associated with the standard deviation, and the mean chip power-to-failure. In the case that the difference between the mean chip power-to-failure and the power-to-failure specification level is small, and the pin power-to-failure standard deviation level is also wide, then the worst-case pin power-to-failure may be on the power-to-failure distribution "tail." In this case, the ESD protection strategy or the semiconductor process must be altered to establish an increase in the margin between the worst-case pin and the ESD specification level.

In many cases, the worst-case pin failure may be associated with different peripheral circuits, and are not contained within the Gaussian or normal distribution of pin failures. For example, receiver networks may not be contained within the I/O OCD failure distribution, but may represent its own power-to-failure distribution (e.g., and may contain a different failure mechanism). In this case, it is not always clear that the changes in the semiconductor process will lead to shift in the margin between the ESD specification and the worst-case pin

failure level. In the case that it will track with the semiconductor process or ESD network, improving the mean power-to-failure distribution will lead to an increase in the margin between the worst-case pin and the ESD specification.

1.7.1.5 Total ESD area to total chip area ratio

An ESD metric of interest is the ratio of the total area utilized for ESD networks to the total chip area. This is a valuable metric for floor planning a design where the area on the chips are budgeted according to different functional objectives. For example, the peripheral circuit budget may be driven by Rents' Rule which relates the number of I/O relative to the number of logic gates. The area of a given I/O cell may be budgeted based on the number of I/O, and the desired ratio of the core logic relative to the peripheral I/O budget. In this floor planning metric, the amount of area for ESD protection may be budgeted to avoid utilization of excess design space.

$$\frac{(\mathrm{A_{ESD}})_T}{A_{\mathrm{Chip}}}$$

1.7.1.6 ESD area to I/O area ratio

A common ESD metric used in semiconductor chip floor planning is on the acceptable level of area of an I/O book utilized for ESD protection.

$$\frac{(A_{\mathrm{ESD}})}{A_{\mathrm{I/O}}}$$

In the floor planning of a microprocessor, or an ASIC design, the area dedicated to I/O is planned to be a certain percent area. In ESD design practice, the percentage of the I/O book dedicated to the ESD protection is budgeted according to the above metric. In the past, the acceptable ratio ranged from 0.2 to 0.3.

1.7.2 Circuit Level ESD Metrics

The metrics for a given circuit are focused on both the performance degradation imposed with the addition of the ESD structure as well as the area consumption. Additionally, for circuits, the relationship between the ESD robustness of the circuit and the capacitance loading ratio is also a crucial ESD metric or FOM. Hence circuit-level ESD metrics are as follows:

- Circuit ESD protection level to ESD loading effect.
- Circuit performance to ESD loading effect.
- ESD area to total circuit area ratio.
- Circuit ESD level to specification margin.

1.7.2.1 Circuit ESD protection level to ESD loading effect

To evaluate the ESD protection level to the loading effect, the protection level is compared to the loading effect penalty. For example, given the loading effect is capacitive in nature, a circuit level ESD FOM can be represented as

$$(\mathrm{FOM})_{\mathrm{Ckt}} = \frac{V_{\mathrm{ESD}}}{C_{\mathrm{ESD}}}$$

where the circuit level FOM is the ratio of the ESD voltage of failure to the capacitance of the ESD network. For example, the ESD voltage can be the HBM failure voltage. This provides a measure of the protection value add for the amount of capacitance added to the circuit.

1.7.2.2 Circuit performance to ESD loading effect

An important metric from a circuit designer's perspective is the effect of the capacitance loading effect on the performance of a circuit. Hence, an ESD metric that quantifies the loading effect as a percent decrease in the performance is of value to quantify the ESD impact on the circuit performance. This is achievable by the ratio of the difference of the ‘‘unloaded’’ circuit performance minus the ‘‘ESD loaded’’ circuit performance in the numerator and the ‘‘unloaded’’ circuit performance in the denominator.

$$\frac{P(\mathrm{w/o\,ESD}) - P(\mathrm{with\,ESD})}{P(\mathrm{w/o\,ESD})}$$

In the past, the ESD loading effect was a minimal effect on the circuit performance. With technology scaling, the implications of the ESD loading effect has become more significant.

1.7.2.3 ESD area to total circuit area ratio

As in the total chip case, the budgeting of the area to functional utilization relative to the ESD protection is important for the understanding of the difficulty to ESD protect a given network and will determine its capability as the circuit is scaled

$$\frac{A_{\mathrm{ESD}}}{A_{\mathrm{Ckt}}}$$

For example, in microprocessors in a 0.5-μm technology generation, the area ratio should be below 0.05 (5% area) for the ESD protection network.

1.7.2.4 Circuit ESD level to specification margin

A valuable ESD metric is the ESD margin between the circuit failure level and the specification. This provides an understanding of the ESD benchmarking of the given circuit

in the technology and for that given circuit generation. As the circuit is scaled, or the technology is scaled, the understanding of how the circuit performs relative to the specification is critical to evaluate its future performance.

1.7.3 Device ESD Metric

ESD metrics of ESD devices can provide an insight in the value add of a given protection network. ESD metrics and figures of merit determine how much of the capability an ESD network can provide for a given design or ESD circuit type. The following metrics are used to evaluate the ESD design effectiveness:

- ESD area percentage utilization factor.
- ESD robustness to ESD loading effect ratio.
- Power-to-failure to maximum power condition.

1.7.3.1 ESD area percentage utilization factor

This metric is a measure of the area efficiency of an ESD element. For a given width, W, and length L, a maximum area to minimum area factor can be defined, where the numerator is a maximum function, and the denominator is a minimum function for a geometry factor of

$$\frac{\mathrm{Max}\{W, L\}}{\mathrm{Min}\{W, L\}}$$

This FOM can be used to evaluate area utilization and the efficiency of the area utilization of ESD protection.

1.7.3.2 ESD robustness to ESD loading effect ratio

On the ESD device level, the FOM for the ability to achieve a high-ESD robustness of a device of a given width and length, compared to the loading effect, is important for evaluation of the ESD device efficiency for achieving certain ESD levels for a given loading capacitance (e.g., impedance). This can be expressed as

$$(\mathrm{FOM})_{\mathrm{ESD}} = \frac{V_{\mathrm{ESD}}\{W, L\}}{C_{\mathrm{ESD}}\{W, L\}}$$

1.7.3.3 Power-to-failure to maximum power condition

An ESD FOM is the maximum power-to-failure compared to the maximum functional power that a structure can maintain. For a given semiconductor device, the power-to-failure can be determined from the Wunsch–Bell model. The maximum power of a semiconductor device,

such as a bipolar transistor, can be obtained from the Johnson Limit relationship. Hence, the ratio of the power-to-failure to the maximum power can be compared. This ratio forms a dimensional group relating the power-to-failure to the maximum functional power

$$\frac{P_{\mathrm{f}}}{P_{\mathrm{Max}}}$$

1.7.4 ESD Quality and Reliability Business Metrics

In establishing an ESD strategy, quality, and reliability, ESD metrics can be established for measuring the success of the ESD implementation and strategy. Different corporations will have individual needs whose ESD metrics may differ according to the business quality model, business reliability objectives, or the state of the ESD strategy at a given time in the business strategy. The following are a few ESD business metrics utilized to measure the success of a corporate strategy:

- Percentage of products above an ESD specification level (e.g., HBM specification of 2 or 4 kV).
- Percentage of products above a given ESD specification on first design pass.
- ESD plateau level (e.g., ESD protection mean level for all products vs. time).
- ESD product learning rate (e.g., for HBM specification, kV/year).
- Dollars Lost versus ESD protection level.
- Yield loss versus ESD protection level.

The first ESD metric measures the ability to maintain a technology or number of technologies above a given ESD specification level. This is a measure of success at some point in the design release process.

The second ESD metric is a measure of the ability of ESD design success on first design pass. This ESD metric may be a measure of good ESD protection devices, good ESD design manuals, good ESD checking and verification, and robust circuits. This may be a demonstration of circuit designer training in ESD work and ESD design discipline.

The ESD protection plateau level is an ESD metric which may be a measure of the baseline of success of the ESD designs, technology robustness, and the ESD designer. The stability to a given ESD baseline may be a measure of the manufacturing control and ESD design discipline. The level of the ESD protection plateau may also be a measure that no ESD learning is in process and ESD design conservatism.

The ESD product learning rate can be a powerful metric in understanding the success of ESD semiconductor technology transitions, semiconductor scaling trends and a measure of success of new ESD implementations. In practice, over a number of years, the ESD trend can be evaluated to project either MOSFET scaling trends or implementation success. For example, a learning rate of 2 kV/year (HBM) from a 2 kV HBM ESD baseline by introducing semiconductor process changes, followed by ESD design layout improvements, followed again by OCD resistor ballasting, and finally adding RC-triggered ESD power clamps.

Another form of ESD metrics can be evaluated based on semiconductor manufacturing product losses, and losses as a function of ESD protection levels. For example, this can be measured as a function of dollar or yield loss in time or plotted as a function of the ESD protection level. These are a measure of the ESD control program, handling procedures, and the margin between the ESD sensitivity of the tooling and handling relative to the ESD product sensitivity.

1.8 TWELVE STEPS TO BUILDING AN ESD STRATEGY

In the practical implementation of an ESD program, there are a number of steps to be taken in delivering ESD sensitive parts successfully. In ESD program management, T. Dangelmeyer noted twelve ''critical factors'' for building an ESD strategy from the product to the customer [100]. These are as follows:

- Effective implementation plan.
- Management commitment.
- A full-time coordinator.
- An active ESD committee.
- Realistic requirements.
- ESD training for measureable goals.
- Auditing using scientific measures.
- ESD test facilities.
- A communication program.
- Systematic planning.
- Human factor engineering.
- Continuous improvement.

The focus of this program is the management of a facility and corporation in managing its staff, tooling, and establishing corporate objectives.

To address the ESD design phase alone, there are also a number of critical steps that need to be taken. In order to achieve a good ESD design and release strategy, these 12 steps must be taken in order to insure consistent and acceptable ESD protection levels in a business that releases components which are sensitive to ESD [101]. The following are 12 steps needed to insure an establishment of an ESD strategy:

1. ESD device and circuits strategy.
2. ESD test site methodology.
3. ESD test equipment and testing methodology [102,103].
4. ESD device and circuit simulation strategy.

5. ESD computer aided design (CAD) design implementation.
6. ESD CAD design rule checking (DRC) tools.
7. ESD CAD design verification tools.
8. ESD design engagement, review, and release process.
9. ESD qualification process [102,103].
10. ESD metrics of devices, circuits, products, technologies, and learning.
11. ESD specifications, targets, and corporate objectives.
12. ESD technology benchmarking, scaling, and continuous learning strategy.

The means at which one carries out these ESD 12 steps can strongly influence the success or failure of a successful ESD design and release process.

1.9 SUMMARY AND CLOSING COMMENTS

In this chapter, an ESD floor plan was established for the rest of the textbook. The chapter introduced a very brief history of electrostatics, the ESD field, and key inventions and patents that will be discussed. This history, topics, and patents will be referred to in the future chapters. The chapter then lays out ESD failure mechanisms on the semiconductor device level, and circuit level, as well as chip level; this forces the reader to start thinking about the nature of failure mechanisms and will be a blueprint for the future discussion. The reader is then exposed to a new way of thinking about ESD. How the ESD design practice is unique? What are the concepts? As the book unfolds, this blueprint of ESD concepts will be apparent through the examples. The chapter then introduced time concepts weaving together the electromagnetic time constants, thermal time constants, ESD pulse time constants, and those of devices, circuits, and systems; this gets the reader thinking in a time domain and what phenomena is important for a given ESD pulse event. The chapter then focused on the concept of resistance, capacitance, and inductance, and how things distribute in space and time; this opens the concept of analysis—whether lumped or distributed, and the physical efficiency of the structures, circuits, and systems. Then the question of analysis—how do we simplify the thinking to a simple circuit and current loop? . . .and how will that scale ? We closed the chapter getting the reader to then reduce the thoughts to simple ESD metrics that will be handy for thinking, quantifying, and analyzing. Now the reader is prepared with an ESD mindset to read the rest of the text. Once you have mastered the ESD thinking of Chapter 1, the rest is commentary; the reader is now prepared to start sinking into the details, specifics, and examples.

In Chapter 2, we take a step backwards, and start getting into the practical details; the semiconductor chip ESD architecture is discussed. ESD is both an electrical as well as spatial phenomenon, and hence the architecture and synthesis must reflect both issues. The spatial and electrical connectivity is addressed and how this influences the design and synthesis of ESD networks and floor planning of semiconductor chips.

PROBLEMS

1.1. Show the time constant hierarchy of the physical time constants on a time axis, for the ESD pulse waveform time constants, MOSFET transit time, bipolar transistor unity current gain cutoff frequency, bipolar transistor unity power gain cutoff frequency, MOSFET circuit gate delay, cross-chip chip interconnect delay time, and package LC time constant.

1.2. Derive the ratio of the human body model and machine model peak current.

1.3. Derive the ratio of the machine model (MM) and the cassette model peak current. Assuming a 200 pF capacitor for the machine model, and a 10 pF capacitor for the cassette model. In both cases, assume a 10 Ω resistor in series with the capacitor source.

1.4. Derive a relationship between the total energy for a transmission line pulse (TLP) and a very fast-transmission line pulse (VF-TLP), where assume for the TLP trapezoidal waveform a 10 ns rise and fall time, and a 100 ns pulse width, and for the VF-TLP trapezoidal waveform a 1 ns rise and fall time, with a 5 ns pulse width.

1.5. Calculate the total capacitance and total energy stored in a charged coaxial cable of unit capacitance C per unit length. Assume a typical coaxial cable capacitance, and calculate the total capacitance for a 1, 10, and 100 foot cable. Assuming an initial charging of voltage V, calculate the total charge for the different length cables.

1.6. For the coaxial cables in Problem 5, assume an initial charging of 100 V, and 1000 V. Assuming a discharge of the cable into a system, calculate the peak current assuming discharging into a 500 Ω resistor.

1.7. Assuming a 100 foot coaxial cable of capacitance C, convert the coaxial cable waveform into a single capacitor element. What is the source capacitance?

1.8. Given the ladder network in Chapter 1, derive the relationship for the Stieljes continued fraction form for the output impedance term z_{22} (s).

1.9. Given the ladder network in Chapter 1, derive the relationship for the impedance parameters z_{12} (s) and $z_{21}(s)$.

1.10. Given an ESD diode in the reverse bias mode, we can assume the top electrode has a high resistance and the lower electrode has zero resistance. We can also represent the reverse biased diode as a capacitor element. Assume a ladder network consisting of N resistors on the top electrode, and N capacitors as the rungs of the ladder network, derive the impedance matrix terms.

1.11. Given an ESD diode in a forward bias mode, we can assume the top electrode has a high resistance and the lower electrode has zero resistance. We can represent the forward biased diode as a conductance term. Assume a ladder network consisting of N resistors on the top electrode, and N conductance terms for the rungs, derive the impedance matrix terms.

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2 Design Synthesis

2.1 SYNTHESIS AND ARCHITECTURE OF A SEMICONDUCTOR CHIP FOR ESD PROTECTION

In on-chip electrostatic discharge (ESD) circuit design, the design architecture and synthesis is critical in achieving ESD robustness. This chapter will briefly address the fundamental of the physical elements in ESD design. In ESD design, there are fundamental elements needed in the chip design synthesis to establish an alternative current loop to prevent the ESD current from causing chip or system damage. In ESD design, the fundamental elements in the design synthesis are the following:

- ESD input protection networks
- ESD power clamps networks
- ESD rail-to-rail networks
- Guard rings

In ESD design, the ESD robustness of the system will be a function of the following:

- Placement
- Physical size
- Triggering conditions
- Inherent robustness of the ESD circuitry
- Inherent robustness of the circuits that require protection

Figure 2.1 shows an example of an ESD input circuit, power rails, and an ESD power clamp network. The high-level schematic highlights the electrical connectivity between the

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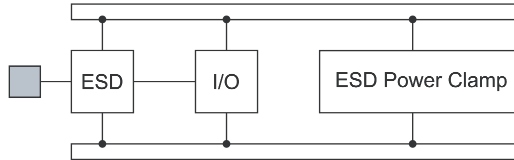

Figure 2.1 High-level electrical schematic highlighting the electrical connectivity between the pad, ESD network, power rails, and the ESD power clamp

pad and both power rails. Additionally, the ESD power clamp also establishes electrical connections to both power rails.

2.2 ELECTRICAL AND SPATIAL CONNECTIVITY

In an ESD design, the inter-relation of the elements in the system is key in achieving ESD robustness. The inter-relationship and interaction of the physical elements in the system can be dependent on both electrical connectivity and spatial connectivity. The electrical connectivity between a first electrical node and a second electrical node in the system will influence the ESD robustness of a design, chip, or system. The spatial connectivity between a first spatial point and a second spatial point can also influence the ESD robustness of a semiconductor chip. Depending on the ESD mechanism, the issue of the spatial relationship is not always critical.

2.2.1 Electrical Connectivity

Electrical connectivity is an important concept in ESD design. It is critical to establish a design architecture that allows electrical connectivity between external pins and power rails, and power rails to power rails. To establish good ESD robustness, current must be able to flow from external pins connections to power rails. Hence, a current path must exists which allows between all physical external node (e.g., input/output circuits, peripheral circuits). A power boundary condition can be stated that states that the flow of current must be able to flow from any node which connects to outside the system to any second node (e.g., a second input pin, or power rail) within the physical system. A second condition is that current must be able to flow from one power rail to a second power rail. In order to achieve this, electrical connectivity must exist between a first and second power rail, where the first and second rail do not have to be at the same bias condition.

In order to provide ESD protection, a Kirchoff current loop can be established between the first node and the grounded reference power supply. The input source serves as part of the Kirchoff current loop from the ground, through the source element, the electrical switch, and the input node of the device under test (DUT). The Kirchoff current loop continues to the grounded reference and back to the ground plane. In the case of power supply to power supply, the Kirchoff current loop does not contain the input pin but from a first power supply to second power supply.

2.2.2 Thermal Connectivity

Thermal connectivity, analogous to the electrical connectivity, also plays a role in ESD protection in a system. A thermal circuit contains thermal components and thermal nodal points. The thermal network can be associated with a point in the circuit or spatial location. There are temperature values associated with the thermal nodal points. Through the substrate region, components interact through thermal coupling. In the thermal equivalent circuit, the thermal coupling can be represented as thermal transfer resistance terms and thermal feedback phenomenon. Thermal interaction between adjacent structures can play a role in current and voltage distribution.

2.2.3 Spatial Connectivity

Spatial connectivity also plays a role in ESD protection. The primary reason for issues of a spatial nature is ESD phenomena which is interactive through the silicon substrate [1]. Through the substrate, both electrical and thermal physical phenomena exist. From an electrical perspective, there is inductive and capacitive coupling, as well as minority carrier injection phenomena. There are also initial conditions where uniform charge exists in the substrate prior to electrical discharge. For example, in the charge device model (CDM) test, the substrate is charged across the entire substrate region. The spatial relationship between input pads, peripheral circuits (e.g., off-chip drivers (OCD), receivers, transmitters), wire interconnects, ESD input circuit networks, ESD power clamps, and busses can play a critical role in the ESD response of a network (Figure 2.1). When addressing the spatial dependence, the physical time constants of the system are critical in the understanding of the semiconductor circuit response. These can include the charge relaxation time, the carrier diffusion time, and the circuit time constant response of the network involved in the CDM event. Figure 2.2 denotes the interaction of the electrical, thermal, and spatial connectivity.

2.3 ESD, LATCHUP, AND NOISE

ESD protection, latchup, and noise are all influenced by the electrical, thermal, and spatial connectivity in a chip or system. Providing good electrical connectivity between segments of

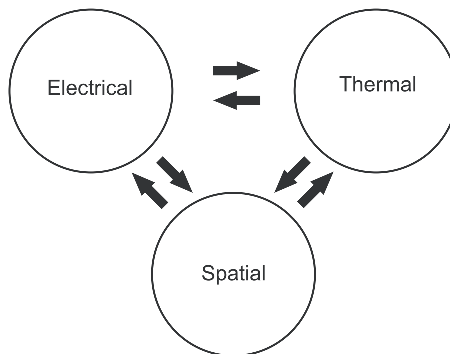

Figure 2.2 Electrical, thermal, and spatial connectivity

a chip or a system can provide improved ESD protection, but at the same time introduce noise concerns. Consequently, providing good noise isolation can lead to poor ESD protection; this does not have to be true. Choosing the right design choices in the synthesis of the design segments, circuit set, and the ESD protection type can allow for achieving both good noise isolation as well as good ESD robustness.

ESD, latchup, and noise are also dependent on the process technology and the substrate region. The choice of the *n*-well, *p*-well, triple-well, and substrate doping concentrations have a strong influence on all three issues. Typically, higher well doses can lead to lower parasitic bipolar current gain in parasitic transistor elements. This also reduces the noise injection into the substrate region. When using diode-based ESD solutions, it was shown that higher well doses lead to improved ESD diode performance [1]. On the other hand, using MOSFET-based ESD protection leads to a lowering of the MOSFET second breakdown with higher well doses [1]. In the case of the substrate doping concentration, lower substrate doping concentration improves noise isolation. At the same time, the minority carrier lifetime in the substrate improves, leading to a greater concern of latchup initiation from minority carriers.

2.3.1 Noise

There are many design practices to reduce noise in a chip [2–17]. Some noise reduction techniques have no influence on ESD robustness or latchup. Some of these design practices may also be good solutions for ESD protection and latchup minimization. Many noise prevention and reduction techniques have been proposed by Verghese, Schmerbeck and Allstot [2,3,6,7,11]. Noise prevention can be achieved by reduced noise generation through avoiding switching large transient supply current, reduced I/O driver generated noise, and lower switching function bus impedance [2].

Switching large transient supply currents is a function of whether the circuitry uses balanced current steering logic or voltage switching internal logic families. Noise reduction can also be achieved by power management. This is achievable by shutting down switching functions, logic circuits, or OCD networks. The I/O driver noise generation can be reduced by temporal and spatial placement solutions of the networks. For example, temporal improvements in the noise is achieved by avoiding simultaneous switching of I/O circuits, use of slower OCD circuits, use of voltage rise time-controlled networks, and use of balanced current steering OCD networks [3]. Placement of the drivers close to the power rail returns reduces the network inductance. Use of lower switching function bus impedance is achievable using multi-level and grid-like design, adding distributed on-chip decoupling capacitors, and providing a maximum number of chip power pad/pin ratio. Noise reduction techniques can be achieved by isolating sensitive circuits and providing noise-tolerant circuits. Isolation of sensitive circuits can be achieved by maximizing the impedance between the noise source and the sensitive circuits. This can be achieved by spatial separation and semiconductor process choices of the semiconductor substrate. Noise isolation of the sensitive circuit can also be achieved using guard rings, isolation structures, substrate contact, and shielding films or regions [3]. Many of these solutions for noise reduction are also good solutions for ESD protection and latchup in semiconductor components.

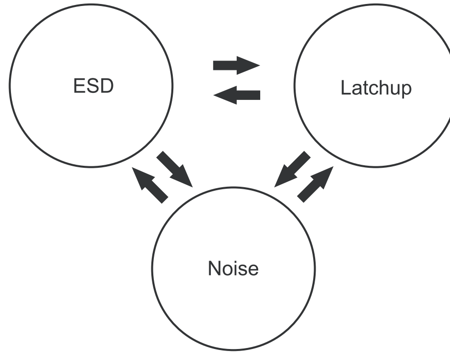

Figure 2.3 ESD, latchup, and noise

2.3.2 Latchup

Latchup occurs in semiconductor technology as a result of the presence of a parasitic *pnp* and *npn* bipolar transistor forming a *pnpn* (e.g., silicon controlled rectifier) [18–20]. Latchup robustness is a strong function of semiconductor technology in CMOS and BiCMOS technology [18–40]. The electrical, thermal, and spatial connectivity can influence the latchup robustness of a semiconductor chip. Latchup can be both a local as well as global phenomena in a semiconductor chip [36,40–42]. The electrical connectivity of pads, circuits, and circuit functional blocks can influence the latchup robustness of a semiconductor chip. The placement of pads, circuits, circuit function, power rails, and the architecture of the semiconductor chip or system can also play a key role in the latchup sensitivity. As with noise, the relative placement of injection sources, and latchup-sensitive circuits is key to latchup robustness [36,39,40]. Analogous to the noise issue, semiconductor process choices and semiconductor layout design influences latchup sensitivity. Substrate contacts, isolation structures, and the relative placement of circuits influence the spatial and electrical coupling which occurs in the semiconductor chip. Hence, the spatial and electrical solutions can influence noise, latchup, and ESD protection (Figure 2.3). Latchup design practices, as is true in ESD design practice, can involve the following concepts:

- Addressing high current and high voltage sources.
- Involvement of parasitic elements.
- Utilization of guard rings.
- Decoupling from power supply and ground connections.

2.4 INTERFACE CIRCUITS AND ESD ELEMENTS

Circuits and structures that interface with the external environment are vulnerable to electrical overstress (EOS), ESD, and latchup events. To prevent the failure of semiconductor components, circuits, or chips from ESD events, the circuits must be suitable to absorb the ESD event without damage to the circuit function. In the majority of cases, additional elements are added to the circuit whose function is to provide additional protection to the

circuit element. The network choices are dependent on the circuit function, performance requirements, and allowed chip area. The choice of the type of network is also a function of the input stimulus or the ESD event.

ESD networks are placed on the input pads of the circuits which interface with the external environment. Typically, ESD protection networks are placed in the semiconductor substrate and are composed of the same material as the semiconductor chip. In this fashion, the ESD protection networks are constructed out of the same materials and devices as the semiconductor process to which it is to provide the ESD protection. The fact that the ESD protection elements comprise the same technology it is to provide the ESD protection produces a challenge in that each technology will have a different operation and ESD performance.

ESD networks are placed on input pins (e.g., or connected to the input pads) for all circuits. According to Rent's rule, as the number of logic gates increases, the number of input/output (I/O) circuits also increases as [43]

$$N_{I/O} = A(N_C)^B$$

where $N_{I/O}$ is the number of I/O pads, N_C is the number of circuits, and the parameter A and B are constants. Given that the all I/O pads require an ESD protection network, then $N_{I/O} = N_{ESD}$; hence

$$N_{ESD} = A(N_C)^B$$

where N_{ESD} is the number of I/O ESD networks needed for a semiconductor chip.

Given a chip design contains an I/O network equal to area defined as $A_{I/O}$ (e.g., area of a given I/O network) then the total area $(A_{I/O})_T$ estimated for the I/O networks can be assumed to be approximately

$$(A_{I/O})_T = A_{I/O}N_{I/O} = (A_{I/O})A(N_C)^B$$

In typical implementations, the area of the ESD networks is a percentage of the total area dedicated to the I/O networks. The depending on the circuit, the application, and the ESD objectives, the percentage of the area can vary from 10 to 50% of the I/O network area. Defining a variable which represents the ratio of ESD area to the I/O cell area (e.g., k_{ESD}, where k_{ESD} varies from 0 to 1), we can estimate the total chip area dedicated to ESD protection of the input pads as

$$(A_{ESD})_T = k_{ESD}A_{I/O}N_{I/O} = k_{ESD}(A_{I/O})A\,(N_C)^B$$

ESD networks on input (input or output) pads are designed to provide protection against human body model (HBM) [44], machine model (MM) [45], charged device model (CDM) [46], and fast pulse phenomena that occurs on the physical pads. ESD networks can also serve as providing circuit protection from over- and under-voltage phenomena. The ESD networks can provide clamping function which assists in both over-voltage protection as well as chip functional performance.

ESD networks used for input pads in a peripheral I/O environment are placed near the physical pads for the given circuit function. In some chip architectures, OCD networks are

grouped in a semiconductor design. In an ''array I/O'' chip architecture, ESD networks are placed near the I/O circuit itself and are not local to the input pad. Hence, the ESD network is placed local to either the pad itself or the circuit itself, depending on whether the placement is on the chip boundary, or grouped in ''I/O banks,'' or in an array. The architecture of the chip and floor plan will determine the placement. The placement of the pad, the relative distance between the pad and ESD network, and the relative distance between the ESD network and the I/O device can influence the ESD robustness of the system. The electrical connectivity and spatial connectivity play a role; this is most critical with CDM failure protection.

ESD networks can be constructed to provide ESD protection from multiple types of events, where different circuit elements play a different role.

To provide ESD protection from HBM [44] or MM [45] events, a network is required to allow current flow of a positive or negative polarity which is applied to the input pad. HBM event waveforms are a damped double-exponential waveform of a single polarity. These events can be of a positive or negative polarity. As a result, an element is required for both types of events. For example, a double-diode network (Figure 2.4) can provide against both positive and negative ESD events.

To provide ESD protection against an MM event [45], the network must provide protection against an oscillatory waveform which oscillates from positive to negative polarity within a given pulse event at the input pad node. In the HBM event, only one polarity occurs at a given event. In these processes, the location or placement of the ESD network relative to the input pad is not crucial.

To provide ESD protection against CDM events [46], the spatial placement of the protection scheme relative to the vulnerable circuit element is very important. In the case of the CDM event, the substrate region is charged prior to the discharge process. As a result, the source of charge or current is not initially at the input pad, but contained within the semiconductor chip or package. In this case, the relative placement of the charge source and all physical elements in the network relative to the grounded pad is critical to the protection strategy. In a CDM event, the substrate doping concentration and the substrate charge relaxation time play a role in how the charge transfers to the various elements.

A circuit type which is sensitive to the CDM event are MOSFET receivers. A typical case is a MOSFET inverter input connected to an input pad. The MOSFET receiver input is

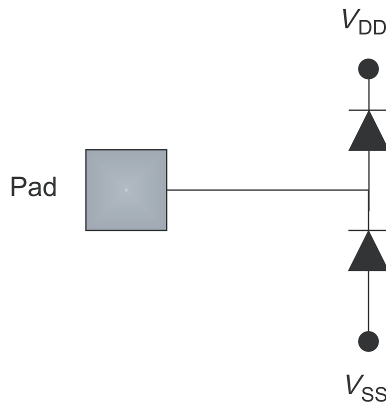

Figure 2.4 Circuit with double-diode ESD network

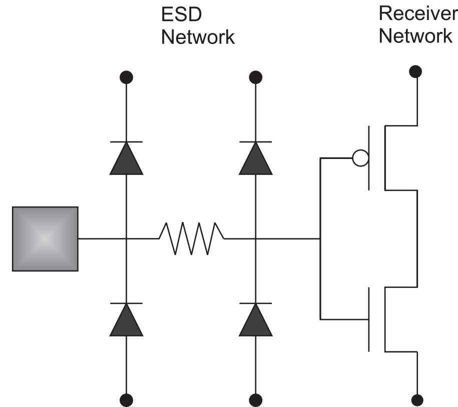

Figure 2.5 Example of a ESD network

connected to the gate of the *p*-channel MOSFET pull-up device and the gate of the *n*-channel MOSFET pull-down device. In a *p*-substrate wafer, the *n*-channel MOSFET gate is vulnerable to ESD damage during a CDM event. As the substrate is charged positively, and the input pad is grounded, the potential on the MOSFET inverter gates are at a ground potential. Charge from the substrate flows through the MOSFET gate dielectric structure. In this case, the MOSFET dielectric failure will occur. To avoid this issue, a *p-n* diode is needed local to the MOSFET gate whose impedance is lower. At the time constant of the discharge process, if the impedance through the diode structure is lower than the impedance of the MOSFET gate structure then the *p-n* junction will ‘‘current rob’’ the CDM current, avoiding destruction of the MOSFET gate structure. In this case, the spatial location of the CDM *p-n* diode and its net impedance will play a role in the effectiveness of protecting the MOSFET gate structure. By placement of an ESD protection *n*-diffusion device in the *p*-substrate spatially local to the gate, the holes flow from the substrate across the *p-n* metallurgical junction formed between the substrate and the *n*-region contained in the substrate (Figure 2.5).

2.5 ESD POWER CLAMP NETWORKS

In the architecture of systems and chip design, a current loop exists between the pad and the input circuit to a reference point. The ESD current loop is in parallel with the circuit current loop. The objective of the ESD current loop is to allow the current to flow through this bypass current loop avoiding failure of the sensitive circuits. In the ESD Kirchoff current loop, ESD input element allows the current to flow from the input pad to the power rails of the system. In order for the current to flow to the grounded reference rail, the ESD current must flow through the power grid, and from one power rail to another to complete the ESD Kirchoff current loop. The effectiveness of the ESD system is a function of the sum of the effectiveness impedance of the ESD Kirchoff current loop (Figure 2.6).

In very large systems, significant capacitance can exist between the power rails. The impedance between the power rails is inversely proportional to the product of the frequency

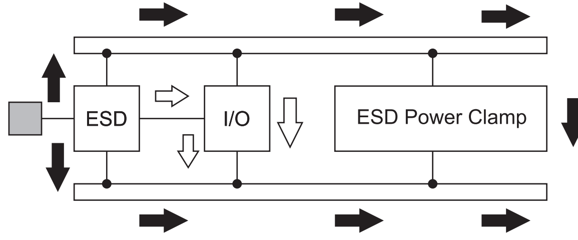

Figure 2.6 Illustration of the circuit Kirchoff current loop and the ESD Kirchoff current loop

of the ESD event and the capacitance, C_{eff}, between the power rails.

$$Z(\omega) = \frac{1}{j\omega_{\mathrm{ESD}} C_{\mathrm{eff}}}$$

In large systems, or large semiconductor chips, the impedance between the V_{DD} power rail and V_{SS} power rail can be small. With technology evolution and scaling, the sensitivity of the circuits has increased, requiring a lower impedance through the ESD Kirchoff current loop. Additionally, to achieve higher circuit performance the ESD input node circuit capacitance must be reduced. As the signal ESD structures are reduced in size, the impedance of these elements will increase. This increases the requirement for a lower power rail impedance in order to maintain a constant impedance through the ESD Kirchoff current loop.

With technology scaling and integration, noise is also a concern. To minimize noise, regions of the systems are separated to reduce noise coupling between circuits. This is achieved by creation of many separated power supply and ground rails. As the power rails are separated into smaller domains, the ESD Kirchoff current loop is limited to a smaller chip region, increasing the effective chip capacitance and the impedance.

To improve the effectiveness of the ESD Kirchoff current loop, ‘‘ESD power clamps’’ are placed between the power rails (e.g., V_{DD} and V_{SS}) to lower the effective impedance. In the case where no ESD power clamps are placed in the network, the system will find a current path which is the lowest impedance path. By placement of the ESD power clamp in the system, the current flow can be directed through specified current paths.

ESD events can also occur on the power rails. In this case, the ESD power clamp establishes a ESD Kirchoff current loop to the grounded reference point. The ESD power clamp also serves the role of establishing a low-impedance path to establish the direction of the current flow. As a result, the ESD power clamps serve a dual role of providing improved input pad protection and power rail-to-power rail connection.

ESD power clamps then provide electrical connectivity to nodal points in a system to allow the current flow from node to node. Whereas the functional objective of the system is to provide both spatial and electrical separation, the ESD power clamp plays the role of reestablishing electrical connectivity during ESD events.

The ESD power clamp networks can consist of passive or active elements. Active elements can consist of semiconductor components in the technology. ESD power clamps can consist of active elements such as *n*-channel or *p*-channel MOSFETs, and bipolar transistors. ESD power clamp elements can also contain passive elements such as resistors and capacitor elements.

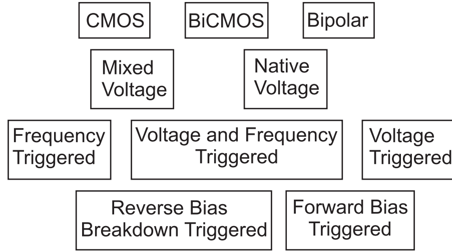

Figure 2.7 Example of classes of ESD power clamps

The ESD power clamps can be initiated by frequency or voltage triggering. As a result, different classes of ESD power clamps exist, with tradeoff in each implementation (Figure 2.7). In all cases, the ESD power clamp functional objective is not to be activated during a chip power-up or power-down, not to interfere with system functionality, and to activate during ESD events. Frequency-triggered ESD power clamps remain ‘‘off’’ during dc phenomenon but respond to the ‘‘ac’’ signal induced by the ESD pulse event (Figure 2.8). Voltage-triggered ESD power clamps remain ‘‘off’’ during normal voltage conditions and chip operation, but turn ‘‘on’’ when a voltage condition is exceeded. This can be an over-voltage condition, overshoot or undershoot phenomenon, or any high current event.

2.5.1 Placement of ESD Power Clamps

In the floor plan of the system or semiconductor chip, the placement of the ESD power clamps can influence their effectiveness. In the system or semiconductor chip, the power rail distribution has both resistance, capacitance, and inductive characteristics that can influence the current distribution in the ESD Kirchoff current loop. These impedance characteristics will provide a distributed nature to the current flow through the system. It is the impedance characteristics of the power rail system which will influence the floor plan and placement of the ESD power clamps.

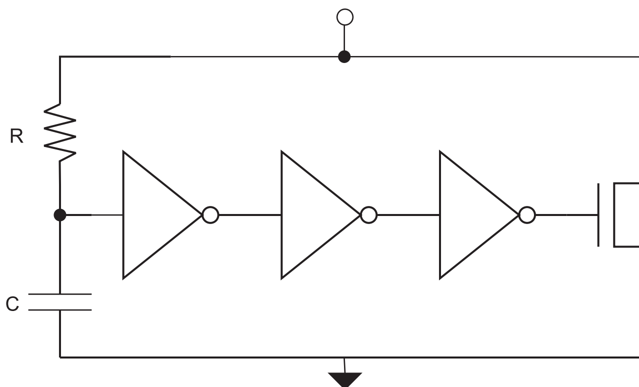

Figure 2.8 A frequency-triggered ESD power clamp

The second aspect of importance of the floor plan is the location of the signal pins (e.g., as well as corresponding ESD signal pin network) relative to ESD power clamps. The signal pin, the distributed power grid, and ESD power clamp element are contained in the ESD Kirchoff current loop. As the signal pin distance increases from the ESD power clamp element, the ESD current must flow through a farther distance through the power grid. As the distance increases, there will be a limitation of the total impedance in the ESD Kirchoff current loop which will limit the effectiveness of the ESD system. In this case, the placement is an electrical connectivity and electrical impedance defining the spatial positioning of the ESD power clamps relative to the signal pins [47].

In the floor plan of a chip design, there are other tradeoffs and issues that influence the placement of the ESD power clamps. ESD power clamps can be the sources of minority carrier injection and noise. ESD power clamps can also be sensitive to CMOS latchup. ESD power clamps can serve as a source of minority carrier injection which may affect adjacent circuitry causing noise concerns or external CMOS latchup. ESD power clamps may also undergo CMOS latchup. This can occur within the circuit itself or between elements in the ESD power clamps coupling with adjacent circuitry. ESD power clamps are also typically large area circuits. In a manufacturing environment, this can influence the photolithography, polish, and filling aspects. There may be advantages of placement and distribution based on improved manufacturability.

As a result, the architecture and placement of the ESD power clamps are critical to the ESD robustness of the system or chip.

In the evolution of the integration of the power clamps, in the 1.0–0.5-μm technology nodes (e.g., late 1980s to early 1990s), circuit design teams did not want to utilize chip area for ESD power clamps. It was common in peripheral I/O floor plans that ESD power clamps were placed in the corners of semiconductor chips. In an peripheral I/O design floor plan, the corner areas were not utilized for circuitry but left as empty areas. The placement of the ESD power clamps were placed in the corners, and electrically connected to the peripheral I/O power supply rail and the ground rails. It was experimentally found that as the power clamps were integrated into the I/O peripheral footprint, the ESD robustness improved. Early improvements in logic and microprocessor chips demonstrated a 4× improvement in HBM results as the power clamps were placed along the power bus.

For the future technology nodes below 0.5-μm technology (e.g., by mid 1990s), in peripheral I/O design, the ESD power clamps were placed more frequently as the need for a local power and ground pad was required. ASIC and microprocessor design methodologies required power pads and ground pads at a higher frequency of usage. Design methodologies required power pads at a fixed periodicity with a requirement for placing every number of I/O cells. In that case, the ESD power clamps were placed in the power and ground "service pad" areas. As the number of power pads (and corresponding ESD power clamps) increased, the ESD results improved; the role of the peripheral I/O metal bus resistance decreased between the I/O cell and the local ESD power clamp.

In some design methodologies, the ESD power clamps were integrated into the power placement methodology (Figure 2.9). In many design methods, the ESD power clamp was placed automatically with the placement of the "power book" or "power service module." With the automated integration of the ESD power clamps with the power pads, the design methodology provided an improved "built-in reliability" into the design and chip architecture.

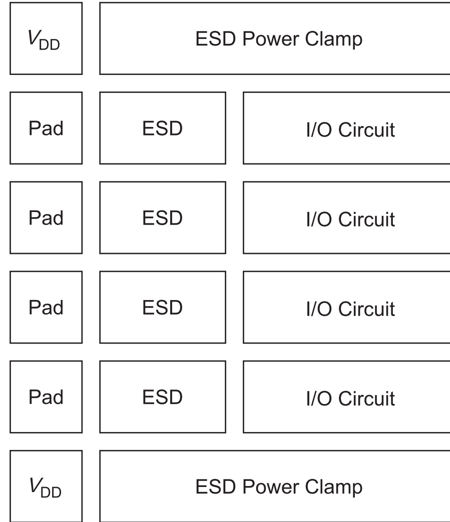

Figure 2.9 Placement of ESD power clamps

2.6 ESD RAIL-TO-RAIL DEVICES

In the architecture of systems and chip design, noise reduction is a key concern. Technology required to decrease the effect of noise on noise-sensitive circuits include lightly doped substrates, substrate region isolation (e.g., CMOS dual-well technology, triple-well technology, isolated epitaxial regions, and silicon-on-insulator), guard rings, and spatial separation [3]. To maximize the impedance from the noise source to the noise-sensitive circuitry, circuits are placed on separate power grids, power rails, and pads. Electrical connectivity is also reestablished at the package, board, or card level avoiding the on-chip noise sources impacting noise-sensitive circuits.

For ESD protection, an ESD Kirchoff current loop must be established between the power rails to allow electrical connectivity from any signal pin to any other power rail. In the ESD Kirchoff current loop, ESD input element allows the current to flow from the input pad to the power rail of the system. In order for the current to flow to a separate reference rail, the ESD current must flow through the power grid, and from one power rail to another to complete the ESD Kirchoff current loop. The effectiveness of the ESD system is a function of the sum of the effectiveness impedance of the ESD Kirchoff current loop [48].

The impedance between the power rails is inversely proportional to the product of the frequency of the ESD event and the rail-to-rail capacitance, C_{RR}, between the power rails

$$Z(\omega) = \frac{1}{j\omega_{\mathrm{ESD}} C_{\mathrm{RR}}}$$

In the case of ground rails, the rail-to-rail capacitance is intentionally reduced to minimize the noise coupling by lightly doped substrates, separate power grids, and spatial separation. Additionally, in the case of two power rails (e.g., core V_{DD} and I/O V_{DD}), the coupling is intentionally reduced to prevent the I/O networks from influencing the core quiescent power supply rail.

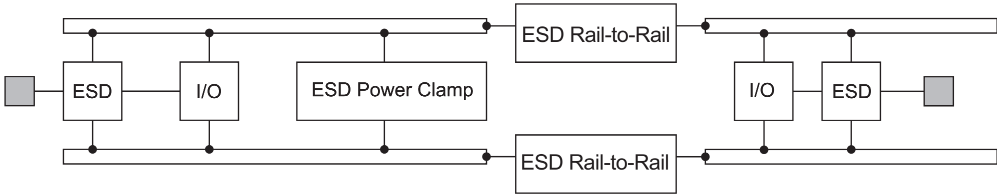

Figure 2.10 ESD rail-to-rail protection integrated into multi-rail chip design architecture

With scaling, the sensitivity of the circuits has increased, requiring a lower impedance through the ESD Kirchoff current loop. This increases the requirement for a lower power rail impedance in order to maintain a constant impedance through the ESD Kirchoff current loop. As the power rails are separated into smaller domains, the ESD Kirchoff current loop is limited to a smaller chip region, increasing the effective chip capacitance and the impedance.

To improve the effectiveness of the ESD Kirchoff current loop, ‘‘ESD rail-to-rail’’ networks are placed between the power rails (e.g., chip substrate V_{SS} and I/O V_{SS}) to lower the effective impedance. In the case where no ESD rail-to-rail clamps are placed in the network, the system will find an alternative current path, which is the lowest impedance path (which may not be favorable). Additionally, the ESD testing results will be significantly lower or destruction of structures or circuits is possible. By placement of the ESD rail-to-rail networks in the system, the current flow can be directed through specified current paths.

ESD rail-to-rail networks provide electrical connectivity to nodal points in a system to allow the current flow from node to node but, at the same time, not to impact the noise requirements [48,49]. Whereas the functional objective of the system is to minimize noise using both spatial and electrical separation, the ESD rail-to-rail network plays the role of reestablishing electrical connectivity during ESD events (Figure 2.10).

These ESD networks are typically bi-directional in nature. This is to allow the current flow between the rails in either direction. The ESD rail-to-rail networks can be the networks where the electrical bias potential may be equal or unequal. ESD rail-to-rail networks can be voltage-or frequency-triggered elements.

For example, a typical ESD rail-to-rail network is a bi-directional string of diode elements (Figure 2.11). The number of elements in series is a function of the noise margin and voltage differential between the two rails. The size of the diode structures is a function of the desired impedance needed for the ESD Kirchoff current loop to allow the ESD current to flow to the isolated power rail. In digital design, the voltage differential may establish the number of series elements desired. In analog and radio frequency (RF) design, the capacitance coupling may determine the number of desired elements and the physical size of each diode element.

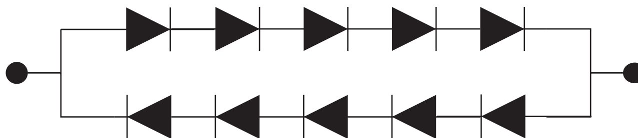

Figure 2.11 Example of a ESD rail-to-rail network

2.6.1 Placement of ESD Rail-to-Rail Networks

In the floor-plan of the system or semiconductor chip, the placement of the ESD rail-to-rail network can be a function of the impedance characteristics or architecture and floor plan of the semiconductor chip. The location of the signal pin, the nature of the distributed power plane, and ESD rail-to-rail element are contained in the ESD Kirchoff current loop [47].

2.6.2 Peripheral and Array I/O

In establishing the floor plan for the semiconductor chip, the ESD design architecture must be considered for the peripheral and the array foot print I/O planning. Figures 2.12 and 2.13 are examples of the peripheral and ‘‘array’’ I/O circuitry. There are key distinctions in the ESD design synthesis for the two different floor plans.

In peripheral I/O design, the fundamental features have certain ESD design advantages; these are as follows:

- Wire bonds and the I/O pads are placed on the chip periphery.
- Wire bond pad area can be utilized for ESD structures under the pads.
- ESD elements are placed local to the wirebond pad.
- ESD element can be placed local to the I/O pad circuit. In the case where the ESD element and the receiver circuit are separated spatially, this can lead to CDM concerns.

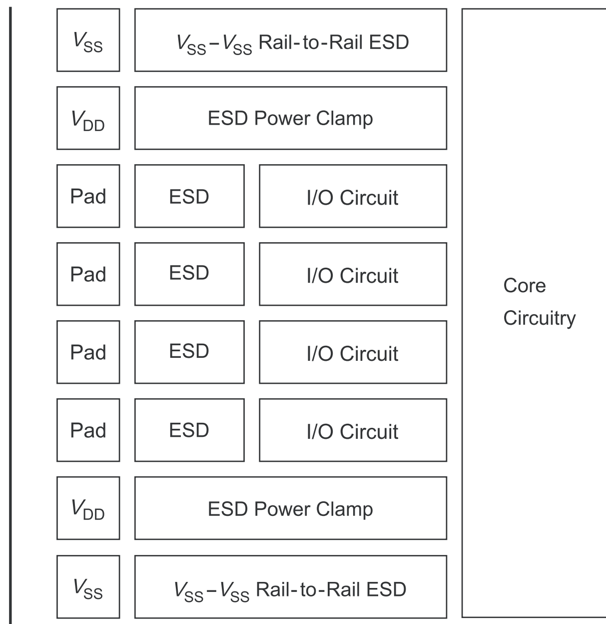

Figure 2.12 Peripheral input/output (I/O) floor plan

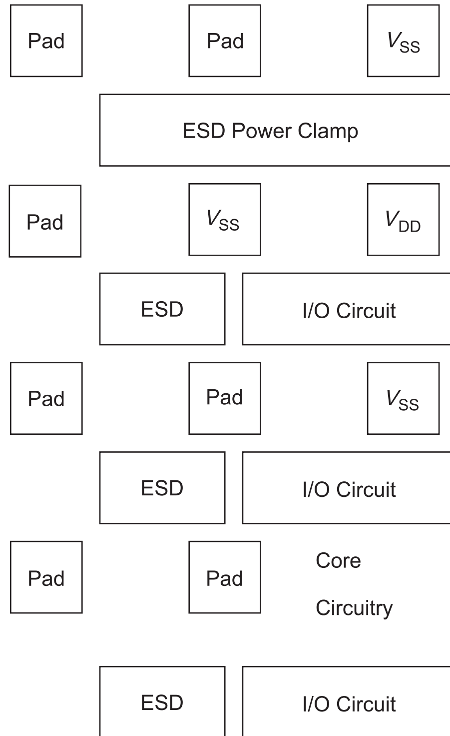

Figure 2.13 Array input/output (I/O) floor plan

- Adjacent pads can utilize ESD "diode sharing" and dummy metal rails.
- Guard rings can isolate the ESD and I/O circuits from the interior latchup sensitive circuits.
- ESD power clamps can be placed under power pads local to the I/O pads.
- ESD Rail-to-Rail clamps can be placed under the power pads local to the I/O pads and power rails.
- Power bussing for the ESD and I/O can be placed around the periphery of the semiconductor chip.
- Substrate ground guard ring exists on the semiconductor chip substrate, providing a good substrate ground.
- Power bus ground for ESD and I/O can be placed around the periphery of the semiconductor chip.
- Electrical wire connection between the pad and the ESD device is not density or wire-track nor wire-scaling limited.
- External latchup sensitivity associated with the ESD network, I/O network, and its interaction with internal circuitry can be reduced with guard rings and physical spatial separation.

In an array I/O design, the fundamental features have certain ESD design advantages and disadvantages; these are as follows:

- Circuitry exists under the pad regions. There is no "structure under pad" restriction.
- ESD element are placed local to the I/O pad circuit within the I/O book.
- Guard rings can be placed within the I/O pad book. Latchup is a greater concern in this architecture.
- ESD power clamps and rail-to-rail circuits must be placed in a service module for every grouping of I/O circuits.
- ESD rail-to-rail clamps must be placed in a service module for every grouping of I/O circuits.
- Power bus for the ESD and I/O can be placed as a "grid" lowering the total bus resistance distribution problem that occurs in peripheral I/O bus. This lowers the resistance between any I/O pin and the ESD power clamps, as well as the voltage distribution across the entire chip.
- Substrate ground guard ring exists on the external part of the chip, as well as internal substrate contact distribution.
- Power ground bus for the ESD and I/O can be placed as a "grid," lowering the total ground bus resistance distribution problem; this lowers the resistance between any I/O pin and the ESD power clamps, as well as the voltage distribution across the entire chip.
- Electrical wire connection between the pad and the ESD device is density or wire-track or wire-scaling limited; this leads to interconnect failure as a major ESD failure mechanism in high-pin count semiconductor chips.
- External latchup sensitivity associated with the ESD network, I/O network, and its interaction with internal circuitry can be a key concern. This can occur from voltage or current perturbations. HBM, machine model, and cable discharge events (CDE) can lead to latchup in array environments (Figure 2.14).
- External noise injection from the I/O network and its interaction with internal circuitry can be a key issue.

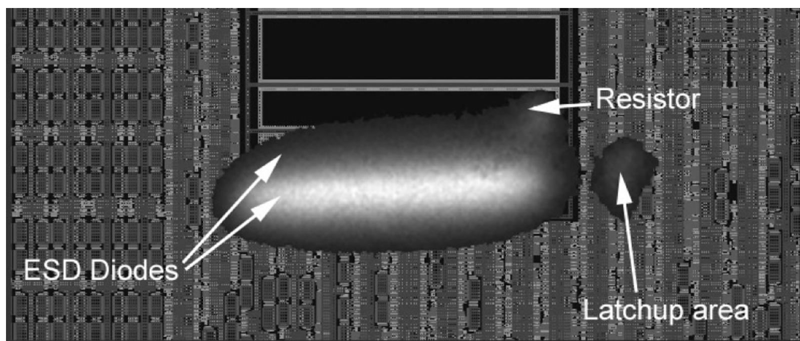

Figure 2.14 Example of latchup problem from array I/O due to ESD networks

2.7 GUARD RINGS

Guard rings are used in semiconductor chip design to isolate circuits and circuit functions. Guard rings serve multiple roles in semiconductor chip design [1,3,19–20,22,29]. Guard rings can be used to separate different types of circuits, and digital, analog, and RF circuit functions [3]. Digital circuits serve as noise sources to analog and RF networks; hence, the isolation by separate power domains and guard rings is critical. Guard rings serve as good electrical contact regions, absorb minority carriers, and establish spatial separation between the noise source and the sensitive region. Guard rings can avoid parasitic *pnpn* devices between the different types of circuits (e.g., inter-circuit parasitic *pnpn*).

Guard rings are used to separate different circuit function. Guard rings isolate peripheral circuits from core circuits. Peripheral circuits, such as ESD networks and I/O OCD, can serve as a source of minority-carrier injection and noise. Adding guard rings serves in collecting the minority-carrier injection and serves as a ground shield. The effectiveness of the guard ring to collect minority carrier is a function of the ‘‘guard ring efficiency.’’ Guard ring efficiency is a function of the type of guard ring (e.g., *n*-well, p^+ substrate contact, deep trench), the depth and width, and the underlying substrate properties [20,22,29].

Guard rings are also used within a circuit or sub-circuit to avoid latchup (e.g., intra-circuit parasitic *pnpn*) (Figure 2.15). To avoid CMOS latchup in I/O OCD networks, guard rings are used between *p*-channel MOSFETs and *n*-channel MOSFET, which can form parasitic *pnp*, and *npn* devices, respectively. The inter-coupling of the *pnp* and *npn* forms an intra-circuit parasitic *pnpn* leading to CMOS latchup.

CMOS latchup can occur between two I/O cells, or between the ESD network and an I/O network [36,40–42]. As a result, placement of the guard rings minimizes spatial and electrical coupling between ESD networks and I/O networks, which can lower the concern for CMOS latchup.

Guard rings can also be integrated into the ESD design [1]. For example, they can be used as part of the ESD design to achieve discharge to the substrate or to the power rails. In this case, the guard ring can serve as a guard ring and ESD function (Figure 2.16).

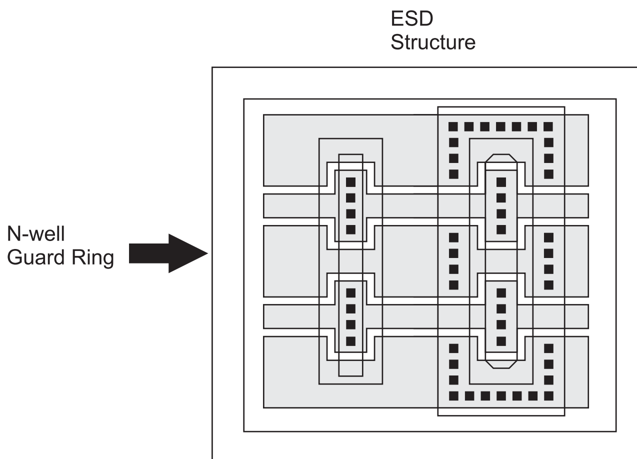

Figure 2.15 Guard ring structures

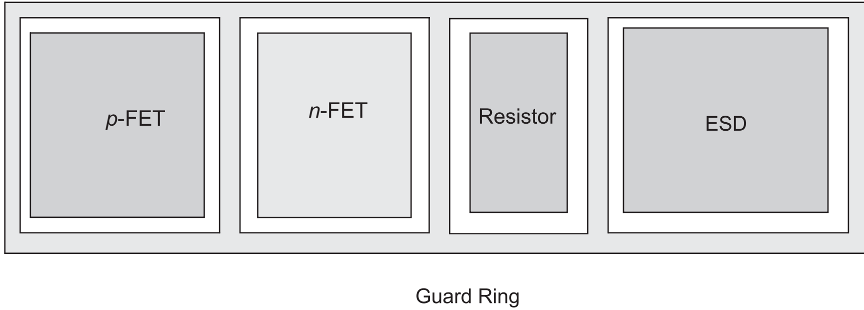

Figure 2.16 Example of guard rings integrated into the ESD design

2.8 PADS, FLOATING PADS, AND NO CONNECT PADS

In the design and floor planning of systems and semiconductor chips, the "foot print" (e.g., pad size, spacing, and pitch) of the pads is defined not by the circuits in the chip but by the packaging or design system for compatibility. In this environment, there are cases of floating pads, unused, or "no-connect pads." The footprint and placement of these pads can lead to ESD concerns. These structures are metal shape that can be charged from semiconductor wafer processing, human sources, shipping, or test equipment. These unused pads can be covered with an insulator film, exposed metal shape, or have solder balls. The solder balls are placed as mechanical supports but are not electrically connected to any circuits or power rails. In the case of source of current or charging of these elements, the voltage increases on the structures. As they charge, when the dielectric voltage is exceeded, inter-level dielectric (ILD) insulator failure occurs, leading to either cracking, insulator melting, or metal filling of the material defect.

As a result, the placement of signal lines, power busses, and the floor plan of these relative to the floating or "no-connect" pads can influence the failure mechanisms that can occur. Hence, the lack of electrical connectivity to the system and its spatial placement are critical to the success or failure of the usage of "no connect" structures.

2.9 STRUCTURES UNDER BOND PADS

In the floor plan and design of a semiconductor chip, the area on a chip for different circuit function is established by chip function. ESD signal pin, ESD power clamps, and ESD rail-to-rail devices can consume chip area, which is not insignificant. The area consumed by the ESD devices is a function of the number of logic circuits (e.g., Rent's rule). The area includes the number of signal pins, the number of power pads (e.g., V_{DD}, V_{SS}), and the size of the ESD networks. To reduce the area impact, area that are not used for functional applications can be utilized for ESD networks. These areas can include areas under the bond pads, between the bond pads, the corners of the chip, "fill areas."

ESD structures can be placed under bond pads to minimize the area impact to the chip [50–55]. For peripheral signal pads, the I/O cells are placed near the periphery of the semiconductor chip [50]. In this case, the architecture of the chip lends itself to allow the ESD networks under the pads. The floor plan of the semiconductor chip would involve allowing the ESD network under the bond pad and subsequently be connected to the

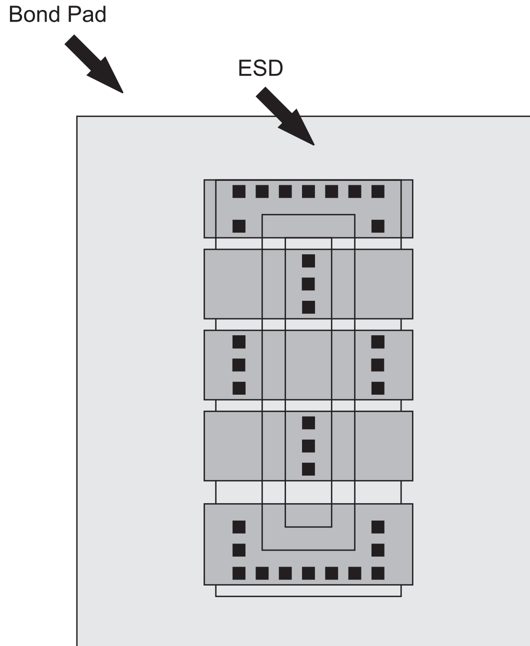

Figure 2.17 Structures under pads

peripheral circuit. This also lends itself to allow the ESD rail-to-rail networks under the power pads. In this architecture, the ESD networks are located on the outside of the chip, followed by the peripheral circuit, and then the core circuitry.

In many technologies, structures under bond pads (also known as circuits under pads) can lead to mechanical dielectric cracking, bond pad adhesion issues, and failure during humidity and temperature stressing [55]. The success of the ability to place semiconductor devices under bond pads is a function of the dielectric material, the thickness of the dielectric materials, the metallurgy material properties, and the physical design. Because of the technology issues, the type of the ESD device, and the interconnect and wiring design can be influenced by the requirements (e.g., metal line width, metal-to-metal spacings, and the allowed metal level) [51–54] (Figures 2.17 and 2.18). In today's technologies, there exist both aluminum and copper interconnects for the metal levels. Additionally, there are both silicon dioxide and low-*k* materials on the same and different levels. As a result, the qualification of ESD structures under pads must address different material mechanical properties.

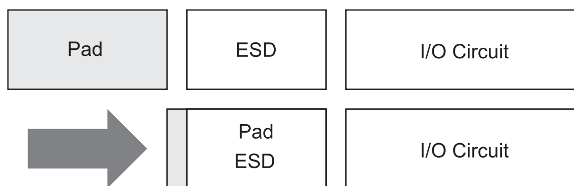

Figure 2.18 Examples of an I/O book with pad over part of I/O cell

2.10 SUMMARY AND CLOSING COMMENTS

In Chapter 2, a brief overview of the elements to construct ESD protection was discussed: ESD input circuits, ESD power clamp circuits, ESD rail-to-rail circuits, guard rings, and pad structures. The inter-relationship of electrical and spatial phenomena was discussed to provide the reader an understanding that one must think about both these aspects concurrently in the floorplan and architecturing of ESD in a semiconductor chip. Additionally, the relationship of noise, latchup, and ESD is briefly discussed, with the objective of making the reader conscience that other phenomena must be addressed in establishing the ESD design architecture and synthesis.

This provides a top-down perspective in developing an ESD strategy for a semiconductor chip. These will be discussed in depth in the following chapters; but first, spiraling downward, a bottom-up approach will be taken, starting from the basic design elements of MOSFETs, diodes, resistors, and other physical elements—then return to the elements discussed in this chapter.

In Chapter 3, the layout and design of MOSFET devices are discussed. The MOSFET device is used in core and peripheral circuits, as well as in ESD networks and ESD power clamps. The design and layout fundamentals associated with designing MOSFETs are fundamental to the understanding of establishing ESD protection in NMOS, PMOS, CMOS, RF CMOS, and BiCMOS technologies.

PROBLEMS

2.1. Given a square semiconductor chip with signal pads and power pads on the periphery of the chip, of width W, pitch P, and chip size W_{chip}. Assume the maximum wire width from the signal pad to the ESD network is $W/2$. What is the maximum number of signal pins N, assuming a power pad is needed for every four signal pins? At what pad density will the wire interconnect failure occur below 4000 V HBM, assuming the wire achieves 500 V/μm?

2.2. Given a square chip with peripheral pads (as stated above), assume a metal bus runs across a double-diode ESD networks with a diode series resistance R_d. Assume a metal bus resistance signal pad to signal pad of R. Assume an ESD power clamp in each corner of the semiconductor chip. Plot the total resistance from all signal pads to the ESD power clamp including the diode series resistance and bus resistance. Derive the relationship as a function of chip size.

2.3. Given a square chip with peripheral pads as above, but assume a power pad (with an ESD power clamp in each power pad) is placed within the signal pads where the ratio of power to signal pads is fixed for a given design. Derive the resistance relation for each pad to each power clamp, as a function of the ratio of power to signal pads.

2.4. Given a square chip of edge W_C, and array of pads whose pads are in an $M \times M$ array, where the total number of pads is $N = M \times M$, and are on the last level of metal, LM. Assume the metal level, LM-1, under the metal pads has a width W. Assume each successive metal level is scaled according to the MOSFET scaling parameter α. Assume the interconnect from the LM-1 level connects from the pad to the ESD

network and I/O cell. Assuming a minimum wire width, what is the width of the metal level for a LM-1 level? Assuming the first-level metal M1 fails from ESD events at a value V_0 (in terms of HBM voltage), when does the successive levels fail at? How do these results compare to a peripheral signal pin result where the metal from the pad to the ESD is $W/2$ of a first level metal M1 material?

2.5. Given an I/O bank of OCDs, where the ESD network is integrated within the I/O cell, given a fixed I/O form factor of width W and length L. Assume the metal line connecting the I/O bank are in a wiring bay of fixed pitch associated with the I/O width W. At what I/O width, assuming 500-V HBM per unit micron of wire width will the chip not achieve 10-kV HBM? 8-kV HBM? 6-kV HBM? 4-kV HBM? 2-kV HBM? Assume the width and space between adjacent lines are equal for each I/O cell.

2.6. OCD bank ESD results can degrade along a chip design when the metal bus is not properly terminated. Given a bank of N OCD in series on a single metal V_{DD} bus. Assume that the bus is electrically connected to the chip power on one side. Produce an incremental model showing the ESD resistance and the bus resistance of the successive OCD cells. Assume a width W for the width of the OCDs, and a wire resistance R between each successive driver. Derive the anticipated ESD roll-off that occurs in the OCD bank for an assumed failure mechanism assuming an ESD current I. Make an assumption on the circuit type and failure mechanism in that circuit.

2.7. Assuming that ESD structures are placed under a pad. Given a square chip of edge W, square pad width W_{pad}, pad pitch P (pad and space), and square ESD devices of size W_{ESD}. Assume a core chip square area of W_{CORE} is needed for circuitry. Derive a relationship of the number of pads for a given chip size, as a function of the variables above. Evaluate the total chip area savings when the ESD device is placed under a pad where the ESD area and the pad sizes are equal in magnitude. Given a 200- and a 300-mm wafer, what is the productivity improvement?

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3 Electrostatic Discharge (ESD) Design: MOSFET Design

3.1 BASIC ESD DESIGN CONCEPTS

MOSFET ESD design contains many fundamental ESD concepts that are relevant to the MOSFET as well as to other structures. ESD design concepts address the control of MOSFET second breakdown [1–22], and the prevention of MOSFET dielectric breakdown [23–27]. These incorporate the concepts of sensitivity to ESD mechanisms such as human body model (HBM), machine model (MM), and charged device model (CDM) events [28,29]. MOSFET design must incorporate local to global effects from the contact to the multi-finger MOSFET structure. In this chapter, we will focus on the MOSFET to highlight these issues.

In ESD design, there are some underlying fundamental concepts that one can adhere to in order to have effective ESD results:

- Provide a solution that establishes a low-voltage trigger element, which can discharge a high current.
- Provide spatially uniform current density within the trigger element.
- Avoid localized Joule heating within the trigger element.
- Avoid electrical connections that exceed the breakdown voltage of the dielectric films.
- Operate the device under the MOSFET second breakdown voltage.
- Improve thermal stability of the MOSFET structure.

The ability to provide a low-voltage trigger element can be achieved by the following means:

- Minimum channel length MOSFETs to provide low MOSFET snapback voltages.
- Low threshold voltage MOSFETs.
- Gate coupling techniques.

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- Drain coupling techniques.
- Substrate coupling.
- Dynamic threshold MOSFET coupling techniques.

High current can be achieved in MOSFET ESD structures by the following means:

- *n*-channel MOSFETs instead of *p*-channel MOSFETs for higher mobility (e.g., increased MOSFET current drive).
- Low-threshold MOSFET for increased MOSFET current drive (e.g., maximize $V_G - V_T$).
- Dynamic threshold voltage techniques.

Spatial uniformity is achieved in the MOSFET ESD structure by the following means:

- Provide design symmetry in the metal and contact design.
- Ballasting in the direction of the MOSFET current flow.
- Ballasting perpendicular to the direction of the MOSFET current flow.
- Segmentation of the MOSFET into multiple regions.

Avoidance of localized heating in the MOSFET structure can be achieved by the following means:

- Provide design symmetry in the metal and contact design.
- Ballasting in the direction of current flow.
- Ballasting perpendicular to the MOSFET current flow (e.g., lateral ballasting).
- Introduce internal ballasting elements.
- Introduce external ballasting elements in the MOSFET ESD circuit.
- MOSFET structures with deep junctions for increased emitter depth.
- MOSFET structures with ESD implants (e.g., deep junctions) for increased emitter depth.
- MOSFET structures with extension implants or deep low doped drain regions.

Avoidance of MOSFET second breakdown [1–22] can be achieved by the following means:

- Avoid the ESD MOSFET from undergoing MOSFET snapback.
- MOSFET gate coupling techniques.

Avoidance of failure of the MOSFET structure due to dielectric breakdown [23–29] can be achieved via the following means:

- Avoid MOSFET gate-to-power rail direct connections.
- Avoid MOSFET gate-to-pad direct connections.

Ballasting can be introduced in a MOSFET structure using the following ESD design methods:

- Removal of refractory metal silicides on the MOSFET source and drain regions in the direction of the MOSFET current flow.
- Removal of refractory metal silicides on the MOSFET source and drain region lateral to the MOSFET current flow.
- Removal of silicide under contact regions.
- Maintain high-resistance phase state of the silicide film (e.g., titanium has two resistive states).
- Introduction of resistor elements in series with the MOSFET structure (e.g., n diffusion, p^- diffusion, n-well, polysilicon film, tungsten local interconnect, and wire resistors).
- Segmentation of MOSFET into multiple source and drain by introduction of isolation perpendicular to the MOSFET source and drain region.
- Segmentation of MOSFET by introduction of lateral high resistance source and drain regions.
- Segmentation of p-well and n-well regions by introduction of lateral well resistance regions.

Under high-current operation, the MOSFET undergoes electrical and thermal breakdown. Second breakdown is an electro-thermal effect typically leading to thermal runaway and component failure. Parasitic bipolar transistors are inherent in bulk and silicon-on-insulator (SOI) MOSFET devices in parallel with the surface channel MOSFET conduction.

In a MOSFET, the current flow from the drain to source. In parallel with the drain and source diffusion, a parasitic bipolar transistor is formed. The total drain current can be expressed as a function of the MOSFET drain-to-source current, the parasitic bipolar current, and the thermal generation current,

$$I = I_{\text{DS}} + I_{\text{C}} + I_{\text{G}}$$

The parasitic bipolar transistor can express the current in the form,

$$I_{\text{C}} = I_{\text{s}}\left[\exp\left(\frac{qV_{\text{BC}}}{kT}\right) - \exp\left(\frac{aV_{\text{BE}}}{kT}\right)\right]$$

where

$$I_{\text{s}} = \frac{q^2 A^2 n_i^2 \langle D_n \rangle}{Q_{\text{B}}}$$

$$\langle D_n \rangle = \frac{qA \int_0^{x_{\text{B}}} p(x)\,\mathrm{d}x}{\int_0^{x_{\text{B}}} \frac{p(x)}{D_n}\,\mathrm{d}x}$$

and

$$Q_{\mathrm{B}} = qA \int_0^{x_{\mathrm{B}}} p(x)\mathrm{d}x$$

The base current can be expressed in a similar form where current is a function of the excess charge in the base divided by the recombination time,

$$Q'_{\mathrm{B}} = qA \int_0^{x_{\mathrm{B}}} [n(x) - n_0]\mathrm{d}x$$
$$I_{r\mathrm{B}} = \frac{Q'_{\mathrm{B}}}{\tau_n}$$

In the case of a MOSFET, the base region is the p^- substrate region. In the base, it can be assumed that the doping concentration in the lateral transistor structure is a constant. This simplifies the collector current equation.

$$I_{\mathrm{C}} = I_{\mathrm{s}}\left[\exp\left(\frac{qV_{\mathrm{BC}}}{kT}\right) - \exp\left(\frac{aV_{\mathrm{BE}}}{kT}\right)\right]$$
$$I_{\mathrm{s}} = \frac{q^2A^2n_i^2\langle D_n\rangle}{Q_{\mathrm{B}}} \approx \frac{qA_{\mathrm{e}}n_i^2D_n}{N_{\mathrm{a}}L_{\mathrm{eff}}}$$

where A_{e} is the emitter area, D_n is the electron diffusion coefficient in the channel region, N_{a} is the doping concentration in the channel region, and L_{eff} is the lateral bipolar base width of the lateral *npn* which is the effective channel length. For a MOSFET, the emitter area is equal to the product of the MOSFET channel width and the source/drain implant junction depth, $W_{\mathrm{eff}}x_{\mathrm{j}}$. The effective area is the area that participates in the forward bias injection into the substrate.

$$I_{\mathrm{s}} \approx \frac{q\left(W_{\mathrm{eff}}x_{\mathrm{j}}\right)n_i^2D^n}{N_{\mathrm{a}}L_{\mathrm{eff}}} \equiv q\frac{W_{\mathrm{eff}}}{L_{\mathrm{eff}}}\frac{n_i^2D_n}{N_a}$$

For the base current, the equation can be expressed as

$$I_{\mathrm{B}} = I_{0\mathrm{e}}\left[\exp\left(\frac{qV_{\mathrm{BE}}}{kT}\right) - 1\right]$$

where the base current term $I_{0\mathrm{e}}$ is expressed as

$$I_{0\mathrm{e}} \approx \frac{qA_{\mathrm{e}}n_i^2D_p}{N_{\mathrm{DE}}L_{p\mathrm{E}}} \equiv \frac{q\left(W_{\mathrm{eff}}x_j\right)n_i^2D_p}{N_{\mathrm{DE}}L_{p\mathrm{E}}}$$

The bipolar current gain is obtained from the ratio of the collector current to the base current. In the case of forward active voltage, the exponential term for the collector–base is negligible, and the bipolar current gain can be expressed solely as a function of the ratio of

the two current expressions.

$$\beta_{\mathrm{f}} = \frac{I_{\mathrm{C}}}{I_{\mathrm{B}}} \approx \frac{I_{\mathrm{s}}}{I_{0\mathrm{e}}}$$

This can be expressed as

$$\beta_{\mathrm{f}} = \frac{I_{\mathrm{C}}}{I_{\mathrm{B}}} \approx \frac{I_{\mathrm{s}}}{I_{0\mathrm{e}}} \equiv \frac{D_n}{D_p} \frac{N_{\mathrm{DE}}}{N_{\mathrm{a}}} \frac{L_{p\mathrm{e}}}{L_{\mathrm{eff}}}$$

From the current model, avalanche generation can be expressed as a function of the multiplication factor and the total current flowing through the high-electric-field region, where the generation current can be expressed as

$$I_{\mathrm{G}} = (M-1)(I_{\mathrm{DS}} + I_{\mathrm{C}})$$

When the electric fields are low, M is unity, leading to no generation occurring. As the electric field increases in the transistor, avalanche multiplication increases leading to the generation term. In this expression, some of the hole generation current will serve as base current for the lateral bipolar element, while some of the holes generated will enter the substrate serving as substrate current. The substrate current can be expressed as [17–21],

$$I_{\mathrm{SX}} = (M-1)(I_{\mathrm{DS}} + I_{\mathrm{C}}) - I_{\mathrm{B}}$$

The substrate current in a MOSFET is typically an issue for hot electron generation and total power consumption. For ESD analysis, the substrate current is important because it is associated with the voltage drop that occurs locally in the MOSFET region at high currents [17–21];

$$V_{\mathrm{SX}} = I_{\mathrm{SX}} R_{\mathrm{sub}}$$

hence, the voltage drop in the substrate can be expressed as

$$V_{\mathrm{SX}} = [(M-1)(I_{\mathrm{DS}} + I_{\mathrm{C}}) - I_{\mathrm{B}}]R_{\mathrm{sub}}$$

When the voltage drop equals the forward bias voltage of the p–n junction formed between the source and the substrate, MOSFET snapback occurs. This can be stated as,

$$V_{\mathrm{BE}} = V_{\mathrm{SX}} = [(M-1)(I_{\mathrm{DS}} + I_{\mathrm{C}}) - I_{\mathrm{B}}]R_{\mathrm{sub}}$$

or a condition for MOSFET snapback occurs when

$$V_{\mathrm{BE}} \geq [(M-1)(I_{\mathrm{DS}} + I_{\mathrm{C}}) - I_{\mathrm{B}}]R_{\mathrm{sub}}$$

From this development, it is important to quantify the substrate resistance in order to anticipate the onset of MOSFET snapback. In a multi-finger structure, the MOSFET can be represented as a plurality of parallel MOSFET devices where the gate and the drain are coupled to common nodes, and the sources are independent nodes. The MOSFET fingers are also coupled together through the substrate potential drops. This introduces a complex model

for the substrate current and the substrate resistances. This can be addressed through coupled system of equations, matrices, or transfer resistance representations.

In MOSFET devices, avalanche breakdown occurs in the metallurgical junction formed between the MOSFET drain and its supporting structure. In the case of an n-channel MOSFET, avalanche breakdown occurs in the n^+ source/drain implant to p^- epitaxy (e.g., or p^- substrate) metallurgical junction. From the Townsend criteria,

$$\int \alpha \mathrm{d}x = 1$$

where the integration of the impact ionization over the physical space where there exists a non-zero electric field. From this form, the avalanche multiplication factor M can be related to the impact ionization coefficient integrated over the depletion width and can be expressed as

$$M = \frac{1}{1 - \int \alpha \mathrm{d}x}$$

In a depletion region, the peak electric field is maximum at the center region of the dipole. In the analysis of the MOSFET, the model is simplified to express it as a function of the depletion width. Hence, it can be integrated over the integral and stated in the form

$$M = \frac{1}{1 - \alpha x_{\mathrm{d}}}$$

From semiconductor physics, it is known that the depletion width can be expressed as a power of the applied voltage

$$x_{\mathrm{d}} \propto (V_{\mathrm{D}})^n$$

The power of this relationship is a function of the doping profile at the metallurgical junction. In this form, it is also clear that when the voltage is greater than the avalanche breakdown voltage, the multiplication factor should increase rapidly. Hence heuristically, it is clear that the multiplication expression should satisfy the form

$$M = \frac{1}{1 - \left(\frac{V_{\mathrm{D}}}{V_{\mathrm{av}}}\right)^n}$$

In this form, as the drain voltage approaches the avalanche breakdown voltage, the multiplication factor approaches infinity. Amerasekera pointed out that the above relationship does not address the effect of the gate voltage on the electric field in a MOSFET gated diode region. As the gate electrode voltage in a MOSFET is increased, the electric field in the drain region increases. From the expression

$$M \approx \frac{1}{1 - \alpha(E) x_{\mathrm{d}}} = \frac{1}{1 - \alpha_0 x_{\mathrm{d}} \exp\left\{-\frac{B}{E}\right\}}$$

Substituting in a voltage condition where the electric field is the voltage over a physical distance, where the voltage across the depletion region is the drain voltage minus the drain saturation voltage, and the distance is the depletion region

$$M \approx \frac{1}{1-(\alpha_0 x_\mathrm{d})\exp\left\{-\frac{Bx_\mathrm{d}}{\{V_\mathrm{D}-V_{\mathrm{d_{sat}}}\}}\right\}}$$

where the drain saturation velocity is expressed as

$$V_{\mathrm{d_{sat}}} = \frac{V_\mathrm{G}-V_\mathrm{t}}{a+b(V_\mathrm{G}-V_\mathrm{t})}$$

where saturation velocity is the voltage drive divided by a two-parameter expression in the denominator, and the voltage drive is the gate voltage minus the MOSFET threshold voltage.

The avalanche generation current can then be calculated from multiplication factor and the current flowing through the drain junction. The current flowing through the drain structure is the MOSFET current flowing through the surface region (e.g., MOSFET source-to-drain current) as well as the current flowing from the parasitic bipolar transistor formed from the MOSFET source, epitaxy region, and the MOSFET drain forming a lateral *npn* transistor. In this case, the MOSFET drain and source serve as the bipolar junction transistor collector and emitter, and the epitaxial region serves as a base. The avalanche current can be expressed as

$$I_\mathrm{av} = (M-1)I = (M-1)\{I_\mathrm{DS}+I_\mathrm{C}\}$$

The avalanche generation current flows to the p^- substrate region of the n-channel MOSFET structure. A portion of this current flows to the base of the lateral parasitic *npn* transistor serving as the emitter–base current, while the rest of the current will flow to the substrate region as substrate current. Hence, the avalanche current can be defined as the sum of the substrate current (flowing to the substrate contact), and the base current of the lateral *npn* transistor (serving as base drive current)

$$I_\mathrm{av} = I_\mathrm{SX}+I_\mathrm{B}$$

Then the substrate current can be estimated as

$$I_\mathrm{SX} = I_\mathrm{av}-I_\mathrm{B} = (M-1)\{I_\mathrm{DS}+I_\mathrm{C}\}-I_\mathrm{B}$$

From this expression, Amerasekera noted that the avalanche current and the substrate current can be expressed as a function of the impact ionization, the depletion width, drain voltage, drain saturation voltage, and MOSFET n-channel and parasitic *npn* current [17–21].

$$I_\mathrm{av} \approx \left(\frac{1}{1-(\alpha_0 x_\mathrm{d})\exp\left\{-\frac{Bx_\mathrm{d}}{\{V_\mathrm{D}-V_{\mathrm{d_{sat}}}\}}\right\}}-1\right)\{I_\mathrm{DS}+I_\mathrm{C}\}$$

and

$$I_{SX} \approx \left(\frac{1}{1 - (\alpha_0 x_d) \exp\left\{ -\frac{B x_d}{\{V_D - V_{d_{sat}}\}} \right\}} - 1 \right) \{I_{DS} + I_C\} - I_B$$

3.1.1 Channel Length and Linewidth Control

In the ESD design of a MOSFET structure, the MOSFET channel length has a key role. The MOSFET channel length has a role in the MOSFET snapback voltage and the MOSFET dynamic on-resistance [30,31]. On a local scale, the MOSFET channel length and the MOSFET linewidth control have an important role in the current distribution in multi-finger MOSFET structures. On a global level, the MOSFET across-chip linewidth variation (ACLV) has an influence on the ESD failure pin probability distribution and cumulative failure distribution functions [31] (Figure 3.1).

The understanding of the MOSFET channel length control plays a role in the ESD response of single-finger and multi-finger MOSFET structures. On a local scale, the MOSFET linewidth control has an important role in the MOSFET snapback voltage and the current distribution in multi-finger MOSFET structures. In a multi-finger MOSFET structure, the relative channel lengths play a role in how the current distributes in the MOSFET structure. On a global level, the MOSFET ACLV has an influence on the ESD failure pin probability distribution and worst-case pin failure. The MOSFET channel length and the channel length linewidth control is a function of the MOSFET photolithography, MOSFET gate stack structure, and the MOSFET gate etch process [31].

The scaling of MOSFETs has led to a significant evolution of the photolithography and gate conductors etching processes. Scaling of the numerical aperture (NA) and exposure wavelength of lithographic systems from G-Line (436 nm), I-line (365 nm), deep ultra-violet DUV (e.g., 240 nm), and 193-nm lithography permitted technology scaling to sub-0.5 μm dimensions. Today, demonstrations of extreme-ultraviolet (EUV) micro-exposure tools at 32 nm have

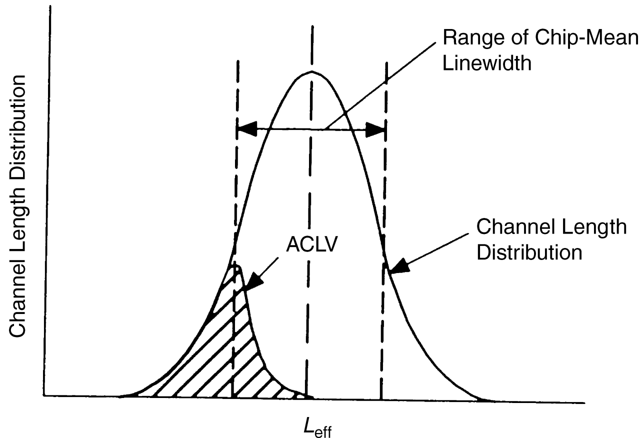

Figure 3.1 Linewidth

been demonstrated for 30-nm isolated lines. With the transition from LOCOS isolation to shallow trench isolation (STI) and the introduction of anti-reflective coating (ARC), topography issues that influence linewidth were reduced; however, new gate conductor linewidth issues were discovered that influence MOSFET design. MOSFET linewidth distribution is used to control semiconductor manufacturing assembly lines. At long channel lengths, channel length limited yield (CLLY) tends toward zero because of poor chip performance. At short channel lengths, yield tends to zero because of MOSFET channel length hot electron degradation, MOSFET device leakage, MOSFET punch-through, and MOSFET timing race conditions. These limitations have led to considerable amount of interest in gate linewidth centering, optimization, and control. Channel length control can be divided into two broad categories: chip-mean linewidth variation (CMLV) and across-chip linewidth variation (ACLV). Both CMLV and ACLV influence the ESD failure distribution and ESD robustness of an individual semiconductor chip. CMLV and ACLV both determine the channel length variation, δL. CMLV consists of across-wafer components, wafer-to-wafer, and lot-to-lot variations. CMLV is calculated as the root-mean-square variation of the lot-to-lot, wafer-to-wafer, and chip-to-chip variation. This distribution contains both systematic and random variations. Each variation can be driven by different production issues. Chip-to-chip variation, for example, can occur due to tool radial distributions of etch processes.

Wafer-dependent lithographic variations can determine wafer-to-wafer linewidth control variations. The chip mean linewidth distribution is a function of how a manufacturing line is controlled and a tool set quality. On the other hand, ACLV component, the within-chip linewidth variation, is driven by the local lithographic and gate-conductor etch processes. For large chips, systematic and random mask variations, lens distortion, and photo tool slit intensity variations play a role in the across chip variations. ACLV includes systematic effects associated with variations in the x–y orientation (e.g., astigmatism and comma), identical and non-identical lines, gate-to-gate spacing (e.g., gate pitch), and within-chip spatial variations. ACLV also contains etch-loading effects: aspect ratio-dependent etching (ARDE), micro-loading, and macro-loading. For ARDE, etch bias is dependent on adjacent structures. Micro-loading occurs where etch bias for identical structures varies as a result of local pattern density factors. Macro-loading reflects the etch-bias differences created by average etch loading on a wafer.

CMLV and ACLV are treated as two separate and independent parameters. For ESD analysis of semiconductor chips, these two parameters should be considered as separate issues. In the case of CMLVs, this impacts the ESD robustness chip-to-chip. Given that the MOSFET linewidth influences the ESD robustness of the technology, this will influence the ESD variation of tested product and will influence the sample size to guarantee the worst-case ESD robustness. From a design perspective, the ACLV issue is a larger concern in which it influences the ESD variation within a MOSFET, the pin-to-pin ESD failure probability distribution, and the worst-case pin condition.

3.1.2 ACLV Control

Controlling across-ACLV is one of the most important variables in semiconductor chip development, and can play a key role in ESD design practices for single finger and multi-finger MOSFET design. ACLV is important for circuit functionality, circuit-to-circuit matching, standby power, and MOSFET hot-electron degradation [31]. ACLV is a function of both

etching and photolithographic bias. Etching bias variability is defined as the difference between a photo-resist and etched critical dimensions. Etching and photolithographic bias variability are the two dominant components in ACLV control. ACLV consists of both local and non-local effects from both photolithography and gate conductor etching. The non-local systematic and random effects influence the ESD pin distribution, when the MOSFET channel length is the dominant ESD-limiting result. The local systematic effects influence the MOSFET design layout and the ESD robustness of a given single- or multi-finger MOSFET structure.

Parameters that are key to ACLV are:

- Line-to-line matching of two adjacent lines.
- Orientation.
- Nesting effects.

Photolithographic chip field variations influence the MOSFET channel length of two identical MOSFET transistors with the same orientation, at two different locations in the optical field. This non-local macroscopic effect of chip field variations leads to a wider ESD pin distribution. Lens distortion, such as astigmatism and coma, can lead to *x–y* orientation-dependent effects. ACLV measurements of identical MOSFET structures, which are oriented on a different axis, have different channel length distributions. The *x–y* orientation is relevant to semiconductor chips with peripheral I/O books, which contain I/O off-chip drivers and ESD elements, whose orientation changes around the semiconductor chip. In the choice of the floor plan, the orientation of the MOSFET-based off-chip driver (OCD) circuits and ESD elements changes on two sides of the chip. Therefore, ESD pin distributions are widened by this issue. In the peripheral I/O floor plan, the ESD pin distribution samples both the full chip field variations and the *x–y* orientation issues.

For local ACLV effects, the "nesting" phenomenon is of significant importance to the ESD design of single- and multi-finger MOSFET structures. Linewidth control in the

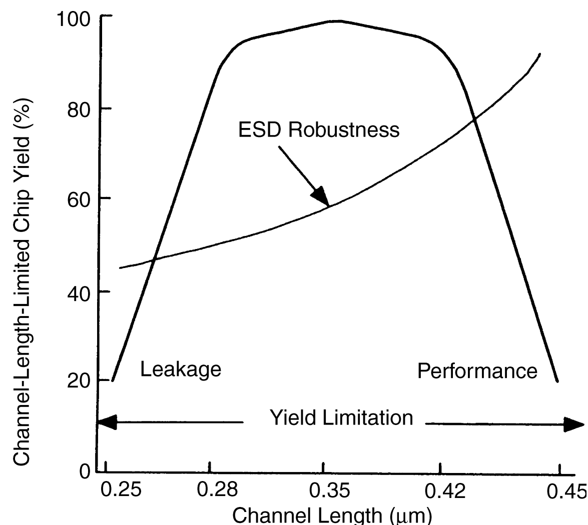

Figure 3.2 Linewidth distribution and ESD

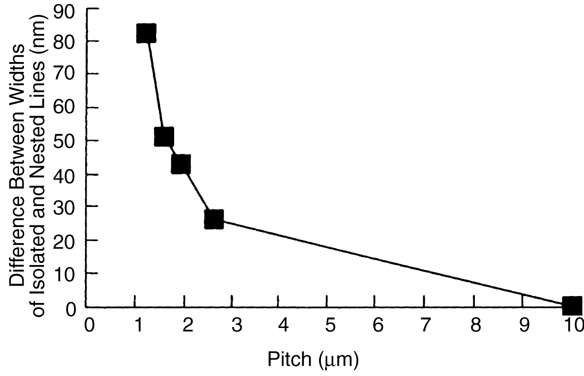

Figure 3.3 Difference between an isolated and nested line bias as a function of design pitch

diffraction limit of photolithography tools for minimum images leads to linewidth bias, which is dependent on both the gate conductor length and space to the adjacent gate conductor. Linewidth bias occurs when the relative difference between the maximum and minimum intensity is modulated by the spacing between the adjacent intensity peaks. For positive tone resist, as the space between the two identical gate conductor lines decreases, the linewidth bias increases. For negative tone resist, linewidth bias decreases with decreasing gate-to-gate space. This effect is the result of the differences in the resist exposure in the optical diffraction limit. Hence, depending on the photo-resist, opposite effects can occur as a function of the linewidth gate-to-gate space. For the etch process, with etching complex gate structures, several sequential plasma etching steps are required leaving behind sidewall passivation and polymer build-up. Aspect ratio-dependent etching dominates the linewidth variation as a function of the gate-to-gate space.

Linewidth control influences the ESD robustness of a multi-finger MOSFET. Figure 3.3 shows the linewidth difference as a function of the MOSFET gate pitch (e.g., sum of the MOSFET gate length and gate-to-gate space). As the pitch decreases, the linewidth variation difference between "isolated" line and the closely spaced "nested" line rapidly decreases. Figure 3.4 shows an "isolated" and "nested" MOSFET image. An "isolated" line is a

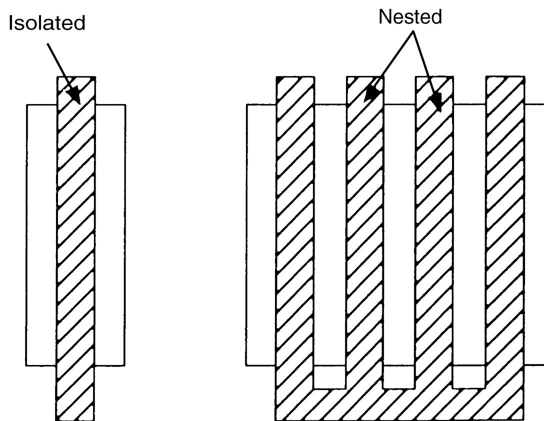

Figure 3.4 Example of an "isolated" and "nested" MOSFET image

gate conductor with no parallel adjacent gate structure within some distance (e.g., gate-to-gate space greater than 10 μm). As the spacing increases, the photo and etch bias change decreases, providing a fixed linewidth "isolated line." A "nested" line is a MOSFET gate structure with an adjacent parallel gate structure within a given distance (e.g., gate-to-gate spacing less than 10 μm). As the pitch decreases, the "nested-to-isolated" bias increases. For positive tone resist process, the "nested-to-isolated" etch and the photolithographic bias are additive. For negative tone resist process, the "nested-to-isolated" etch and photolithographic bias are subtractive.

Linewidth metrology can determine the linewidth structure. For characterization of the MOSFET linewidth, four-point probe resistor structures with "dummy lines" are measured. To evaluate the change in the linewidth, the linewidth and pitch can be varied to understand the dependency. In Figure 3.5, linewidth distributions were determined using isolated and nested structures for the positive and negative tone processes [31].

The "nested-to-isolated" effect also influences the MOSFET gate conductor sidewall slope. The MOSFET sidewall slope influences the MOSFET effective channel length, and

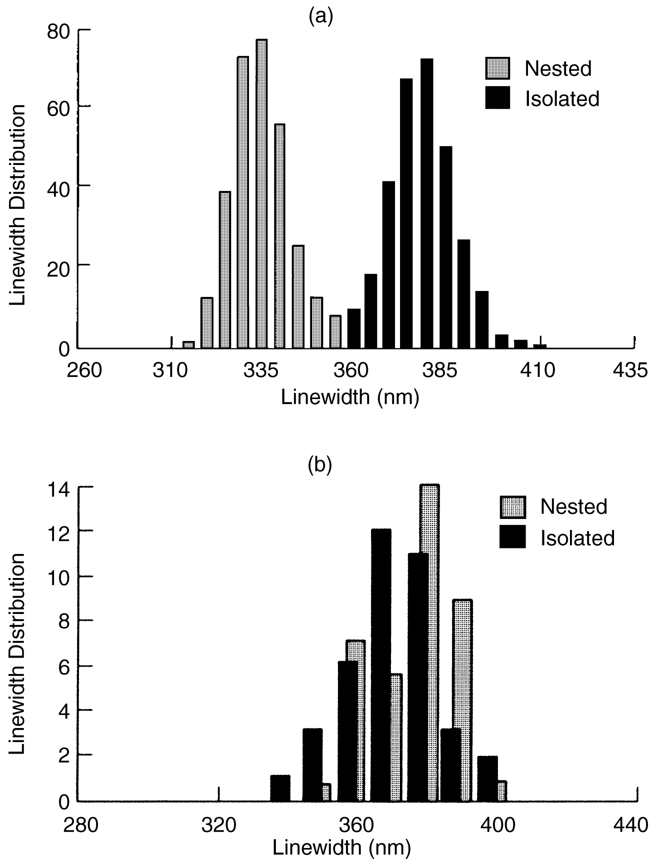

Figure 3.5 (a, b) Positive and negative tone resist linewidth distributions for isolated and nested MOSFET gate structures

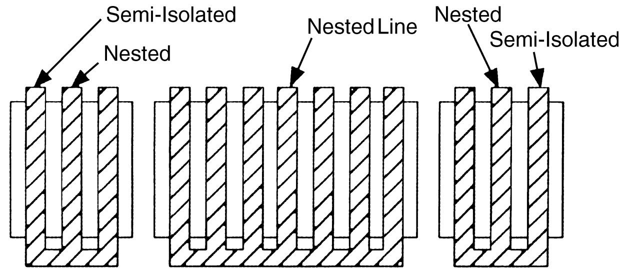

Figure 3.6 MOSFET driver pull-down polysilicon level and source/drain region. The MOSFET is segmented for improved slew rate control

hence the MOSFET snapback voltage. Gate conductor sidewall variations can alter MOSFET second breakdown by influencing the MOSFET source and drain implant profiles in the MOSFET overlap region. The gate conductor sidewall profile is also affected by ARDE, micro-, and macro-loading effects. Using two-dimensional atomic force microscope (2-D AFM) metrology techniques, the sidewall slope can be accurately measured. As the MOSFET gate-to-gate spacing increases, with positive tone resist, the MOSFET sidewall slope decreases. Hence, isolated structures will not only have a higher MOSFET channel length, but will also have a more gradual MOSFET drain doping profile [31].

As an example, an application of a MOSFET OCD network contained an *n*-channel MOSFET pull-down device. The MOSFET pull-down was separated into three segments. During functional operation, to control slew rate, the three segments were driven at different times. The gate structure consisted of a first three-finger MOSFET gate structure, a multi-finger MOSFET gate, and a second three-finger MOSFET gate structure. Figure 3.6 shows a picture of the MOSFET OCD gate structure.

Measurements of the MOSFET polysilicon fingers show that the edge lines of the three-finger MOSFET stages were 0.01 μm larger than the center line. In the ESD measurements, failure analysis consistently showed that the MOSFET failure occurred in three locations. First, the center fingers of the two three-finger structures consistently showed ESD damage during HBM testing. The location of the MOSFET second breakdown damage always occurred in the center finger of the three fingers (Figure 3.7). In the case of the larger multi-finger center structure, damage was typically contained within one of the center fingers in the seven-finger structure, but never the edge MOSFET polysilicon fingers of the center stage. Hence, although many other design features are of concern in ESD MOSFET design, in this implementation, the dominant failure mechanism was driven by the MOSFET ‘‘nested-to-isolated’’ issue.

3.1.3 MOSFET ESD Design Practices

In summary, the MOSFET ESD and I/O design must note the following ESD design issues:

- Orientation of MOSFET ESD elements and MOSFET-based OCDs may be dependent on the *x*–*y* orientation channel length, driven by optical lens distortion. This is most likely in peripheral I/O design.

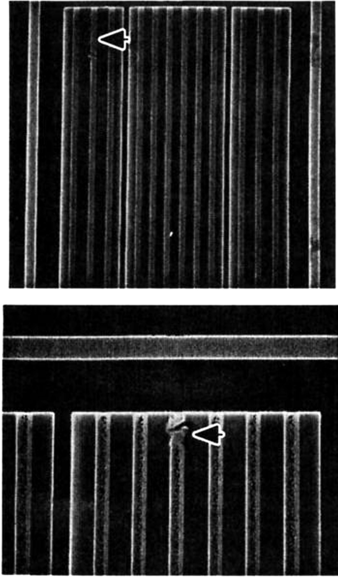

Figure 3.7 Failure analysis of MOSFET with systematic MOSFET second breakdown

- Placement of MOSFET ESD elements and MOSFET-based OCDs on the periphery of the entire chip will be sensitive to optical chip-field variations.
- Multi-finger MOSFETs are sensitive to ‘‘nesting’’ phenomenon; the MOSFET gate-to-gate spacings and the ‘‘nested-to-isolated’’ linewidth variation impact the channel length matching of MOSFET channel lengths.

The following MOSFET ESD design practices can be instituted to provide better MOSFET finger linewidth matching:

- Configure MOSFET OCDs in the same *x–y* orientation if possible to eliminate *x–y* lens distortion effects.
- Place MOSFET OCDs and MOSFET ESD networks locally adjacent to provide improved across chip matching and reduce the effect of the full optical field.
- Provide a fixed gate-to-gate spacing of MOSFET fingers in a given MOSFET network.
- Use an even number of MOSFET polysilicon fingers instead of odd number of fingers (e.g., two instead of three).
- Provide a MOSFET gate-to-gate spacing, which is not in the strong roll-off region of nested-to-isolated bias.
- Place ‘‘dummy MOSFET gate’’ fingers on the edges to eliminate mismatch of the end gate structure to the nested MOSFET fingers.
- Avoid semiconductor processes with high ‘‘nested-to-isolated’’ linewidth mismatch.

- Use semiconductor processes where the MOSFET gate etch and photolithographic bias are subtractive.
- Use thinner polysilicon gate structures (reduces ARDE issues).
- Use negative tone resist instead of positive tone resist.
- Linewidth metrology can be used for MOSFET ESD model development to accurately evaluate the relationship between the true linewidth and the MOSFET snapback condition.

3.2 ESD MOSFET DESIGN: CHANNEL WIDTH

3.2.1 *n*-Channel MOSFET Design: Channel Width

In ESD design, the MOSFET channel width is an important design parameter. The effectiveness of a MOSFET for ESD protection is a function of how the current distributes through the MOSFET structure. The effectiveness of a MOSFET for ESD protection associated with its width is a function of the following design parameters:

- MOSFET source/drain lateral sheet resistance.
- MOSFET silicide resistance.
- MOSFET contact-to-contact spacing.
- MOSFET metal resistance along the MOSFET width.
- MOSFET finger width symmetry (similar or dissimilar lengths).
- MOSFET substrate contact orientation relative to the MOSFET width.
- MOSFET lateral ballasting design.

In the list above, the first four items influence the effective lateral resistance in the MOSFET structure along the MOSFET width. These parameters affect the MOSFET current constriction and the MOSFET second breakdown ESD metric of MOSFET current/unit width (e.g., at the MOSFET second breakdown). Additionally, the MOSFET finger width symmetry finger-to-finger influences the ESD failure. This is most apparent in programmable impedance OCD circuitry. Additionally, the orientation of the substrate contact and lateral ballasting technique influence the current distribution in the MOSFET.

3.3 ESD MOSFET DESIGN: CONTACTS

In ESD design, the microscopic and macroscopic interactions within a MOSFET structure influence the high current operation of a MOSFET. In a MOSFET structure, the placement of the physical contacts influences the ESD robustness. The placement of the MOSFET source and drain contact relative to the MOSFET gate locally influences the current distribution within the physical space. The MOSFET contact-to-contact spacing also defines the current

uniformity at the MOSFET gate edge. The MOSFET contact-to-isolation can influence MOSFET leakage mechanism post-ESD stress. The MOSFET contact on the edge of the MOSFET can influence ESD failure mechanisms at the edges of the MOSFET structure.

3.3.1 Gate-to-Contact Spacing

The MOSFET contact-to-gate spacing locally influences the current uniformity within the MOSFET source and drain junctions [32]. For MOSFET with refractory metal silicide, the current flows through the refractory metal silicide film from the physical contact to the MOSFET gate. Evaluation of the current density within the silicide film provides some insight into the local current distribution and spatial variation in the MOSFET structure. Assuming a two-dimensional plane where the circular contact is placed on a silicide surface, a solution can be obtained.

Using the method of images, let us assume a source and sink at $x = a$ and $x = -a$ equally spaced from a virtual plane perpendicular to the source and sink [33–35]. The x-direction is the direction toward the MOSFET gate structure. Defining a complex variable function,

$$w = -\mu \ln\left(\frac{z-a}{z+a}\right)$$

where the complex variable, z, can be represented in polar coordinates,

$$z - a = r_1 e^{i\theta_2}$$
$$z + a = r_2 e^{i\theta_2}$$

Separating the real and imaginary parts, the complex number z can be represented as a mapping of two harmonic conjugate fields, which satisfy the Cauchy–Riemann equations,

$$z = \phi + i\psi$$

where

$$\phi = \mu \ln\left(\frac{r_1}{r_2}\right)$$
$$\psi = \mu(\theta_1 - \theta_2)$$

Given the source and sink are line charges of a given charge density per unit length, of equal and opposite strengths, $+\lambda$ and $-\lambda$, respectively, the density function can be defined as

$$\mu = \frac{\lambda}{2\pi\varepsilon}$$

In planar coordinates, the harmonic conjugate fields can be represented as

$$\phi(x, y) = -\frac{\lambda}{2\pi\varepsilon} \ln\left[\frac{\sqrt{(a-x)^2 + y^2}}{\sqrt{(a+x)^2 + y^2}}\right]$$
$$\psi(x, y) = -\frac{\lambda}{2\pi\varepsilon}\left[\pi + \tan^{-1}\left(\frac{y}{a-x}\right) - \tan^{-1}\left(\frac{y}{a+x}\right)\right]$$

If we let the first conjugate harmonic field be a constant then the ratio of the first and second radius, r_1 and r_2, is a constant. This can be shown to produce a locus of points that prescribe a circle. Letting the function ϕ be a scalar potential field, the electric field can be represented as minus the gradient of the potential field. Since the natural mapping of this potential field produces circular potential contours, we can represent one of the equi-potentials as a contact with a given radius. Assuming a contact of radius R, we can find the equi-potential surface by finding a first and second point where the ratio of the radii is a constant. Let us define a spacing between the center of the MOSFET contact and the MOSFET gate edge as distance "l". We can now relate the original sink "a" to the MOSFET contact radius, R, and the distance between the center of the contact and the gate edge, "l."

$$\frac{R+l-a}{R+l+a}=\frac{a-(l-R)}{a+(l-R)}$$

where solving for a,

$$a=\sqrt{l^2-R^2}$$

The potential difference between the contact and the image contact can be solved as:

$$V_0=2\left[\frac{\lambda}{2\pi\varepsilon}\ln(r_1/r_2)\right]$$

Substituting in the MOSFET contact radius and the MOSFET gate to contact center point,

$$V_0=-\frac{\lambda}{\pi\varepsilon}\ln\left(\frac{R+l-a}{R+l+a}\right)$$

From the above expression, the solution of the line charge can be represented as a function of the potential difference and the physical dimensions,

$$\lambda=\frac{V_0\pi\varepsilon}{\ln\left\{\frac{l}{R}+\sqrt{\frac{l^2}{R^2}-1}\right\}}$$

The solution of the harmonic conjugate fields, the potential field as well as the electric field, can be obtained,

$$\phi(x,y)=-\frac{V_0}{2\ln\left\{\frac{l}{R}+\sqrt{\frac{l^2}{R^2}-1}\right\}}\ln\left\{\sqrt{\frac{(a-x)^2+y^2}{(a+x)^2+y^2}}\right\}$$

$$\psi(x,y)=-\frac{V_0}{2\ln\left\{\frac{l}{R}+\sqrt{\frac{l^2}{R^2}-1}\right\}}\left\{\pi+\tan^{-1}\left(\frac{y}{a-x}\right)-\tan^{-1}\left(\frac{y}{a+x}\right)\right\}$$

The solution of the vector electric field is obtained by the applying the gradient of the scalar potential field.

$$\vec{E}(x,y) = -\frac{V_0}{2\ln\left\{\frac{l}{R}+\sqrt{\frac{l^2}{R^2}-1}\right\}}\left[\frac{2a(y^2+a^2-x^2)\vec{i}-(4axy)\vec{j}}{\left((a+x)^2+y^2\right)\left((a-x)^2+y^2\right)}\right]$$

To obtain the current density, assuming a uniform conductivity in the silicide film, we can obtain the local current density as [36,37]

$$\vec{J}(x,y) = -\sigma\frac{V_0}{2\ln\left\{\frac{l}{R}+\sqrt{\frac{l^2}{R^2}-1}\right\}}\left[\frac{2a(y^2+a^2-x^2)\vec{i}-(4axy)\vec{j}}{\left((a+x)^2+y^2\right)\left((a-x)^2+y^2\right)}\right]$$

To evaluate the local self-heating between the contact and the MOSFET gate, we can evaluate the product of the current density, J, and the electric field [32,36,37]. Hence, the current density can then be represented as

$$|\vec{J}(x,y)\bullet E(x,y)| = \sigma\frac{V_0^2a^2}{\ln^2\left\{\frac{l}{R}+\sqrt{\frac{l^2}{R^2}-1}\right\}}\left[\frac{1}{(y^2+a^2-x^2)^2+4x^2y^2}\right]$$

Temperature is proportional to the square root of the joule heating, and defining a local temperature as approximately,

$$T(x,y)\propto\sqrt{|\vec{J}(x,y)\bullet E(x,y)|} = \sqrt{\sigma}\frac{V_0a}{\ln\left\{\frac{l}{R}+\sqrt{\frac{l^2}{R^2}-1}\right\}}\left[\frac{1}{(y^2+a^2-x^2)^2+4x^2y^2}\right]^{1/2}$$

From this expression, the temperature field can be evaluated in the x- and y-direction. Additionally, the lateral thermal flux can be evaluated by minus the gradient of temperature.

Addressing the peak self-heating that occurs on the $y=0$ axis. Let $y=0$, this is equal to

$$|\vec{J}(x,y=0)\bullet E(x,y=0)| = \sigma\frac{V_0^2a^2}{\ln^2\left\{\frac{l}{R}+\sqrt{\frac{l^2}{R^2}-1}\right\}}\left[\frac{1}{(a^2-x^2)^2}\right]$$

where

$$a=\sqrt{l^2-R^2}$$

and the contact-to-gate spacing is equal to the distance l minus the contact radius. At the gate edge, $x=0$, we obtain a simplified solution of

$$|\vec{J}(x,y=0)\bullet E(x,y=0)| = \sigma\frac{V_0^2}{a^2\ln^2\left\{\frac{l}{R}+\sqrt{\frac{l^2}{R^2}-1}\right\}}$$

Substituting in for the variable a, we can put it in a form

$$|\vec{J}(x,y=0)\bullet E(x,y=0)|=\sigma\frac{V_0^2}{R^2\left[\left(\frac{l}{R}\right)^2-1\right]\ln^2\left\{\left(\frac{l}{R}\right)+\sqrt{\left(\frac{l}{R}\right)^2-1}\right\}}$$

Let us define a parameter

$$k=\frac{l}{R}=\frac{d+R}{R}$$

where the variable k is a function of the contact-to-gate distance, d, and the radius of the contact, R.

$$|\vec{J}(x,y=0)\bullet E(x,y=0)|=\sigma\frac{V_0^2}{R^2[k^2-1]\ln^2\left\{(k)+\sqrt{(k^2)-1}\right\}}$$

From this expression, it is clear that the self-heating in the silicide film between the contact and the MOSFET gate structure is a function of the parameter k. The parameter k shows the relationship between the center point of the contact and the ratio of the contact size. Hence, the dimensional size of the physical contact and the spacing of the contact to the MOSFET gate structure influence the peak self-heating in the MOSFET structure.

Hence, in the ESD design of contact structures in MOSFETs, the following design parameter is

- The ratio of the sum of the MOSFET contact-to-gate space and the contact radius over the contact radius is a key ESD design parameter in the MOSFET self-heating, where k is expressed as

$$k=\frac{l}{R}=\frac{d+R}{R}$$

3.3.1.1 Off-axis current distribution

To determine the current gradient off-axis, the values off the $y=0$ axis can be evaluated from the current equation. This is obtained by evaluating the derivative of current with respect to the variable y keeping the variable x a constant.

3.3.1.2 Self-heating equi-energy contours

To determine equi-energy contours, the general equation for self-heating can be set to a constant. Setting the expression equal to a constant, C, the solution for the equi-energy potential can be solved as a function of x and y [36,37]. The solution forms a quartic polynomial expression, which is quadratic in y^2.

$$y^4+2y^2x^2+x^4+2a^2y^2+a^2(a^2-4K)=0$$

where K is a function of constant C, and expressed as

$$K = \sigma \frac{V_0^2}{4C \ln^2\left\{ \left(\frac{l}{R}\right) + \sqrt{\left(\frac{l}{R}\right)^2 - 1} \right\}}$$

In quadratic form, the expression can be converted into a canonical form if the coefficients were symmetric, but they are asymmetric. At the position where "a" is much greater than x and y (e.g., at the MOSFET gate edge), the second-order-form terms dominate leaving the approximate expression

$$y^2 - x^2 = a^2 - 4K$$

where K is equal to

$$K = \sigma \frac{V_0^2}{4C \ln^2\left\{ \left(\frac{l}{R}\right) + \sqrt{\left(\frac{l}{R}\right)^2 - 1} \right\}}$$

Near the center point, the locus of points of equi-energy can be expressed as a hyperbolic equation in canonical form. At large distances from the center, the fourth-order terms dominate, producing an equation of a circle,

$$x^2 + y^2 = a\sqrt{4K - a^2}$$

Between the two limits, the locus of points that form equi-energy contours will be elliptical in nature.

In the MOSFET structure, in the region of self-heating, the local temperature is increasing. As the temperature in a titanium silicide film increases, transformations occur in the material properties. Hence in the region of high local self-heating, the silicide property will be altered during ESD events. Failure analysis of MOSFET devices after MOSFET second breakdown shows that the silicide between the MOSFET contact and the MOSFET gate structure changes thermal properties. Using a Wrights' etch, material, which has undergone material property changes due to self-heating, can be highlighted.

Figure 3.8 shows an example of the contour patterns evident in the contact area. Regions of equi-energy contours that undergo heating will be highlighted in the etch process. The failure analysis demonstrates the elliptical equi-energy contours.

3.3.2 Contact-to-Contact Space

In ESD design, the local interactions within a MOSFET structure influence the high current operation of a MOSFET. The MOSFET contact-to-contact spacing also defines the current uniformity at the MOSFET gate edge [38–43].

Between each physical contact in series, there is a physical resistance associated with the metal bussing, the silicide film, and the contacts themselves. The metal bus, the row of contacts, and the diffusion resistance between form a resistive ladder network along the drain

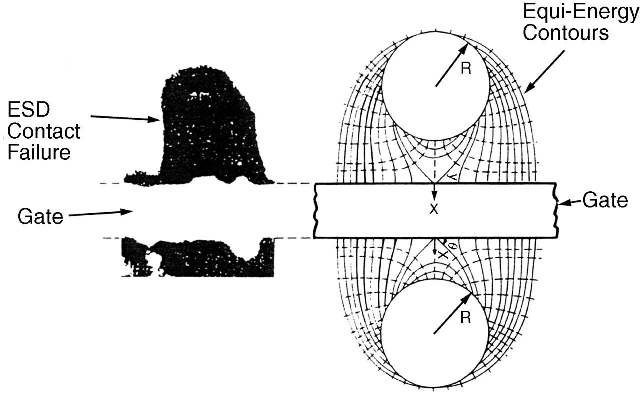

Figure 3.8 Failure analysis of a MOSFET device

and source region. Each incremental section between each physical contact can be treated as a resistive transmission line, where the incrementation is defined by the contact-to-contact spacing.

On a local understanding, as was shown in the analysis of the contact-to-gate spacing, the relative distance between the centroid of the contact to the MOSFET gate, l, and the contact size (e.g., radius R) influences the local current uniformity.

From the analysis, the current in the x- and y-dimension,

$$\vec{J}(x,y) = -\sigma \frac{V_0}{2\ln\left\{\frac{l}{R}+\sqrt{\frac{l^2}{R^2}-1}\right\}}\left[\frac{2a(y^2+a^2-x^2)\vec{i}-(4axy)\vec{j}}{\left((a+x)^2+y^2\right)\left((a-x)^2+y^2\right)}\right]$$

Let us define a new variable where a new contact radius, R, is formed at location $y' = y + b$ and $y'' = y - b$ where the spacing, b, is greater than the contact radius R. Then the current from contact at $y = y - b$ can be expressed as

$$\vec{J}(x,y')\mid_{y'=y-b} = -\sigma \frac{V_0}{2\ln\left\{\frac{l}{R}+\sqrt{\frac{l^2}{R^2}-1}\right\}}\left[\frac{2a\left((y-b)^2+a^2-x^2\right)\vec{i}-(4ax(y-b))\vec{j}}{\left((a+x)^2+(y-b)^2\right)\left((a-x)^2+(y-b)^2\right)}\right]$$

and the current from $y' = y + b$ is

$$\vec{J}(x,y')\mid_{y'=y+b} = -\sigma \frac{V_0}{2\ln\left\{\frac{l}{R}+\sqrt{\frac{l^2}{R^2}-1}\right\}}\left[\frac{2a\left((y+b)^2+a^2-x^2\right)\vec{i}-\left(4ax(y+b)\right)\vec{j}}{\left((a+x)^2+(y+b)^2\right)\left((a-x)^2+(y+b)^2\right)}\right]$$

In the analysis, the current density is shifted relative to the axis of symmetry for each physical contact. When the contact-to-contact spacing is significantly larger than the contact-to-gate and radius of the contact, each solution of the current density will appear independent. If we can assume linear superposition, the net current density along the axis will be the sum of the current source. As the spacing of the contact-to-contact become on the

same scale as the contact-to-gate distance and contact radius, the current at the MOSFET gate surface will become more uniform.

From the above expression, we can normalize the solution to the parameter a, and the contact-to-contact space parameter b.

In the case of $y = 0$, it is clear that the solution can be put in the form of the ratio of the parameter a, and the contact-to-contact space parameter b. For example,

$$\vec{J}(x, y') \mid_{y'=y+b} = -\sigma \frac{V_0}{2 \ln\left\{\frac{l}{R} + \sqrt{\frac{l^2}{R^2} - 1}\right\}} \left[\frac{2a\left((b)^2 + a^2 - x^2\right)\vec{i} - \left(4ax(b)\right)\vec{j}}{\left((a+x)^2 + (b)^2\right)\left((a-x)^2 + (b)^2\right)}\right]$$

At the gate surface, let $x = 0$, we obtain

$$\vec{J}(x = 0, y') \mid_{y'=y+b} = -\sigma \frac{V_0}{2 \ln\left\{\frac{l}{R} + \sqrt{\frac{l^2}{R^2} - 1}\right\}} \left[\frac{2a\vec{i}}{(a^2 + b^2)}\right]$$

or

$$\vec{J}(x = 0, y') \mid_{y'=y+b} = -\sigma \frac{V_0}{2 \ln\left\{\frac{l}{R} + \sqrt{\frac{l^2}{R^2} - 1}\right\}} \left[\frac{2\vec{i}}{a\left(1 + \left(\frac{b}{a}\right)^2\right)}\right]$$

Hence, the solution of the current density at $x = 0$ and $y = 0$ from the contact at $y = b$ is a function of the contact-to-contact space, the contact radius R, and the MOSFET gate-to-contact spacing. Additionally, the influence of the contact on its adjacent contact is a function of the ratio of a second ratio term, which we can refer to as k_2

$$k_2 = \frac{b}{a} = \frac{b}{\sqrt{l^2 - R^2}} = \frac{b}{\sqrt{(d+R)^2 - R^2}}$$

where we define the first parameter as

$$k_1 = \frac{l}{R} = \frac{d+R}{R}$$

As an ESD MOSFET design guideline, we can state the following:

- A first ESD design parameter, which defines the current uniformity from a single contact, is associated with the gate-to-contact spacing, and the contact radius

$$k_1 = \frac{l}{R} = \frac{d+R}{R}$$

- A second ESD design parameter, which defines the current uniformity due to a plurality of contacts, is a function of the gate-to-contact spacing, the contact radius, and the

contact-to-contact spacing,

$$k_2 = \frac{b}{a} = \frac{b}{\sqrt{l^2 - R^2}} = \frac{b}{\sqrt{(d+R)^2 - R^2}}$$

- A ESD design parameter, which inter-relates the two metrics, can be referred as k_3 stated as

$$k_3 = \frac{k_1}{k_2}.$$

During ESD events, as the contact-to-contact spacing decreases, the current uniformity along the MOSFET gate surface improves. In many applications, the contact-to-contact spacing is equal to the size of the physical contact at minimum pitch. If we define the contact-to-contact space as the center-to-center value, b, the physical separation is actually $b - 2R$. Hence, in practice, the distance between the two contacts is $b - 2R$ that equals the diameter of the contact, or $b - 2R = 2R$, or $b = 4R$.

$$(k_2)_{\min} = \frac{4R}{a} = \frac{4R}{\sqrt{l^2 - R^2}} = \frac{4R}{\sqrt{(d+R)^2 - R^2}}$$

On a higher level, between each physical contact in series, there is a physical resistance associated with the metal bussing, the silicide film, and the contacts themselves. The metal bus, the row of contacts, and the diffusion resistance between form a resistive ladder network along the drain and source region. Each incremental section between each physical contact can be treated as a resistive transmission line. In a method by DeChairo [42] and G. Krieger [43], the analysis is discussed as a resistive transmission line. In the higher order model, there are two resistance parameters, one representing the contact-to-contact resistance associated with the metal, diffusion, and silicide, and a second resistance parameter associated with the on-resistance of the MOSFET during conduction. In their analyses, a design parameter associated with the lateral resistance and the MOSFET device resistance solves the characteristic equation. In our analysis, a design parameter is present relating the dimensional similitude of the lateral spacing contact-to-contact, a series term of the contact to the MOSFET gate, and a third parameter, the contact size (Figure 3.9). Note that the

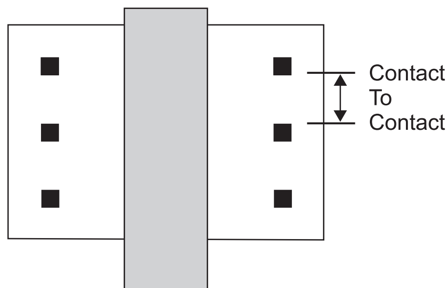

Figure 3.9 Contact-to-contact

current density term is related to a resistance term, related to the local spreading resistance between a first point (source) and a second point (image sink) in a two-dimensional plane, where the first point has a finite radius.

3.3.3 End Contact

Placement of the MOSFET contacts near the end of the MOSFET structure can lead to MOSFET contact ESD failure due to high-current phenomenon from the semiconductor substrate region [38–41]. Given a CDM event, current can flow from the substrate to the grounded node of the MOSFET structure. In the case of a grounded MOSFET gate structure, the current will flow through the MOSFET gate dielectric due to $C\,(\mathrm{d}V/\mathrm{d}t)$ effects. In a CDM event where the MOSFET diffusion is connected to the grounded input node, current will flow from the chip substrate to the input node. In a receiver network, an *n*-channel MOSFET half-pass element will have one diffusion connected to the receiver and the second connected to the input pad. In this case, C. Duvvury stated that the current flowing laterally from the MOSFET drain structure will have a higher current density and flow to the first physical contact on the MOSFET drain [38]. In this case, the first contact in the substrate will obtain a higher current density than adjacent contacts leading to MOSFET failure (Figure 3.10). This is analogous to the three-dimensional effect observed in p^+/n-well diode structures from positive polarity ESD events [32]. ESD design practice to reduce this effect is as follows:

- The MOSFET contact at the beginning and at the end of the MOSFET diffusions are spaced from the end of the physical diffusion at a greater distance than the minimum spacing.

3.3.4 Contacts to Isolation Edge

Placement of the MOSFET contacts near the MOSFET source and drain isolation structure can lead to reliability concerns. This is to avoid LOCOS isolation bird's beak and/or STI pull-down, influencing the MOSFET effective junction depth. The MOSFET contact is spaced from the MOSFET drain and source isolation edge to avoid the process sensitivity

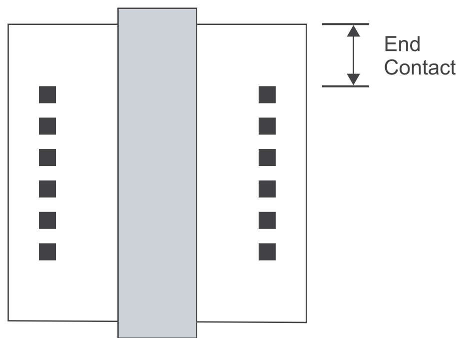

Figure 3.10 MOSFET end contact issue

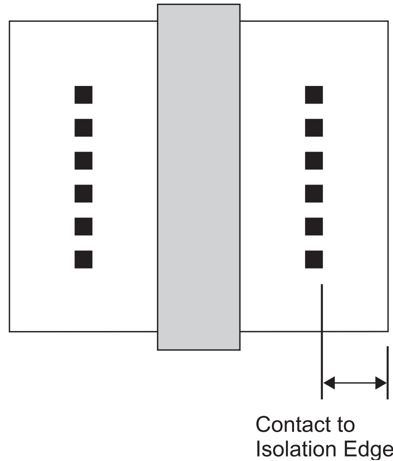

Figure 3.11 Contact to isolation edge

issues. As a conservative measure, the placement of contacts relative to the MOSFET source and drain isolation edges is spaced above a minimum design dimension [38].

ESD design practice to reduce the effect of contact-to-isolation effect is as follows:

- The MOSFET contact is spaced from the MOSFET drain and source isolation edge (Figure 3.11). This is to avoid LOCOS isolation bird's beak and/or STI pull-down, influencing the MOSFET effective junction depth and current crowding issues [30].

3.4 ESD MOSFET DESIGN: METAL DISTRIBUTION

3.4.1 MOSFET Metal Bus Design and Current Distribution

The layout design and resistances of a single- and multi-finger MOSFET have significant influence on the ESD robustness of the structure [38]. Typically, signal pins, I/O pins, and output-only pins consist of large multi-finger MOSFET circuit elements, which are defined by the I/O foot print and pad-to-pad pitch. Additionally, ESD networks use multi-finger layout configurations. The current distribution through these elements have significant influence on the ESD robustness.

3.4.2 MOSFET Ladder Network Model

An early model analyzed this effect as a resistive ladder network [42]. DeChairo assumed during avalanche breakdown that each MOSFET source-to-drain region can be analyzed as a simple single resistor element, R_1. The resistor R_1 represents the total resistance across a single-finger MOSFET structure from the drain to the source. In this model, it is assumed that the resistance value R_1 is time invariant during an ESD event. In the ‘‘comb’’ structure, the metal routing from a finger-to-finger was assumed to be a second resistor R_2 (e.g., the metal connection between each adjacent finger). Figure 3.12 shows the multi-finger MOSFET represented as a resistive ladder network.

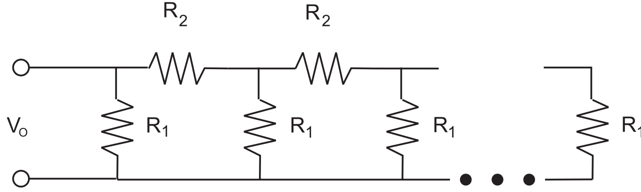

Figure 3.12 Multi-finger MOSFET ladder network model

In this ladder network, the left-hand side (LHS) has a voltage source that supplies the incoming current to the distributed ladder network. In this model, the lower source connections is at the same electrical potential with no resistive elements on the lower part of the ladder network.

Using Kirchoff's current law, the solution for the *i*th current loop can be solved as

$$(2R_1 + R_2)I_i - R_1 I_{i-1} + R_1 I_{i+1} = 0$$

For N current loops, there exists N equations of this form. The set of N equations can be represented in a matrix equation form consisting of a generalized $N \times N$ resistance matrix, a current column vector, and a "zero" column vector.

$$R^* I = 0$$

where

$$I = (I_0, I_1, \ldots, I_N)$$

and the tri-diagonal matrix is given by

$$R = \begin{bmatrix} 2R_1 + R_2 & -R_1 & 0 & 0 & \bullet & \bullet & \bullet & 0 \\ -R_1 & 2R_1 + R_2 & -R_1 & 0 & & & & \bullet \\ 0 & -R_1 & 2R_1 + R_2 & -R_1 & & & & \bullet \\ 0 & 0 & -R_1 & 2R_1 + R_2 & & & & \bullet \\ 0 & 0 & 0 & & \bullet & & 0 & \bullet \\ \bullet & & & & & \bullet & -R_1 & 0 \\ \bullet & & & & 0 & -R_1 & 2R_1 + R_2 & -R_1 \\ 0 & \bullet & \bullet & \bullet & \bullet & 0 & -R_1 & 2R_1 + R_2 \end{bmatrix}$$

In this matrix, the term $2R_1 + R_2$ is on the main diagonal, and R_1 is on the off-diagonal terms, which are adjacent to the main diagonal.

The solution to this matrix is achieved by defining two recursion coefficients X_j and Y_j, which satisfies the relation

$$I_{j+1} = X_j I_j + Y_j$$

At the end of the ladder network, only the Nth and $(N-1)$th current terms exist, simplifying the Nth loop equation to

$$(2R_1 + R_2)I_N - R_1 I_{N-1} = 0$$

rearranging the terms

$$I_N - \frac{R_1}{(2R_1 + R_2)} I_{N-1} = 0$$

From the above recursive relationship, letting $j = N - 1$,

$$I_N = X_{N-1} I_{N-1} + Y_{N-1}$$

where the recursive relation is put in the form

$$I_N - X_{N-1} I_{N-1} - Y_{N-1} = 0$$

From this

$$X_{N-1} = \frac{R_1}{(2R_1 + R_2)}$$
$$Y_{N-1} = 0$$

Once the boundary condition is established for the $(N - 1)$th loop, the recursive coefficients can be solved for each of the current loop terms. This is achieved by resubstituting the recursive coefficient equation into the current loop equation.

The recursive coefficient equation can be substituted into the current loop equation for the ith loop. From this, a general expression for the recursive coefficient can be obtained

$$X_i = \frac{R_1}{(2R_1 + R_2 - R_1 X_{i+1})}$$
$$Y_i = \frac{R_1 Y_{i+1}}{(2R_1 + R_2 - R_1 X_{i+1})}$$

In this double-recursive solution form, the current distribution through the network can be obtained. A key result from the analysis is that the recursive coefficients are a function of the first and second resistor values.

As a special case, let us assume that the finger-to-finger resistance R_2 is significantly larger than on-resistance of the MOSFET device. Let $R_2 \gg R_1$

$$X_{N-1} \cong \frac{R_1}{R_2}$$
$$Y_{N-1} = 0$$

From the boundary condition, the ratio of the two resistances plays a role in the characteristic solution; and the recursive coefficients can be approximated as

$$X_i \cong \frac{R_1}{(R_2 - R_1 X_{i+1})}$$
$$Y_i \cong \frac{R_1 Y_{i+1}}{(R_2 - R_1 X_{i+1})}$$

(where again it can be observed that the ratio of the resistance plays a role in the solution). Hence, the ratio of the resistance of the metal interconnect relative to the MOSFET device source-to-drain resistance (during ESD operation) is critical to the understanding of how the current is distributed throughout the network. This fact is also apparent in the Krieger model of parallel and anti-parallel current flow within a single finger [43]. The form and nature of the coefficient is a function of the assumptions used in the ladder network representation.

In the case that the value of resistance R_2 is much less than R_1, then

$$X_{N-1} = \lim_{R_2 \to 0} \frac{R_1}{(2R_1 + R_2)} = \frac{1}{2}$$

$$X_i = \lim_{R_2 \to 0} \frac{R_1}{(2R_1 + R_2 - R_1 X_{i+1})} = \frac{1}{(2 - X_{i+1})}$$

$$Y_i = \lim_{R_2 \to 0} \frac{R_1 Y_{i+1}}{(2R_1 + R_2 - R_1 X_{i+1})} = \frac{Y_{i+1}}{(2 - X_{i+1})}$$

DeChairo established a metric expression to compare the performance of a single-finger MOSFET to the multi-finger implementation [42]. Opening the comb structure where only current flows through the first element, the current can be expressed as

$$I_0 = \frac{V_0}{R_1}$$

With the full network connected, the difference in the resistance between a single-finger MOSFET and a multi-finger MOSFET can be evaluated as

$$I = I_0 - I_1 = I_0(1 - X_0)$$

DeChairo defined an ESD enhancement factor (EEF), where

$$EEF = \frac{1}{1 - X_0}$$

The EEF metric expression is the enhancement of a multi-finger MOSFET over a single-finger MOSFET. To quantify the ESD roll-off in the multi-finger structure, DeChairo evaluated different cases of the resistance ratio of the metal resistance to the n^+ sheet resistance. In the case that the metal resistance approaches zero (e.g., $R_2 \lll R_1$), the ESD results with increasing structure size should increase linearly. In the opposite limit where the metal resistance is infinite, (e.g., $R_2 \ggg R_1$), current does not flow into the multiple-finger segments beyond the first finger. In this case, as the number of fingers increases, the ESD results do not increase (i.e., they are independent of the number of fingers). In the limit that the finger-to-finger metal resistance approaches zero, the ESD results will increase in a linear fashion with structure size. In the case where the resistance of the metal is significantly higher than the MOSFET resistance, no increase in the ESD results occurs.

Hence, a design curve can be drawn of ESD failure results versus structure size, where the design box is constrained to a triangular region whose upper limit is the linear scaling line with structure size (e.g., MOSFET width) and the lower limit is the ESD failure result for a single-finger structure. Actual measurements will fall within this design curve region. In the

design of a multi-finger MOSFET structure, the ideal case is to have the results approach the upper bound of the design box. As the ratio of the metal resistance to MOSFET source-to-drain resistance decreases, the upper bound of the design box is approached.

3.4.3 MOSFET Wiring: Anti-Parallel Current Distribution

In a MOSFET structure, the local distribution of the ESD current is strongly influenced by the metal routing [43]. The metal routing influences which part of the MOSFET structure will undergo MOSFET snapback or MOSFET second breakdown.

During an ESD event, for example, the current flows into the MOSFET drain metal line, from MOSFET drain-to-source and out the MOSFET source metal line. The electrical connection to the MOSFET source and drain can be on the same or the opposite sides. In the case where the current is flowing in the same direction, it will be referred to as parallel current flow (e.g., enters and exits on opposite ends of the MOSFET structure). In the case, where the current is flowing in opposite directions, it will be referred to as anti-parallel current flow (e.g. enters and exits on the same end of the MOSFET structure) (Figure 3.13).

An incremental model can be established that quantifies the voltage distribution within the MOSFET structure. Krieger proposed that we establish an incremental model, where each contact defines an electrical node and each region between each contact to be modeled

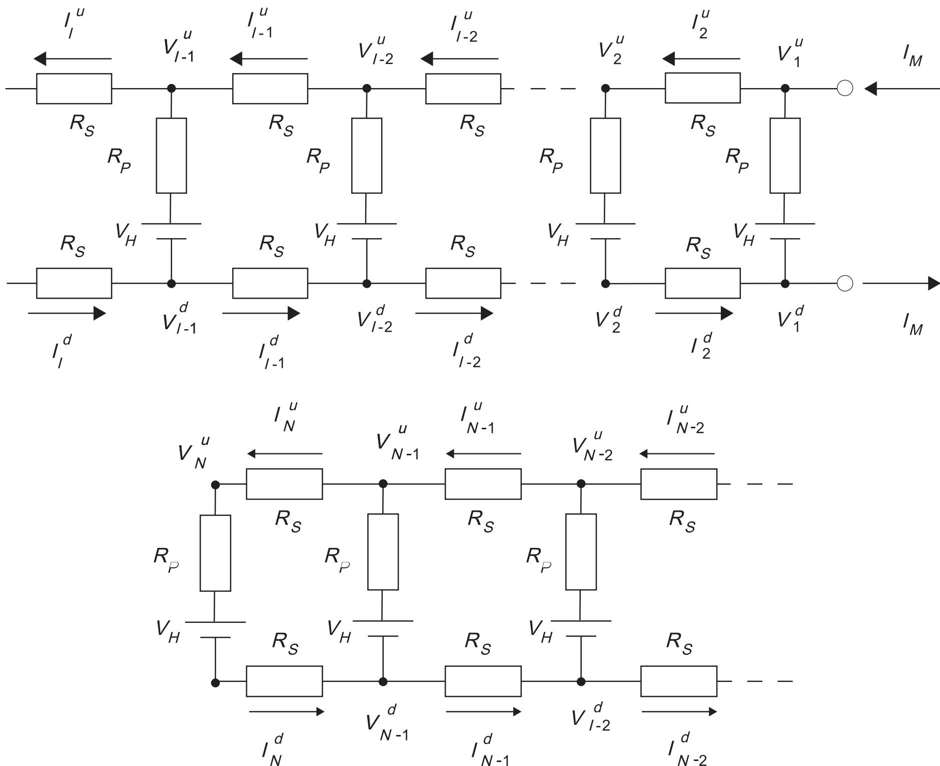

Figure 3.13 MOSFET wiring with anti-parallel current flow

as a resistor element [43]. Krieger proposed to best understand the MOSFET during second breakdown; a distributed model is established based on the holding voltage, the dynamic-on resistance, and the metal resistance. During the MOSFET snapback, the MOSFET goes through an unstable negative resistance state and settles into the holding state. The holding state is the lowest voltage and lowest current point where stability is re-established. Krieger defined a network, where the lateral resistance between each physical contact can be defined as a resistor R_s. The MOSFET is represented as a voltage source V_H (whose magnitude is the holding voltage) and a local term R_p, which represents the dynamic-on resistance R_d divided by the number of electrical nodes along the electrical network. In this fashion, the MOSFET structure is re-represented as a resistive ladder network with a voltage source between the upper and lower segments of the ladder network.

To solve for the solution of the voltage distribution in the MOSFET structure, the boundary conditions must be established. In the case of the anti-parallel current flow, we can establish a boundary condition that the metal lines are "open" on the left-hand side (LHS), and the electrical connections on the right-hand side (RHS) is the source of incoming current and outgoing current. For current conservation, the incoming current in the drain is equal to the outgoing source current.

In the network, it is assumed that the wire resistance of the MOSFET drain and that of source is equal in magnitude, and the contact density is the same. In this fashion, the MOSFET can be divided into equal segments on the upper and lower regions. Along the top and bottom of the network, the regions are segmented with resistors R_s. Between the upper and lower parts of the circuit network, they are electrically connected using resistor R_p and voltage source V_H. Since the current flow is symmetrical for each incremental segment, Krieger noted that the analysis of the anti-parallel routing can establish a line of symmetry [43]. A virtual line of symmetry is established, which divides the voltage source and the resistor by a factor of 2. This is analogous to the method of images, where an image is established around an equi-potential (Figure 3.13). The equi-potential line of symmetry has a zero voltage reference point, and can be at ground potential. From this form, the voltage drop from the first contact to the second contact is the current flowing through that increment times the resistance drop

$$V_i - V_{i-1} = -I_i R_s$$

The current loss between the first and second increment is associated with the

$$V_i - \frac{V_H}{2} = \frac{R_p}{2}\left(I_i - I_{i-1}\right)$$

which can be expressed as

$$I_i - I_{i-1} = -\frac{2}{R_p}\left(V_i - \frac{V_H}{2}\right)$$

Using the differential voltage drop and the differential current drop expressions, Krieger showed that this network can be represented as a second order finite difference equation in the form,

$$\left(V_i - (2+k)\,V_{i-1} + V_{i-2}\right) - \frac{kV_H}{2} = 0$$

and defining

$$k = \frac{2R_s}{R_p}$$

An important aspect of the equation is that the ratio of the incremental interconnect series resistance and the incremental dynamic resistance, which influences the roots and solution values of the network. Hence, the relative magnitude of the two elements is critical to determine the voltage distribution. The characteristic resistance ratio, k, has a significant role. Hence, in ESD MOSFET design, the relative magnitude of characteristic resistance ratio should be a key metric expression.

The solution to the second-order finite difference equation can be expressed as a general set of solutions, where there exists a solution for the voltage at each incremental point

$$V_i = a(\lambda_1)^i + b(\lambda_2)^i + \frac{V_H}{2}$$

which can be expressed as two roots of the solution,

$$\lambda_1 = 1 + \frac{k}{2}\left(1 + \sqrt{1 + \frac{4}{k}}\right)$$
$$\lambda_2 = 1 + \frac{k}{2}\left(1 - \sqrt{1 + \frac{4}{k}}\right)$$

and two constants. The constants, a and b, are a function of the boundary condition. In this method, the boundary condition assumes symmetry of the incoming and outgoing current. From the Kirchoff's nodal current rule at the boundary,

$$\frac{2V_1 - V_H}{R_p} + \frac{V_1 - V_2}{R_s} = I_1 = I_m$$
$$(2V_n - V_H)(1 + k) + V_H = 2V_{n-1}$$

Substitution of the general nodal solution for the case of the first and nth nodal point, the solution for the constants a and b are as follows

$$a = \frac{1}{[X - Y]} I_m R_s \left\{\lambda_2^{n-1}[1 - \lambda_2(1 + k)]\right\}$$
$$b = -\frac{1}{[X - Y]} I_m R_s \left\{\lambda_1^{n-1}[1 - \lambda_1(1 + k)]\right\}$$
$$X = \lambda_2^{n-1}[1 - \lambda_1][1 - \lambda_2(1 + k)]$$
$$Y = \lambda_1^{n-1}[1 - \lambda_2][1 - \lambda_1(1 + k)]$$

As the current flows from the first increment to the last increment, the voltage drop continues along the entire length. The first point, which undergo MOSFET second breakdown, will be the point where the current enters (e.g., the first nodal point). As the voltage increases, the region of the MOSFET where the voltage is above MOSFET breakdown propagated down the metal routing.

From an ESD perspective, this is the worst case routing for providing utilization of the MOSFET structure. Yet, as the characteristic resistance ratio k approaches zero, the method of routing does not limit the ESD robustness and current distribution. Hence, in the ESD design, the routing solution and its success are a function of the characteristic resistance ratio, k.

3.4.4 MOSFET Wiring: Parallel Current Distribution

As discussed in the section on MOSFET current distribution, the local distribution of the ESD current is strongly influenced by the metal routing [42,43]. During an ESD event, for example, the current flows into the MOSFET drain metal line, from MOSFET drain-to-source and out the MOSFET source metal line. The electrical connection to the MOSFET source and drain can be on the same side or opposite sides. In the case where the current is flowing in the same direction, will be referred to as parallel current flow (e.g., enters and exits on opposite ends of the MOSFET structure.

An incremental model can be established that quantifies the voltage distribution within the MOSFET structure for the case of the parallel configuration [43] (Figure 3.14). Using the same model as the anti-parallel case, the solution can be obtained, but due to the asymmetry of the system, the solution is more difficult.

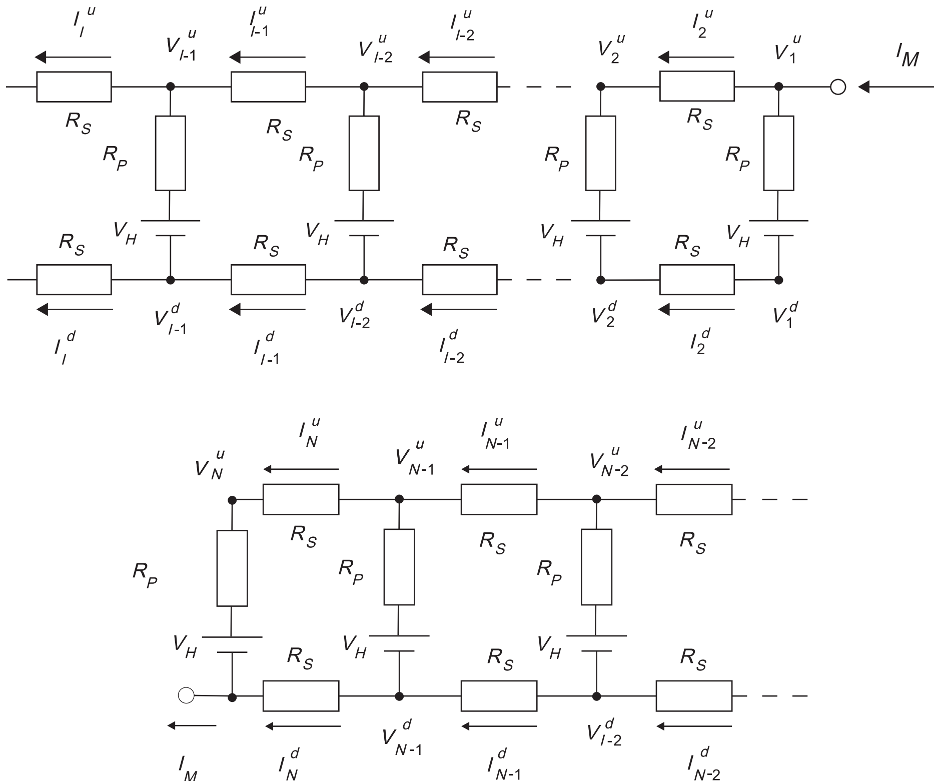

Figure 3.14 (a,b) MOSFET with parallel current flow

Again, Krieger proposed that we establish an incremental model, where each contact defines an electrical node, and each region between each contact to be modeled as a resistor element [43]. Krieger defined a network, where the lateral resistance between each physical contact can be defined as a resistor R_s. The MOSFET is represented as a voltage source V_H (whose magnitude is the holding voltage) and a local term R_p, which represents the dynamic-on resistance R_d divided by the number of electrical nodes along the electrical network. In this fashion, the MOSFET structure is re-represented as a resistive ladder network with a voltage source between the upper and lower segment of the ladder network.

To solve for the solution of the voltage distribution in the MOSFET structure, the boundary conditions must be established. In the case of the parallel current flow, establishing a boundary condition, that the current flows out the bottom of the left-hand side (LHS), and the electrical connections on the right-hand side (RHS) is the source of incoming current. For current conservation, the incoming current in the drain is equal to the outgoing source current.

In the network, it is assumed that the wire resistance of the MOSFET drain and that of the source are equal in magnitude, and the contact density is the same. In this fashion, the MOSFET can be divided into equal segments on the upper and lower regions. Along the top and bottom of the network, the regions are segmented with resistors R_s. Between the upper and lower parts of the circuit network, they are electrically connected using resistor R_p and voltage source V_H.

Incrementally, the voltage drop from the upper node to the lower node is equal to the voltage drops across the network at a node. The current flowing through that nodal point is the current, which is not flowing down the upper region

$$V_{i-1}^{u} - V_{i-1}^{d} = \left(I_{i-1}^{u} - I_{i}^{u}\right)R_{\mathrm{p}} + V_{\mathrm{H}}$$

This can also be represented as the current not flowing between two sequential contacts on the lower segment of the structure,

$$V_{i-1}^{u} - V_{i-1}^{d} = \left(I_{i-1}^{d} - I_{i}^{d}\right)R_{\mathrm{p}} + V_{\mathrm{H}}$$

additionally, the voltage drops along the metal line can be represented by the current flowing down the upper and lower wiring times the resistance drop

$$V_{i-1}^{u} - V_{i}^{u} = \left(I_{i}^{u}\right)R_{\mathrm{s}}$$
$$V_{i-1}^{d} - V_{i-1}^{d} = \left(I_{i}^{d}\right)R_{\mathrm{s}}$$

Using the above four expressions, we can solve for the respective voltage drops from the upper to lower segment as a function of the currents and resistances

$$2\left(V_{i-1}^{u} - V_{i-1}^{d}\right) - 2V_{\mathrm{H}} = \left\lfloor\left(I_{i-1}^{u} - I_{i-1}^{d}\right) - \left(I_{i}^{u} - I_{i}^{d}\right)\right\rfloor R_{\mathrm{p}}$$

as well as the voltage differentials associated with the current differences

$$\left(V_{i-1}^{u} - V_{i-1}^{d}\right) - \left(V_{i}^{u} - V_{i}^{d}\right) = \left\lfloor\left(I_{i}^{u} - I_{i}^{d}\right)\right\rfloor R_{\mathrm{s}}$$

For simplicity, the following values are defined as

$$\left(V_{i}^{u} - V_{i}^{d}\right) \equiv V_{i}$$
$$\left(I_{i}^{u} - I_{i}^{d}\right) \equiv I_{i}$$

and redefine the above equations as

$$2(V_{i-1}) - 2V_{\mathrm{H}} = \lfloor (I_{i-1} - I_i) \rfloor R_{\mathrm{p}}$$
$$(V_{i-1} - V_i) - 2V_{\mathrm{H}} = I_i R_{\mathrm{s}}$$

Krieger showed that this can be expressed as a second-order finite difference equation similar to the anti-parallel case

$$(V_i - 2(1+k)\, V_{i-1} + V_{i-2}) - 2kV_{\mathrm{H}} = 0$$

and defining

$$k = \frac{R_{\mathrm{s}}}{R_{\mathrm{p}}}$$

As in the anti-parallel case, the characteristic term in the parallel wiring configuration equation is the characteristic resistance ratio term. Note that there is a difference of a factor of 2 compared to the prior definition of the characteristic resistance term [43]. Again, a general solution can be formed as

$$V_i = a(\lambda_1)^i + b(\lambda_2)^i + V_{\mathrm{H}}$$

which can be expressed as two roots of the solution

$$\lambda_1 = 1 + k\left(1 + \sqrt{1 + \frac{2}{k}}\right)$$
$$\lambda_2 = 1 + k\left(1 - \sqrt{1 + \frac{2}{k}}\right)$$

In order to solve for the coefficients a and b, the boundary conditions must be solved.

$$2(V_1^u - V_1^d) - 2V_{\mathrm{H}} = 2\lfloor (I_2^d) \rfloor R_{\mathrm{p}}$$
$$2(V_1) - 2V_{\mathrm{H}} = \lfloor (I_2^u - I_2^d) - (I_2^u - I_2^d) \rfloor R_{\mathrm{p}}$$
$$2(V_1) - 2V_{\mathrm{H}} = \lfloor (I_m - I_2) \rfloor R_{\mathrm{p}}$$
$$(V_1^u - V_2^u) - (V_1^d - V_2^d) = V_1 - V_2 = \lfloor (I_2^u - I_2^d) \rfloor R_{\mathrm{s}}$$
$$V_n^d \equiv 0 \rightarrow V_n^u = V_n$$
$$V_n^u + \frac{V_n^u - V_{\mathrm{H}}}{R_{\mathrm{p}}} R_{\mathrm{s}} = \left[I_m - \frac{V_n^u - V_{\mathrm{H}}}{R_{\mathrm{p}}} \right] R_{\mathrm{s}} + V_{n-1}$$
$$V_2 - (1+2k)V_1 + 2kV_2 + I_m R_{\mathrm{s}} = 0$$
$$V_n(1+2k) - V_{n-1} - 2kV_{\mathrm{H}} - I_m R_{\mathrm{s}} = 0$$
$$a = \frac{1}{[U-V]} I_m R_{\mathrm{s}} \{ \lambda_2[(1+2k) - \lambda_2] - \lambda_2^{n-1}[\lambda_2(1+2k) - 1] \}$$
$$b = \frac{1}{[U-V]} I_m R_{\mathrm{s}} \{ \lambda_1[\lambda_1 - (1+2k)] + \lambda_1^{n-1}[\lambda_1(1+2k) - 1] \}$$
$$U = \lambda_1 \lambda_2^{n-1}[\lambda_1 - (1+2k)][\lambda_2(1+2k) - 1]$$
$$V = \lambda_2 \lambda_1^{n-1}[(1+2k) - \lambda_2][\lambda_1(1+2k) - 1]$$

3.5 ESD MOSFET DESIGN: SILICIDE MASKING

3.5.1 Silicide Mask Design

In the ESD design practice, resistor ballasting is introduced into MOSFET structures to prevent MOSFET second breakdown [38]. MOSFET resistor ballasting has two roles:

- Introduction of MOSFET series resistance.
- Introduction of MOSFET lateral resistance.

The MOSFET series resistance serves a first purpose of limiting the current in a MOSFET during ESD events. The role of the series resistance establishes a current limit through the MOSFET structure. In the case that the MOSFET has an ESD element in a parallel ESD current loop, the voltage drop incurred by the series resistance allows for the current to flow through the ESD current loop, buffering the MOSFET network, as well as establishing an increase in the voltage margin of ESD network operation prior to MOSFET failure.

A second aspect is the introduction of MOSFET lateral resistance. The introduction of MOSFET lateral resistance provides lateral ballasting. This is a second ESD design practice of utilization of the MOSFET width by improving the MOSFET "effective width." Current constriction occurs during self-heating in the MOSFET source and drain regions. With the introduction of lateral ballasting, lateral current flow is minimized.

Refractory metal are deposited on MOSFET source, drain, and gate regions to lower the MOSFET series resistance for improved MOSFET functionality. The refractory metal is deposited on the silicon surface forming a silicide compound. The silicide lowers the series resistance of the MOSFET source, drain, and gate significantly enough to lower the ESD robustness of the semiconductor device. The silicide formation is self-aligned to the MOSFET physical regions, and is commonly referred to as self-aligned silicide or salicide. A second aspect is that the low-resistance silicide film is in parallel with the MOSFET silicon diffusion. Given the resistance is significantly lower than the silicon region, the majority of the current flow is contained within the silicide film, leading to high current densities in the silicide film. A third ESD aspect is that the silicide consumes the silicon atoms and forms close to source and drain metallurgical junction; this can lead to a lowering of the MOSFET ESD robustness due to silicide penetration. During ESD events, the MOSFET drain region undergoes self-heating. The peak local temperature in the MOSFET drain region can lead to refractory metal penetration to the metallurgical junction. This will lead to physical failure and leakage. Additionally, the presence of LOCOS or STI triple points (e.g., between the silicide, the silicon junction, and isolation structure) can lead to MOSFET ESD failure [30].

A technique to improve the MOSFET ESD robustness is to eliminate the self-aligned nature of the silicide formation, and place it in regions that provide ESD advantages and eliminate ESD disadvantages. Silicide is an advantage under the contacts to provide good ohmic contacts between the silicide film and the silicon surface. Silicide is also important on the MOSFET gate structure in the case of MOSFET structures that have narrow channels and long MOSFET widths (e.g., MOSFET OCD driver structures). The locations where silicide is a disadvantage are the MOSFET source and drain region between the MOSFET contact and gate region, and MOSFET isolation edges.

3.5.2 Silicide Mask Design Over Source and Drain

Figure 3.15 (a) shows an example of the MOSFET structure with a silicide block mask on the MOSFET source and drain regions. In this ESD design practice, the silicide is formed under the MOSFET contacts and near the MOSFET gate structure but not in the center region of the MOSFET. The advantage of this design practice is that good contact resistance is established in the MOSFET structure. The second advantage is the MOSFET polysilicon gate sheet resistance is maintained. The disadvantage of this implementation is that space is required between the silicide mask and the MOSFET gate mask; between the two regions there exists a small region of salicide in the overlay space. An issue exists in this implementation with some forms of refractory metals. In the case of titanium silicide, as the area decreases, the probability of transformation from the high-resistance phase state to the low-resistance state phase decreases [30]. Hence, the physical area and the transformation probability introduces uncertainty in the nature of the silicide and lateral resistance near

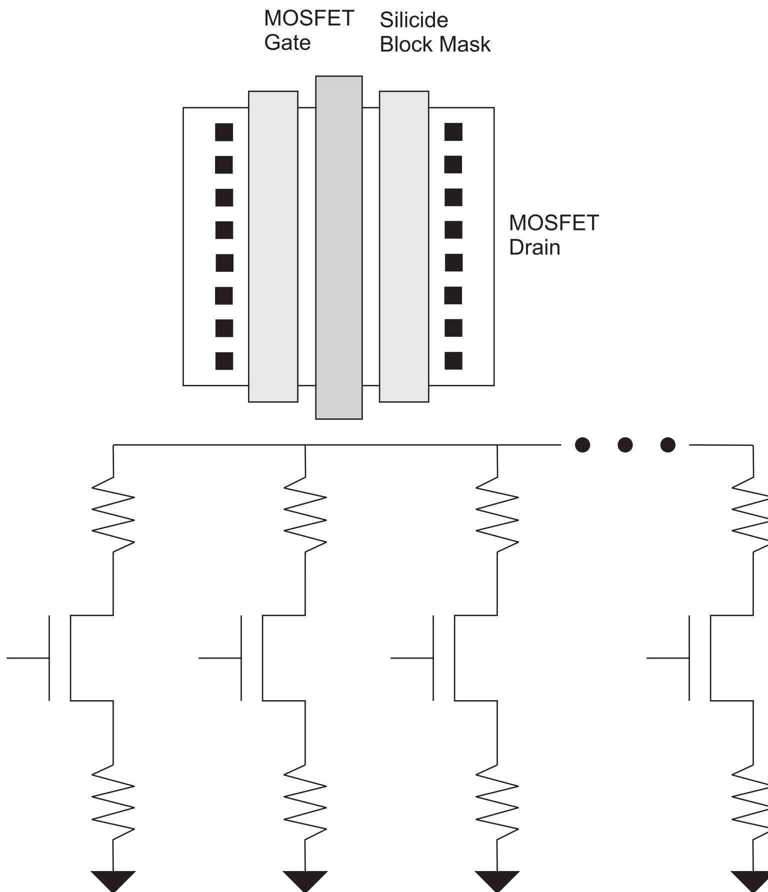

Figure 3.15 (a) Example of MOSFET ESD design using silicide block mask on MOSFET source and drain; (b) Circuit schematic of the MOSFET ESD design with MOSFET source and drain multi-finger ballasting

the gate structure. As the contact-to-gate increases, the series resistance will increase between the MOSFET structure.

Figure 3.15 (b) shows a circuit schematic of a *n*-channel MOSFET with MOSFET source and drain resistance ballasting. The introduction of the salicide block mask presents a series resistor in the MOSFET drain and the MOSFET source. In a multi-finger MOSFET structure, this introduces electrical current uniformity within the MOSFET, from MOSFET finger-to-finger. The MOSFET source resistance also introduces both electrical and thermal stability.

3.5.3 Silicide Mask Design Over Gate

In a second design practice, the MOSFET silicide block mask is extended from the MOSFET source-to-drain contacts (Figure 3.16). In CMOS technologies that do not require the MOSFET gate structure to have silicide films deposited, the silicide can be blocked. For metal gate MOSFET structures, such as MOSFETs with tungsten (W) gate films, the blocking of the silicide is possible. It is also possible to block the silicide on polysilicon MOSFET gate structures for long-channel narrow-width MOSFET structures. This method avoids the formation of the silicide in the narrow region near the MOSFET drain-to-gate overlap region, and will be less sensitive to alignment and overlay issues.

An additional ESD design practice is to eliminate the silicide along the edges of the MOSFET source and drain isolation edges [38]. This lowers the possibility of isolation-silicide-metallurgical junction triple points that lead to ESD failure. The avoidance of the self-alignment between the MOSFET isolation edges and the silicide region has the disadvantage of additional alignment issues (e.g., silicide block mask-to-isolation spacing). The advantage of this ESD design practice is the lack of sensitivity to the semiconductor drain junction and isolation design.

A fourth ESD design practice is separation of the silicide between the contacts. In the silicided contact region, the silicide between the drain contacts in the drain contact-to-contact space can be removed to introduce more lateral ballasting at the drain region. The advantage of this technique is the introduction of the ballasting in the contact region. The disadvantage of this technique is twofold. First, the model prediction of the resistance is more difficult. Second, the overlay between the contact and the silicide block masks impacts the contact-to-contact space and contact density. In one implementation, each contact had its own interconnect wire. The MOSFET OCD was connected with a set of parallel wires and parallel contacts. Where this would seem that this would provide the best

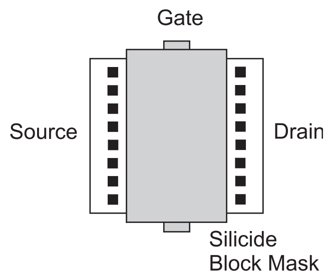

Figure 3.16 MOSFET ESD design practice with silicide blocking from MOSFET source-to-drain contacts

ESD ballasting, in actuality, the ESD failure mechanisms occurred at the contacted areas due to high current densities in some of the physical contacts.

3.5.4 Silicide and Segmentation

MOSFET resistor ballasting can also be introduced by creation of spaces in the MOSFET source and drain area laterally along a single MOSFET gate. This concept was first implemented in microprocessors in the early 1990s using *n*-well resistors and MOSFETs. Figure 3.17 shows an example of resistor ballasting within a single MOSFET finger. In this concept, the MOSFET source and drain is segmented along the MOSFET polysilicon gate finger. Using a single-finger MOSFET, the MOSFET source and drain are ‘‘cut’’ with a minimum space between the drain and source segmentations. The introduction of the segmentation prevents lateral current constriction along the length of the MOSFET structure. The advantage of this ESD design method is that only a small segment of the MOSFET channel width is sacrificed along the MOSFET length, without the need for a salicide blocking mask. The decrease in the MOSFET channel width can be recovered by lengthening of the MOSFET finger and maintaining the total MOSFET design channel width. In the early implementations of this concept, an *n*-well resistor was also integrated with each segmentation. The contacts of the MOSFET were placed at the end of the *n*-well resistor element. Each *n*-well element was integrated with the MOSFET segment along the MOSFET channel width.

In a multi-finger implementation, these segmented MOSFET fingers were then placed in parallel, forming a multi-finger MOSFET with both intra- and inter-finger resistor ballasting. In the MOSFET layout design, the resistor ballasting can be established in (a) the MOSFET drain only, (b) the MOSFET source only, and (c) the MOSFET source and drain. Additionally, in the multi-finger implementation, the MOSFET fingers can be ‘‘mirrored’’ sharing contacts at the MOSFET source or drain region. In the design, for density reasons, only MOSFET drain resistor ballasting is introduced. Additionally, for improving the MOSFET finger-to-finger snapback uniformity, local p^+ substrate contacts can be placed between each the MOSFET fingers at the MOSFET source. The options in this ESD design practice are as follows:

- Intra-finger MOSFET resistor ballasting of the MOSFET drain only.
- Intra-finger MOSFET resistor ballasting of the MOSFET drain and source.

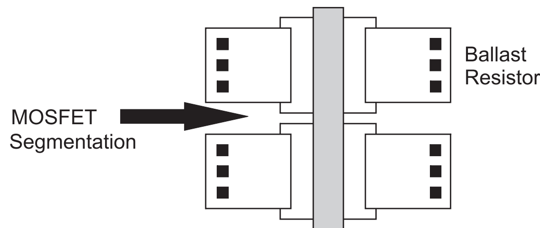

Figure 3.17 MOSFET ESD design of resistor ballasting within a single MOSFET polysilicon gate

- Multi-finger MOSFET with both intra- and inter-finger resistor ballasting.
- Introduction of local substrate contacts between the MOSFET multi-finger MOSFET.

Another ESD design methodology can establish segmentation without the utilization of the local resistor elements (first introduced by S. Voldman and D. Hui). Instead of introducing local resistor elements within the single MOSFET finger, the segmentation along a single finger can be introduced without the local resistor. The disadvantage of the local resistor elements and salicide block masks is the extra loading capacitance and area impact. Segmentation and lateral ballasting can be introduced by ‘‘cutting’’ across a full multi-finger MOSFET whose dimensions are all minimum spacing (e.g., minimum contact-to-gate, contact-to-contact, gate-to-gate, etc.). No substrate contacts are introduced between the MOSFET fingers to reduce area impacts. The ‘‘cut’’ is introduced perpendicular to the MOSFET polysilicon gate structure; this introduces a lateral MOSFET resistor ballasting. In series with the multi-finger structure is a series resistor element for each cut segmentation. This ESD design method introduces intra-finger resistor ballasting, and introduces a global single resistor with each segmentation (for all MOSFET fingers) instead of a separate series resistor for each MOSFET finger. From a MOSFET layout area, and loading capacitance issue, this ESD design method is significantly more efficient than the individual resistor for each multi-finger element. This method introduces effectively intra-finger MOSFET ballasting, and avoids the multi-finger ballasting across the MOSFET fingers. With the smaller area, the distance from the local p^+ substrate contact is comparable MOSFET finger-to-finger. The ESD design methodology is as follows:

- Design multi-finger MOSFET to minimum design rules (e.g. gate pitch, contact-to-gate, contact-to-contact)
- Place resistor element along the channel width
- Introduce source and drain ‘‘cut’’ segmentations perpendicular to the MOSFET polysilicon fingers using isolation structure with the ‘‘cut’’ width is the minimum isolation width.
- Introduce the same ‘‘cut’’ line through the resistor element, segmenting the single resistor into a multiple resistor element.

3.6 ESD MOSFET DESIGN: SERIES CASCODE CONFIGURATIONS

3.6.1 Series Cascode MOSFET

For mixed voltage interface (MVI), MOSFET devices are placed in a series cascode configuration to minimize the MOSFET drain-to-gate voltage [31,44–46]. Reduction of the MOSFET drain-to-gate voltage avoids hot electron voltage degradation, as well as reduces the MOSFET gate oxide stress. Figure 3.18 shows an electrical schematic of a multi-finger series cascode MOSFET element. The example circuit schematic shows the introduction of a MOSFET drain resistor element in series with each MOSFET finger as a ballasting element. In these implementations, the operation of the series cascode MOSFET network in ESD environments is a function of the physical layout implementation of this circuit schematic.

There are two circuit design practices for forming a series cascode MOSFET:

- Series cascode MOSFETs are spatially separated with different source and drain diffusions, and interconnected using metal levels.
- Series cascode MOSFETs are spatially integrated using a common isolation region, with the source and drain diffusions are defined by the array of MOSFET polysilicon gate structure.

In the case of the spatially separated series cascode MOSFET, the design practice is similar to a single multi-finger MOSFET. When placement of the two elements is in series, the series cascode MOSFET snapback will be the sum of the MOSFET snapback voltages. In this fashion, no current will flow through the MOSFET structures until the series cascode MOSFET snapback voltage is achieved. The advantage of this implementation (for a MOSFET OCD that requires ESD protection) is that the placement of the second MOSFET element provides more voltage margin in the network prior to current conduction. This allows the ESD current to flow through an alternate ESD current loop. The disadvantage is that more area is required for the physical contacts and wiring interconnects.

3.6.2 Integrated Cascode MOSFETs

By integration of the first- and second-series MOSFETs, the two transistors are spatially integrated into a single isolation opening. With the integrated series cascode MOSFETs, the MOSFET source of the first transistor is also the same physical diffusion as the MOSFET drain of the second transistor (see Figure 3.18). The two MOSFET gates are placed with no physical contacts between the regions; in this fashion, the first MOSFET source contacts and second MOSFET drain contacts are eliminated, as well as the associated interconnects. This design layout style provides a higher utilization of silicon area for the MOSFET network.

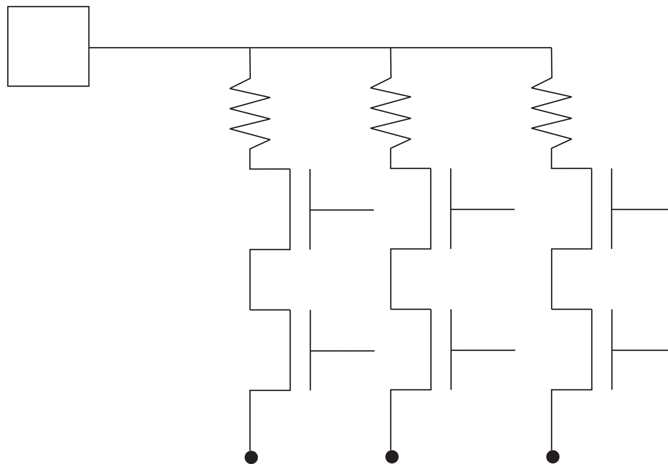

Figure 3.18 Multi-finger series cascode MOSFET structure (with drain resistor ballasting)

Without the presence of the first MOSFET source contacts and the second MOSFET drain contacts, the spacing between the first and second MOSFET gate structures can be minimum. With the integration, a new ESD MOSFET design parameter of interest is the MOSFET gate-to-gate spacing [31]. In this method of integration, the MOSFET gate-to-gate spacing can be reduced well below the MOSFET gate-to-contact spacing [31].

In the case of a multi-finger MOSFET structure, a non-uniform gate-to-gate spacing occurs if the gate-to-contact space does not match the gate-to-gate spacing [31]. From the discussion of MOSFET linewidth control, the non-uniform spacing of gate pitch can lead to nested-to-isolated linewidth offset. This can lead to MOSFET finger-to-finger channel length variations, which can lead to systematic non-uniform MOSFET second breakdown.

In the integrated series cascode MOSFET structure for MOSFET OCD networks as a MOSFET pull-down network, the MOSFET drain of the first transistor is connected to the input node and the MOSFET source of the second transistor is connected to the ground rail (e.g., V_{SS}) or chip substrate. MOSFET snapback is initiated by a high voltage being applied to the MOSFET *n*-channel drain. At the MOSFET drain-to-gate region, avalanche breakdown-generated electron–hole pairs are formed in the depletion region. As the substrate current increases, the local substrate potential decreases, leading to forward biasing of the MOSFET source of the second transistor. In this series cascode structure, since the first transistor MOSFET source is floating, it cannot sustain the MOSFET snapback current. For the series cascode MOSFET structure, the localness of the first and second transistor leads to the forward biasing of the MOSFET source of the second transistor. In parallel with the series cascode MOSFET structure, a parasitic bipolar transistor is formed between the MOSFET drain of the first transistor, the substrate, and the MOSFET source of the second transistor. This parasitic element is then a function of the spacing between the MOSFET drain of the first transistor and the MOSFET source of the second. The effective MOSFET bipolar transistor width is the sum of the first MOSFET gate length, the MOSFET gate-to-gate spacing, and the second MOSFET gate length.

The first evidence of the interaction of the two MOSFETs was evident from scanning electron microscope (SEM), transmission electron microscope (TEM), and atomic force microscope (AFM) imaging by Never and Voldman [31]. Figure 3.19 shows the AFM image of a multi-finger series cascode MOSFET structure after MOSFET second breakdown

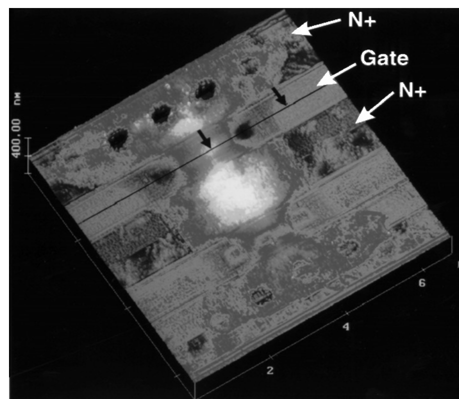

Figure 3.19 Atomic force microscope (AFM) image of the series cascode MOSFET structure

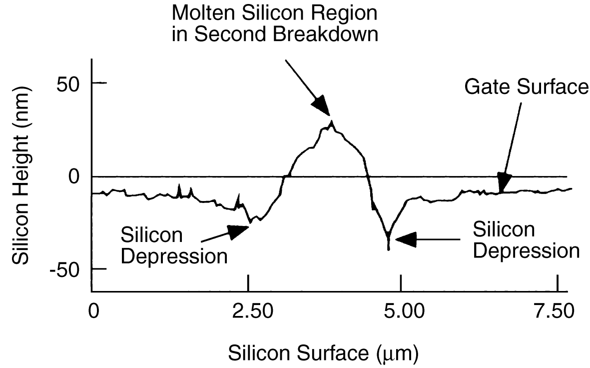

Figure 3.20 Silicon height in the series cascode MOSFET gate structure in the first MOSFET gate through the MOSFET current constriction region

occurs. The first point of interest is that the failure analysis shows that the MOSFET failure between the first and second transistor is a local phenomenon between a group of first MOSFET drain contacts and a second group of second MOSFET source contacts. MOSFET current constriction is evident in the MOSFET gate region. This is followed by a widening in the MOSFET gate-to-gate region where titanium silicide is present. The low resistance silicide region allowed for the widening of the MOSFET current constriction. As the current flow continues under the second MOSFET gate, the current constriction occurs which broadens as it extends to the second MOSFET source contacts. Figure 3.20 shows the silicon surface of the series cascode structure after MOSFET second breakdown. A cross-section was taken parallel to the current flow through the MOSFET second breakdown constriction region, under the first MOSFET gate region. In the center of the MOSFET

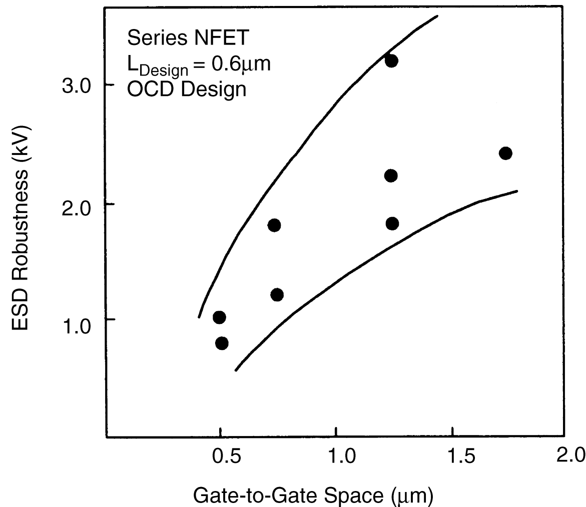

Figure 3.21 HBM ESD robustness of an application as a function of the series cascode MOSFET gate-to-gate spacing

second breakdown, molten silicon of height 20 nm is present with silicon depressions on both sides. The height of the molten silicon is above the MOSFET gate surface.

The first ESD measurements on the series cascoded MOSFET structure were demonstrated in a STI-defined 0.25-μm channel length technology by Voldman [31]. Figure 3.21 shows that the HBM ESD robustness of a series cascode MOSFET multi-finger structure increases with increased MOSFET gate-to-gate spacings. MOSFET device ESD HBM robustness increased from to 2.5 kV as the MOSFET gate-to-gate space increased from 0.5 to 1.5 μm.

As an example implementation, the MOSFET gate-to-gate spacing was varied in a design with a fixed-size ESD network, and fixed OCD pull-up design. In the series-cascode design, the series cascode MOSFET structure in a design implementation, the ESD design remained fixed, but the gate-to-gate spacing was increased from 0.5 to 1.5 μm. Experimental results showed increasing HBM ESD robustness from 4 to 6 kV with the increased spacing.

3.7 ESD MOSFET DESIGN: MULTI-FINGER DESIGN INTEGRATION OF COUPLING AND BALLASTING TECHNIQUES

A fundamental ESD concept is that to provide good current uniformity in a multi-finger MOSFET structure, it is understood that given the MOSFET second breakdown voltage, V_{t_2}, exceeds the MOSFET first breakdown voltage, V_{t_1} [47]. In a standard semiconductor process, the typical condition is the opposite, which leads to a non-uniformity of current distribution in a multi-finger MOSFET. But, using ballasting, coupling, and biasing techniques, the MOSFET second breakdown voltage, V_{t_2}, can exceed the MOSFET first breakdown voltage, V_{t_1}, leading to MOSFET current uniformity in a multi-finger MOSFET structure. Multi-finger MOSFET ESD design utilizes both coupling, and ballasting concepts to improve the current uniformity during high-current events [48]. Coupling and ballasting techniques can be integrated together to provide improved ESD robustness. The following implementations utilize both gate coupling and resistor ballasting:

- Substrate grounded-gate (with gate resistor) resistor-ballasted multi-finger MOSFET.
- Substrate grounded-gate (with gate resistor and capacitor element) resistor-ballasted multi-finger MOSFET.
- Soft substrate grounded-gate resistor-ballasted multi-finger MOSFET.
- Domino source-to-gate coupled resistor-ballasted multi-finger MOSFET.
- MOSFET source-initiated gate-bootstrapped resistor-ballasted multi-finger MOSFET with MOSFET.
- MOSFET source-initiated gate-bootstrapped resistor-ballasted multi-finger MOSFET with diode.

3.7.1 Grounded-Gate Resistor-Ballasted MOSFET

Figure 3.22 shows a substrate grounded-gate resistor-ballasted multi-finger with a resistor between the MOSFET gate and the substrate ground. In this configuration, the gate structure

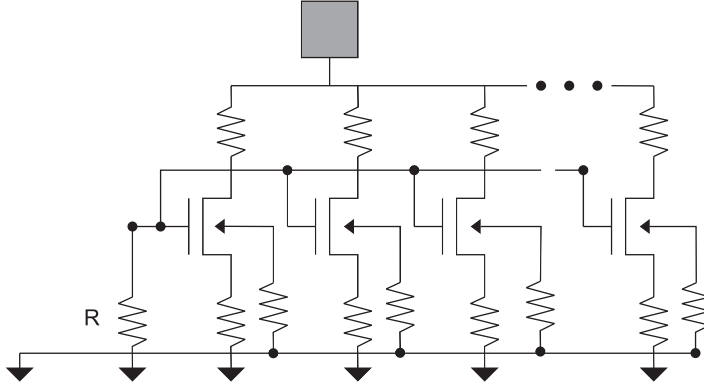

Figure 3.22 Grounded-gate resistor-ballasted MOSFET with gate resistor element

is connected to the ground potential through a resistor element [48]. The resistor element introduces a ''soft-ground'' and allows for RC-coupling of the physical element associated with the resistor, the MOSFET drain-to-gate capacitance (e.g., overlap capacitance). In this implementation, as the potential on the signal pad increases, the MOSFET gate is coupled, leading to a rise in the MOSFET gate potential. The MOSFET gate resistor allows for the MOSFET gate voltage to couple with the input node signal. As the MOSFET gate rises to the MOSFET threshold voltage, MOSFET current conduction is initiated. As the current flows into a given MOSFET finger, the voltage across the drain resistor element leads to a de-biasing effect. This limits the voltage drop across the given element, allowing for the current to distribute to adjacent MOSFET fingers.

In a small modification of the substrate grounded-gate (with gate resistor) resistor-ballasted multi-finger MOSFET, a capacitor element can be placed externally in parallel with the MOSFET gate-to-drain capacitance (Figure 3.23). Maloney highlighted that an additional capacitor element can be placed in a parallel fashion between the MOSFET drain and the MOSFET gate electrode [48]. As the capacitor size increases, the MOSFET gate capacitive couples to the MOSFET drain during a positive ESD event on a pad. As the

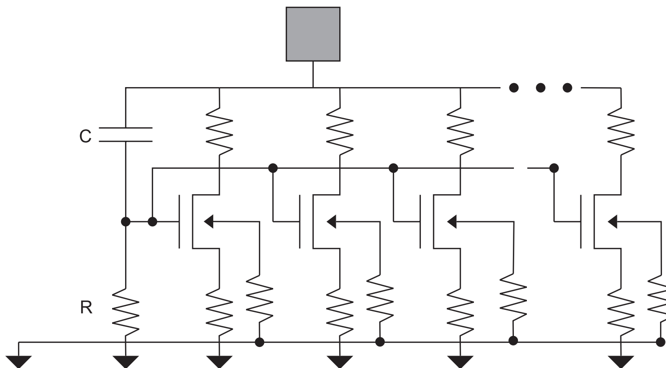

Figure 3.23 Grounded-gate resistor-ballasted MOSFET with gate resistor element and external capacitor element

MOSFET gate voltage increases, MOSFET conduction is initiated, leading to improved current uniformity.

3.7.2 Soft Substrate Grounded-Gate Resistor-Ballasted MOSFET

''Soft'' substrate grounded-gate resistor-ballasted multi-finger MOSFET (e.g., s-ggNMOS) allows the electrical connection of the MOSFET gate structure to increase in potential relative to the semiconductor chip substrate. As in the prior developments, the MOSFET gate potential is allowed to increase. As the MOSFET gate increases to the MOSFET threshold voltage, the MOSFET will conduct current from the MOSFET drain to the MOSFET source, allowing current to flow from the signal pad to the semiconductor chip substrate.

Figure 3.24 is a representation of a ''soft'' grounded-gate resistor-ballasted multi-finger MOSFET (ss-ggNMOS) as represented by Mergens *et al.* [48]. A resistor element is placed in series with the MOSFET drain and the source element for each individual MOSFET finger to introduce MOSFET source and drain resistor ballasting. The MOSFET gate structures are electrically connected across all the MOSFET fingers to allow the MOSFET gate potential coupling between the fingers. In this gate-biasing technique, a local substrate contact is placed near the MOSFET source and drain, but electrically decoupled from the metal V_{SS} power bus. Two key points in this implementation are that the MOSFET drain and source are electrically coupled to the signal pad and the V_{SS} power rail, and the MOSFET gate electrode is resistively decoupled from the V_{SS} power rail, and responds to local substrate perturbations from injection phenomenon in the region of the MOSFET source and drain. As the MOSFET drain potential increases, electrons are attracted to the MOSFET drain region in the metallurgical junction. As the potential increases, electron–hole avalanche occurs. The hole generation flows in the metallurgical junction to the substrate region. The hole injection local to the MOSFET drain increases the local potential, leading to MOSFET snapback of the first MOSFET finger; this is followed by other MOSFET fingers undergoing MOSFET

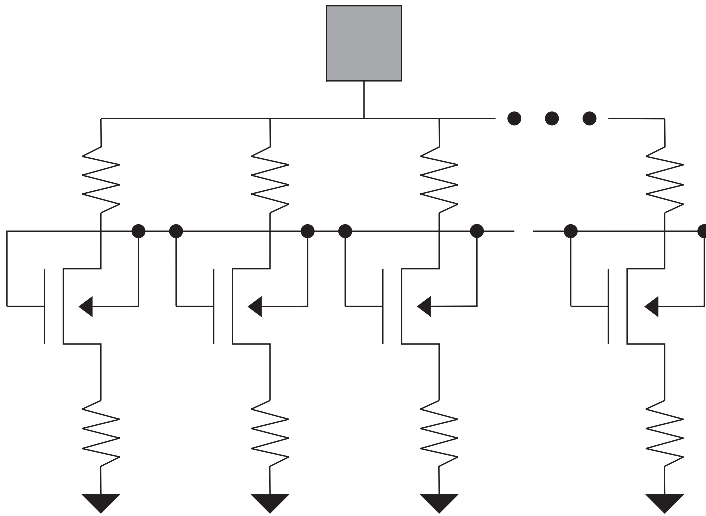

Figure 3.24 Soft grounded-gate resistor-ballasted multi-finger MOSFET

snapback. As the local potential increases, the MOSFET local substrate contact increases, leading to the MOSFET gate to increase in potential. Additionally, as the MOSFET local potential rises, the potential in the MOSFET channel region rises. From the MOSFET reverse body effect, the MOFET threshold voltage decreases as the MOSFET channel potential increases. When the MOSFET gate electrode increases to the MOSFET threshold voltage, the MOSFET source-to-drain conduction occurs. Note that in this implementation, any of the substrate contacts local to any of the MOSFET fingers introduces a MOSFET finger-to-finger coupling through the MOSFET gate structure. Also note that the MOSFET resistor ballasting acts as a "current limit" through any one finger between the separate MOSFET source and drain fingers. In this way, the current redistributes through the MOSFET drain structures. Additionally, the MOSFET source resistances serve to increase the electrical and thermal stability of the network.

MOSFET gate-coupling can be introduced from the MOSFET drain through overlap capacitance, additional capacitors, or through the input signal pads. MOSFET gate-coupling can also be introduced through the MOSFET source region. To initiate MOSFET source-coupling, the MOSFET source potential must be allowed to increase in electric potential. A method to enable the MOSFET source potential to increase relative to the substrate potential is by resistive decoupling. This is achieved by placement of a resistor element between the MOSFET source and the V_{SS} power rail. Introduction of a ballast resistor between the MOSFET source and the V_{SS} power rail allows for the MOSFET source potential to increase.

3.7.3 Gate-Coupled Domino Resistor-Ballasted MOSFET

Mergens *et al*. [48] introduced a "domino" method in a multi-finger MOSFET structure by electrically connecting the MOSFET gate of a second MOSFET finger to the MOSFET source of a first MOSFET finger (Figure 3.25). In this domino source-to-gate coupled resistor-ballasted multi-finger MOSFET, the MOSFET source ballast resistor is split into a first and second resistor element. An electrical connection is established between the two resistor elements and electrically connected to the MOSFET gate of a second finger. This is initiated *adinfinitum* to all the finger elements. The "*n*th finger" MOSFET source connection is electrically connected to the MOSFET gate of the first MOSFET finger. In this fashion, the domino triggering initiation can occur in any MOSFET finger in the structure. As the signal pad increases, the electrical potential of all the MOSFET drain structure increases. As the MOSFET drain potential increases, avalanche multiplication occurs. Eventually, one of the MOSFET fingers undergoes MOSFET snapback. As the electrical conduction occurs in the MOSFET finger, the current flows through the MOSFET source resistor elements. The two resistor elements form a voltage resistor divider. As the voltage increases, the MOSFET gate structure potential increases. As the MOSFET gate potential increases, adjacent MOSFET finger begins to conduct MOSFET source-to-drain current through the MOSFET channel region. As the second MOSFET finger conducts current through its own source, the electrical potential of the MOSFET gate of the third MOSFET finger increases. This continues in this fashion, until the "*n*th" MOSFET finger. As the "*n*th" MOSFET finger undergoes MOSFET conduction, the MOSFET gate of the first MOSFET finger that underwent MOSFET snapback, will have its MOSFET gate potential increase, leading to MOSFET channel conduction instead of a MOSFET snapback state.

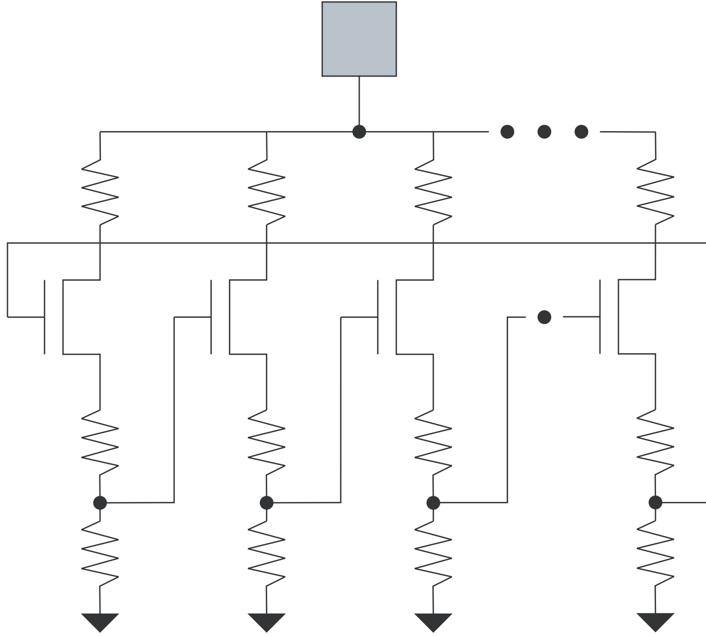

Figure 3.25 Domino source-to-gate coupled resistor-ballasted multi-finger MOSFET

In this implementation, it was pointed out that the nature of the conduction and response in the "Domino" multi-finger MOSFET is different from other multi-finger MOSFETs, in the following ways:

- The response of the network is current-driven (as opposed to frequency-driven).
- The response is a "static" phenomenon not "dynamic."
- The time response of the network is associated with the MOSFET gate delay time and the number of MOSFET finger stages.
- The operation time is "auto-timed" and acts only during a fixed time interval associated with the RC response of the successive stages, the MOSFET gate delay, and the number of successive stages.

These distinctions lead to many advantages over other implementations. For example, the frequency-driven MOSFET networks are a strong function of the MOSFET overlap capacitance of the MOSFET technology, making the ESD operation a strong function of the process technology. Additionally, soft grounded-gate NMOS networks are very dependent on the substrate and *p*-well doping concentration as well as the design layout of the substrate contact structure and the modeling/prediction of the substrate resistance. In this implementation, the MOSFET current and the models are predictive models, as well as the circuit response.

Additional advantage of this implementation is that the turn-on of the individual stages does not require the charging of the entire MOSFET gate structure for all MOSFET fingers.

In the case where all MOSFET fingers are electrically connected together, the circuit response time will be a function of the total gate electrode capacitance (i.e., number of fingers). In this case, the MOSFET finger-to-finger time response will be significantly faster due to the smaller capacitance load of the individual MOSFET finger.

3.7.4 MOSFET Source-inItiated Gate-Bootstrapped Resistor-Ballasted Multi-Finger MOSFET With MOSFET

MOSFET source-initiated gate coupling can be initiated to individual MOSFET fingers sequentially or all MOSFET fingers simultaneously. In an domino-style implementation, the MOSFET fingers are gate-coupled in a sequential manner (Figure 3.26). In the soft grounded-gate MOSFET, all fingers are initiated simultaneously. In the case of the individual sequential coupling technique, the response of the individual gate structures will have a faster RC-time response for each individual fingers. But the disadvantage is the electrical disconnection of the MOSFET gate structure for utilization as a MOSFET off-chip pull-down.

MOSFET source-initiated gate coupling can be implemented in a fashion, where one MOSFET source initiates a common MOSFET gate electrode. As in the domino-style implementation, a MOSFET source is electrically connected to two series resistor elements. The center node of the two resistor elements is electrically connected to initiate MOSFET gate-coupling. With a common gate electrode, the MOSFET source connection cannot be electrically connected to the MOSFET gate. Hence, an additional bootstrap MOSFET is placed between the signal pad and the MOSFET gate electrode. The bootstrap MOSFET drain is connected to the signal pad, its source connected to the primary MOSFET gate electrode. The MOSFET source resistor center-tap is electrically connected to the gate of the bootstrap MOSFET.

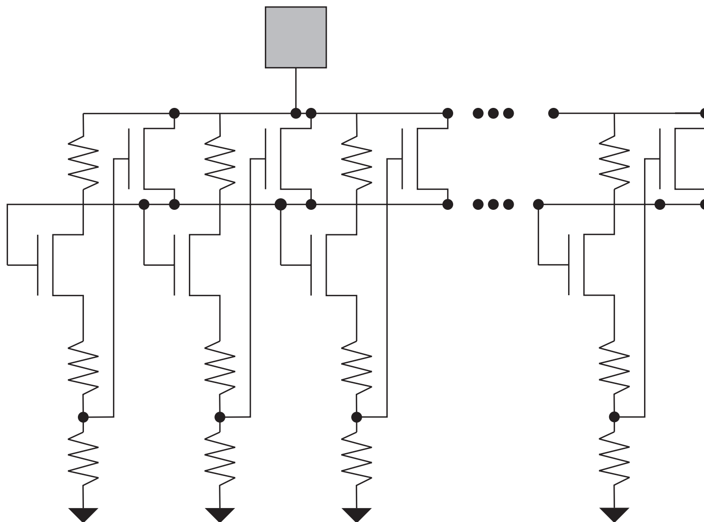

Figure 3.26 MOSFET source-initiated gate-bootstrapped resistor-ballasted multi-finger MOSFET with MOSFET

In this network, the first conducting MOSFET finger source senses the ESD event, leading to a rise in the MOSFET source potential. This first MOSFET finger source rises. The electrical potential of the MOSFET source resistor divider leads to an increase in the gate of the corresponding bootstrap MOSFET element. The bootstrap MOSFET undergoes MOSFET conduction when the MOSFET threshold voltage is exceeded. The bootstrap MOSFET element charges up the MOSFET gate electrode, leading to MOSFET conduction in the other adjacent MOSFET fingers, which were not undergoing MOSFET snapback. The advantage of this method allows for electrical connection of the primary MOSFET gate to a pre-driver network for utilization in OCD networks or other circuits. The disadvantage of this structure is the need for an additional resistor and MOSFET for every segmentation of finger elements. This adds extra capacitance loading and space impact.

3.7.5 MOSFET Source-Initiated Gate-Bootstrapped Resistor-Ballasted Multi-Finger MOSFET With Diode

MOSFET source-initiated gate coupling can be implemented in a fashion, where one MOSFET source initiates a common MOSFET gate electrode. Utilizing a MOSFET source with two series resistor ballast elements and a center tap, MOSFET gate coupling can be initiated through a diode element. In the case that a MOSFET bootstrap element is used, this bootstrap element requires additional space as well as impacting capacitance loading on the signal pad (Figure 3.27). With the utilization of a diode element between the MOSFET source and the MOSFET gate electrode, no additional loading capacitance occurs on the

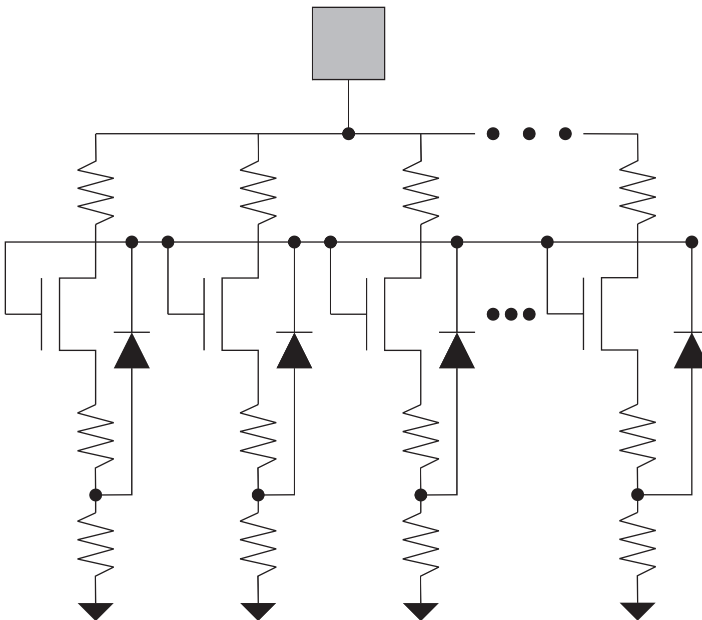

Figure 3.27 MOSFET source-initiated gate-bootstrapped resistor-ballasted multi-finger MOSFET with diode bootstrap element

signal pad, and less area can be utilized. In this network, the first conducting MOSFET finger source senses the ESD event, leading to a rise in the MOSFET source potential. This first MOSFET finger source rises. The electrical potential of the MOSFET source resistor divider leads to an increase in the anode of the bootstrap *p–n* diode element. The bootstrap *p–n* diode element charges the MOSFET gate electrode when the *p–n* diode element becomes forward active. When the MOSFET gate electrode rises, MOSFET channel conduction occurs in all MOSFET finger elements providing uniform current flow. The advantage of this method allows for electrical connection of the MOSFET gate to a pre-driver network for utilization in OCD networks or other circuits. This method also prevents the additional loading on the signal node compared to other bootstrap methods. A disadvantage of this method is that the diode elements must charge the complete MOSFET gate electrode. As a result, this method may be limited by the diode current drive and the number of MOSFET fingers that can be driven by the bootstrap element.

3.8 ESD MOSFET DESIGN: ENCLOSED DRAIN DESIGN PRACTICE

Alternate ESD design practices exist that attempt to avoid metal bus distribution effects and isolation technology issues. One design practice is to create an "enclosed" MOSFET drain.

Figure 3.28 is an example of the enclosed drain MOSFET design style. The MOSFET source encloses the area of the MOSFET structure, with a substrate contact outside of the MOSFET source. The MOSFET polysilicon gate structure is formed in a ring-like structure around the MOSFET drain; the MOSFET drain is contained within the MOSFET polysilicon gate region. In this design style, since a metal contact cannot be placed on the MOSFET polysilicon gate structure dielectric, a small isolation region is formed to "break" the MOSFET dielectric area. A small rectangle is formed where the polysilicon film extends over the isolation structure. At this location, a metal contact can be placed to electrically connect the MOSFET polysilicon gate structure. The metal design pattern will allow a "broad-side" metal connection along the full width of the MOSFET drain without metal distribution and resistance issues. For a multi-finger implementation, the design is "mirrored" around the MOSFET source, and multiple polysilicon rings are formed. In this implementations, there are many potential advantages. First, as discussed, the voltage distribution are minimized because of the "broadside wiring" that allows for no lateral distribution issue. Second, there is no isolation-dependent leakage mechanisms, junction/salicide edge, junction/isolation edge, and triple-point junction/salicide/isolation edge issues (except at the small isolation island area for MOSFET gate connection). This design style effectively contains a polysilicon-bound MOSFET drain region, minimizing LOCOS bird's beak issues and STI pull-down [30]. Additionally, the substrate contact is effectively equal distance from the source and drain on all sides.

In summary, the MOSFET "enclosed drain" ESD design practice avoids the following MOSFET issues:

- MOSFET voltage distribution drops in metal design.
- Technology-dependent LOCOS or STI issues.

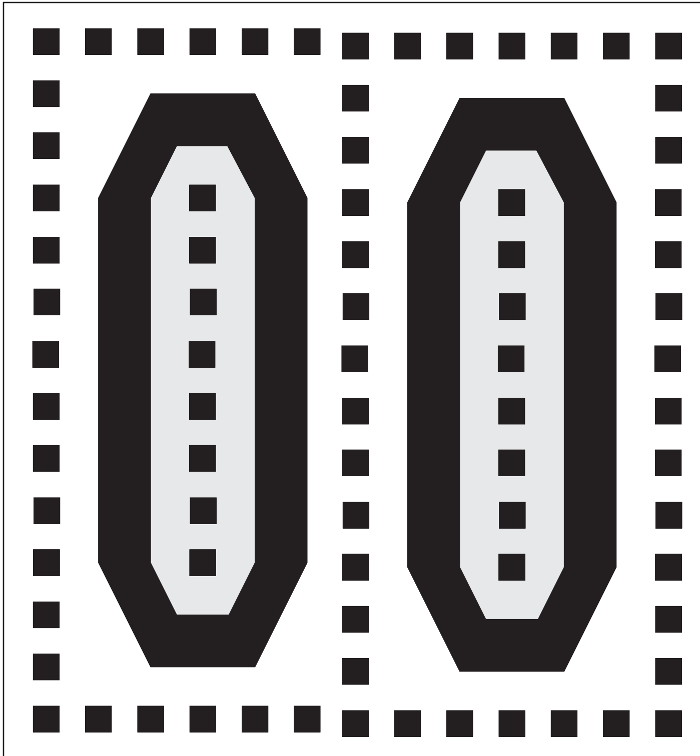

Figure 3.28 Enclosed drain MOSFET ESD design

- Technology-dependent silicide distribution issues.
- Equal source-to-substrate contact spacing.

3.9 ESD MOSFET INTERCONNECT BALLASTING DESIGN

In MOSFET ESD design, resistor ballasting can be introduced using interconnect structures. In the ESD design practice, resistor ballasting is introduced into MOSFET structures to prevent MOSFET second breakdown [48–52]. The MOSFET series resistance serves a first purpose of limiting the current in a MOSFET during ESD events. The role of the series resistance establishes a current limit through the MOSFET structure. In the case that the MOSFET has an ESD element in a parallel ESD current loop, the voltage drop incurred by the series resistance allows the current to flow through the ESD current loop, buffering the MOSFET network, as well as establishing an increase in the voltage margin of ESD network operation prior to MOSFET failure.

MOSFET interconnect resistor ballasting provides series resistance ballasting when connected at the MOSFET drain, and can introduce lateral ballasting by connecting to individual drain contacts. Refractory metals also exist as liner material aluminum and copper interconnect systems. Hence, resistors formed from titanium and tantulum films can serve as

good ballasting elements [49]. Refractory metal resistor films have many advantages for resistor ballasting. Using the liner materials, resistor elements have low capacitance, low skin effect, high linearity, a high melting temperature, high critical current to failure, and do not require space on the silicon surface. The resistor structure can be formed on the walls of a dielectric trough. The structure can be applied to circuit applications such as an ESD network, an RC-coupled MOSFET, a resistor-ballasted MOSFET, and others. The resistors can be in series with the MOSFET or other structures [49]. These structures are also compatible with fuse elements.

In some technologies, there exist refractory metal "local interconnects." Refractory metal layers, such as "M0" tungsten, can serve as resistor ballasting layers and resistor structures for ESD protection [50]. Refractory metals have the advantage of high melting temperatures. For example, tungsten metallurgy used in "local interconnects" has a 3400 °C melting temperature, which is significantly above silicon and dielectric melting temperatures. One advantage of the refractory metal local interconnect is that the film thickness allows to carry significant current. Utilization of a refractory metal resistor as a resistor buffering element was demonstrated by K. Duncan in a DRAM application (Figure 3.29). K. Duncan and C. Brennan noted the resistance response at temperature, $R(T)$, due to self-heating of tungsten interconnects, also provides ESD advantage.

But, it is a disadvantage of using aluminum and copper interconnects as MOSFET ballasting elements because of the low melting temperature, and low interconnect resistances of aluminum and copper. Another disadvantage is that the nature of the films change material state and crystalline structure when undergoing self-heating. A fourth disadvantage is to provide adequate resistance; the interconnect will introduce space and inductance concerns. Removal of copper materials will allow utilization of the refractory liner for resistor-ballasting elements for ESD applications [49].

A design practice advantage of using interconnect ballasting over MOSFET source and drain salicide block masks is the capacitance loading and area reduction of the MOSFET structure [51]. Prior to the ESD design practice of silicide blocking, many technologies constructed ESD designs with silicide. Silicide block masks added additional costs and space. A second advantage is the lack of parasitic mechanisms and lack of interaction with

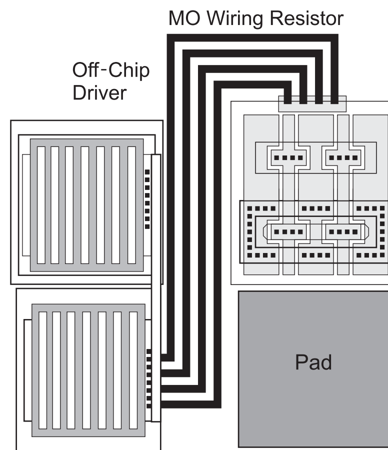

Figure 3.29 M0 local interconnect in ESD MOSFET design

the substrate region. During CDM testing, silicon resistors are interactive and play a role in the CDM response. Hence, using interconnect ballasting elements, utilizing refractory metal resistors instead of silicon-based resistors, can have advantages as long as low-temperature materials, such as aluminum and copper, are avoided.

3.10 ESD MOSFET DESIGN: SOURCE AND DRAIN SEGMENTATION

Source and drain segmentation has been introduced in the early 1990s in microprocessor designs and ASIC implementation with the introduction of resistor ballasting. This was typically achieved by introducing cuts through the single- or multi-finger MOSFET structure. In this process, the MOSFET drain regions maintained a rectangular shape in the segmentation. In new concepts proposed by E. Worley, non-rectangular shapes of the MOSFET source and drain region are introduced to provide local resistance increases. For MOSFETs, E. Worley demonstrated a method of segmentation of the MOSFET source and drain region to introduce resistor ballasting and avoid area loss [52]. The objectives of the MOSFET resistor ballasting include the following:

- Low global parasitic series resistance relative to the MOSFET channel resistance.
- High series resistance in series with a localized hot spot.
- Low drain capacitance.

Worley points out that an additional ballasting objective is associated with the substrate resistance. The key factors that initiate MOSFET snapback spatial dependence are the following:

- Proximity of substrate contact to MOSFET fingers.
- MOSFET channel-to-substrate contact resistance.

Using a first layout scheme, Worley introduced a ‘‘staggered’’ ballasting implementation (Figure 3.30) [52,53]. Using a second new layout scheme, known as the Staggered Segmented diffusion layout, the MOSFET source and drain layout is segmented into

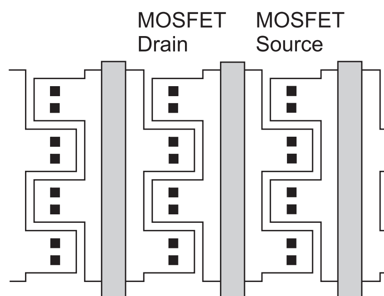

Figure 3.30 Staggered ballasted MOSFET design

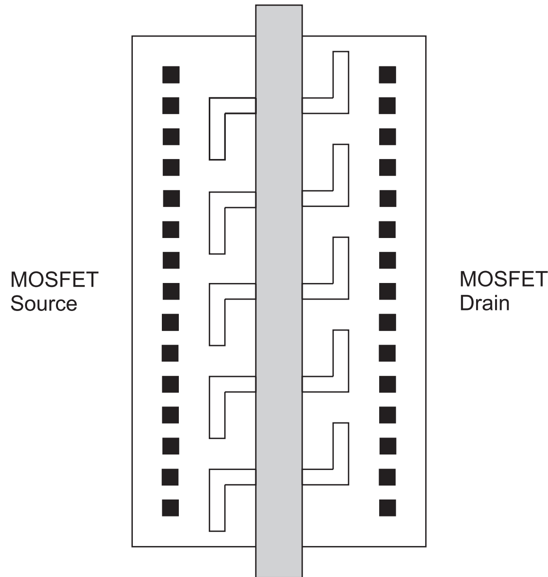

Figure 3.31 Staggered segmented ballasted MOSFET design

sections by extending the MOSFET source and drain to individual contacts between the multi-finger gate regions; this solution introduces local resistors associated with each contact. At the same time, the area on the edges is eliminated lowering the total MOSFET source/drain capacitance. Worley integrated this concept with a second layout, which allows for the local resistor and segmentation of the MOSFET along the length of the MOSFET polysilicon finger. The ''breaking'' of the MOSFET source drain at the edge of the MOSFET, as discussed in prior sections, introduces segmentation of the MOSFET along a given MOSFET finger; this can be integrated with the concept of Worley to provide another means of providing resistor ballasting (Figures 3.31). A new feature is the path at which the current must flow in order to reach the MOSFET channel region, allowing for resistor structures in parallel to the MOSFET gate width, followed by a transition perpendicular to the MOSFET channel gate width.

3.11 SUMMARY AND CLOSING COMMENTS

In this chapter, ESD design practices and analysis are highlighted using the MOSFET as the vehicle for discussion. The ESD design practices discuss all aspects of the layout and design from the physical dimensions, the placement of the contacts, the orientation of the wiring, the placement of silicide, and isolation issues, as well as the single-versus multi-finger structure. The chapter uses the solution of the cylinder and plane surface for evaluation of the microscopic heating between the contact and gate edge. The chapter draws the connection of the local contact-to-gate analysis and the ladder network models of DeChairo and Krieger. In the analysis both contain resistance ratios that can be utilized as ESD design metrics. The chapter then discusses the series-cascode analysis of N. Dickson, G. Gerosa, S. Voldman, and

J. Never. To close the chapter, we provide some of the examples, discussed by M. Mergens, that highlight multi-finger interactions, ballasting, and gate-coupling concepts.

In Chapter 4, the design and layout of ESD diode elements are discussed. Chapter 4 will discuss the ESD issues with diode elements from the wells to the interconnect layout. The chapter will discuss single diode elements as well as series diodes (e.g., also referred to as diode-string diode designs) in single-, dual-, and triple-well technologies.

PROBLEMS

3.1. From the analysis of the electric field and current from a contact of radius, R, shows that the denominator can be put in the form of an inverse hyperbolic cosine (e.g., $\cosh^{-1}(x)$) form. What is the characteristic ratio of the solution? Show an equivalency to the logarithm expression.

3.2. Derive the equation for the locus of points that form equi-energy surfaces in the two-dimensional plane. Solve the fourth order quartic equation.

3.3. Derive the current density at the MOSFET gate (e.g., $x = 0$) case for a single contact. Derive the lateral current density.

3.4. Assuming that the temperature field from a single contact is proportional to the square root of the product of the current density and electric field. Derive the temperature field.

3.5. Assume the heat fluence is equal to minus the derivative of temperature, solve for the heat flux laterally along the MOSFET device from the single contact. Derive the heat flux in the x- and y-dimension.

3.6. Solve the current density for a set of N contacts, which are spaced at a center-to-center spacing of value b, assuming superposition of the N contacts. Solve for the peak current density.

3.7. Given N contacts, and allowing for superposition of the current equation, what spacing b achieves the most uniform current density at the MOSFET gate (e.g., $x = 0$ plane)?

3.8. Show the relationship between the solution of spreading resistance from a single contact in the electrical field solution. Derive the spreading resistance from the contact of radius R to the MOSFET gate (e.g., $x = 0$ plane). Relate this to a resistive ladder network.

3.9. Given the DeChairo ladder network model, derive the maximum voltage and current differential between the first finger and the Nth finger.

3.10. Given the Duvvury ladder network model of broad-side connection of a multi-finger MOSFET structure on the drain, a finger resistance R_F, and a source finger-to-finger bus resistance of R_s, assume that the end resistances are double the center resistance since the last fingers are not folded (e.g., one-sided). Given N drain fingers, solve the relationship resistance matrix as a N-2 region, with two different end resistances R_E. What is the recursive relationship at the ends? Derive the resistance matrix and current in each current loop in the ladder network.

3.11. Given the anti-parallel current flow in a single-finger MOSFET, using the Krieger model, what is the voltage drop between the two ends of the MOSFET finger (e.g., along the upper wire)?

3.12. Given the parallel current flow in a single-finger MOSFET, using the Krieger model, what is the maximum voltage drop along the MOSFET finger (e.g., along the upper wire)?

3.13. Assume that ESD failure does not occur as the voltage is raised into MOSFET second breakdown, V_{t_2}. Derive a relationship for the parallel and anti-parallel cases of the percentage of the wire width that is above V_{t_2} as a function of current source magnitude.

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4 Electrostatic Discharge (ESD) Design: Diode Design

Diodes are the basic building blocks of ESD design. Diodes are used for ESD input node devices [1–15], mixed-voltage interface input environments [16–22], ESD rail-to-rail devices [23,24], and ESD power clamps [25–28]. Diodes and gated-diodes serve as good ESD protection elements in many technologies: CMOS [1–26], radio frequency (RF) CMOS [12,13,15], BiCMOS silicon germanium [29–32], and silicon-on-insulator (SOI) [33–38]. The key to good ESD design of diode structures is establishment of good current uniformity, establish internal ballasting, and avoidance of defect mechanisms that reduce the ESD effectiveness. Quantification of these design aspects can be achieved experimentally by the ESD results, simulation, or failure analysis. In this chapter, we will discuss the design features of ESD diode structures for ESD networks.

4.1 ESD DIODE DESIGN: ESD BASIC

4.1.1 Basic ESD Design Concepts

In ESD design of diode structures, there are some underlying fundamental concepts that one can adhere to in order to have effective ESD results. Diode ESD design have the following design objectives:

- Provide a solution that establishes a low-voltage trigger element, which can discharge a high current.
- Provide spatially uniform current density within the diode structure.
- Avoid localized Joule heating.
- Avoid electrical connections that exceed the breakdown voltage of the dielectric films.
- Operate the device under the diode breakdown voltage.
- Improve thermal stability of the diode structure.

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The ability to provide a low-voltage trigger element can be achieved by the following means:

- Use diode elements in the forward bias mode of operation to achieve low turn-on voltage.
- Minimize the diode series resistance.
- Minimize the number of diode elements in series.
- Maximize the number of parallel diode elements.

High current can be achieved in diode ESD structures by the following means:

- Low-resistance interconnects, via and contact structure and design.
- Minimize the space between the anode and cathode regions.
- Minimize the spacing between anode and cathode physical contacts.
- Maximize the number of anode and cathode contacts that exist at minimum spacing.
- Maximize the anode perimeter-to-area ratio.
- Low-resistance salicide films on anode and cathode.
- Heavily doped anode and cathode regions.

Spatial uniformity is achieved in the diode ESD structure by the following means:

- Provide design spatial and electrical symmetry in the metal and contact design.
- Ballasting perpendicular to the direction of the diode current flow.

Avoidance of localized heating in the diode structure can be achieved by the following means:

- Provide design symmetry in the metal and contact design.
- Introduce ballasting perpendicular to the diode current flow. (e.g., lateral ballasting) via design or semiconductor process.
- Utilize vertical structures to avoid localized heating near the isolation surface.
- Increase doping concentrations to increase the intrinsic temperature (T_i) and reduce the Joule heating of the diode regions.

Avoidance of failure of the diode structure in gated-diode structures due to dielectric breakdown can be achieved by the following means:

- Avoid diode gate-to-power rail direct connections.
- Avoid diode gate-to-pad direct connections.

Avoidance of diode thermal second breakdown and increase in thermal stability can be achieved by the following means:

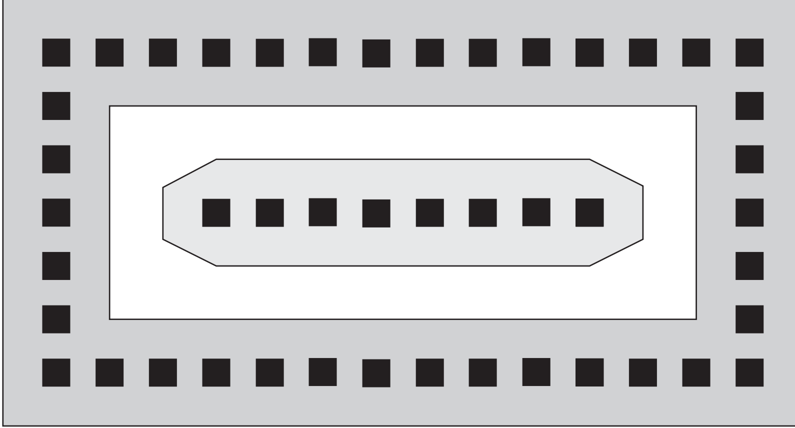

Figure 4.1 Physical layout design of a STI-defined diode structure

- Increase doping concentration of anode and cathode to increase the intrinsic temperature.
- Reduce the IR voltage drop in the diode structure.
- Minimize the Joule heating in the diode structure.
- Avoid avalanche multiplication and electrical diode junction breakdown voltage.

4.1.2 ESD Diode Design: ESD Diode Operation

In the design of ESD diodes, the operation in high-level injection is key to its operation. Figure 4.1 shows an example of the physical layout of a shallow trench isolation (SIT) diode structure. In this figure p^+ anode has chamfered corners, and is surrounded by STI structure.

The diode current equation in high-level injection can be expressed as [1,38]

$$I = I_\mathrm{s} \frac{\left(\mathrm{e}^{V_j/kT-1}\right)\left(1 + \eta\, \mathrm{e}^{q(V_j-\phi_i)/kT}\right)}{1 - \mathrm{e}^{2q\left(V_j-\phi_i\right)/kT}}$$

where

$$I_\mathrm{s} = qA\left\{\frac{D_p}{L_p} p_{n0} + \frac{D_n}{L_n} n_{p0}\right\}$$

and for a p^+/n diode is

$$\eta = \frac{N_\mathrm{a}}{N_\mathrm{d}}$$

and for a n^+/p diode

$$\eta = \frac{N_\mathrm{d}}{N_\mathrm{a}}$$

This expression reduces to the ideal diode case when the excess minority-carrier injection is small compared to the doping concentrations.

Diode resistance is critical in the understanding of the operation of a diode element during electrostatic discharge events [1–6,11–13,17–22,30]. In a p^+/n-well diode structure, the anode resistance is a function of the contacts resistance, silicide film, and the p^+ diode implant resistance. The design of the contacts and the silicide film play a key role in the forward-bias operation and the current density distribution of the diode structure. The cathode resistance (e.g., the n-well region) is a function of the implant profile, the dose, and width of the physical well structure.

On the anode, the resistance can be expressed as

$$R_{\text{anode}} = R_{\text{M}} + R_{\text{C}} + (R_{\text{Sal}})_{\text{eff}} + (R_{\text{d}})_{\text{eff}}$$

where the anode resistance is the resistance of the interconnect, the contact, the salicide film, and the anode implant. For the silicide film, the material, area coverage, and design of the silicide formed on the junction can alter the effectiveness of the silicide as well as the diffusion area on the ESD protection.

$$R_{\text{cathode}} = R_{\text{M}} + R_{\text{C}} + (R_{\text{Sal}})_{\text{eff}} + (R_{\text{d}})_{\text{eff}} + R_{\text{well}}$$

Equivalently, for the cathode, the cathode resistance is the sum of the resistances in series as well as the well resistance. For the cathode, typically the well resistance is the largest component of resistance which influences the ESD results.

From the diode equation, we can express the voltage across the diode as the sum of the voltage drops across the series resistance and the voltage drop across the metallurgical junction

$$I_{\text{D}} = I_{\text{s}}\left\{\exp\left(\frac{qV_{\text{D}} - \sum I_{\text{D}}R_i}{kT}\right) - 1\right\}$$

where summation is over the voltage drops across the series resistances. The resistance can also be obtained from the derivative of the voltage with respect to current [38].

$$\frac{\mathrm{d}V_{\text{D}}}{\mathrm{d}I_{\text{D}}} = \frac{\mathrm{d}(V_{\text{J}} + V_{\text{R}})}{\mathrm{d}I_{\text{D}}} = \frac{\mathrm{d}V_{\text{J}}}{\mathrm{d}I_{\text{D}}} + R_{\text{d}}$$

Solving for the resistance

$$R_{\text{d}} = \frac{\mathrm{d}V_{\text{D}}}{\mathrm{d}I_{\text{D}}} - \frac{\mathrm{d}V_{\text{J}}}{\mathrm{d}I_{\text{D}}}$$

From the high-level injection relationship,

$$I_{\text{D}} = I_{\text{s}} \exp\left(\frac{qV_{\text{J}}}{2kT}\right)$$

and

$$\frac{\mathrm{d}V_{\text{J}}}{\mathrm{d}I_{\text{D}}} = \frac{2kT}{q}\frac{1}{I_{\text{D}}}$$

Substituting in these expression, solving for the diode series resistance term as

$$R_{\text{d}} = \frac{\mathrm{d}V_{\text{D}}}{\mathrm{d}I_{\text{D}}} - \frac{2kT}{q}\frac{1}{I_{\text{D}}}$$

4.2 ESD DIODE DESIGN: ANODE

4.2.1 p^+ Diffusion Anode Width Effect

In the design of the diode structures, the width of the p^+ anode influences the ESD robustness of the diode design [5]. Based on the diode equation under high-level injection, the current through the diode should increase proportionally to the area of the anode region. But, if the summation term of the product of the diode current and internal resistance is significant, the operation will not be linear in the area. Note from

$$I_D = I_s\left\{\exp\left(\frac{qV_D - \sum I_D R_i}{kT}\right) - 1\right\}$$

if

$$qV_D \gg \sum I_D R_i$$

Hence to design a diode to be effective and be proportional to the area, the voltage drops in the diode structure must be minimized. As a result, there is an anode width where this is satisfied. The internal resistance in the diode structure can be minimized using a high contact density, low sheet resistance salicide films, and interconnects that distribute the current effectively through the diode structure [1–3,14].

In the experimental work, using shallow trench isolation (STI) bound p^+ anode diode structure, as the p^+ implant anode area increased, the human body model (HBM) ESD failure level increased linearly, as shown in Figure 4.2 [4,5]. In this case, the length-to-width

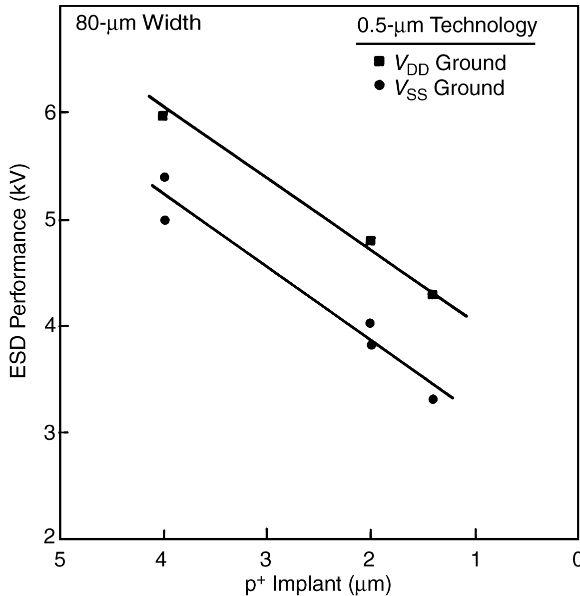

Figure 4.2 ESD robustness as a function of width variation of the diode structure

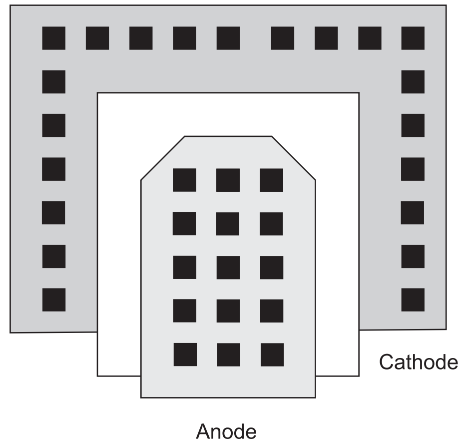

Figure 4.3 Cartesian array of contacts in a ESD anode design

ratio of the anode was varied from 100:1 to 50:1 (e.g., electrical connections were initiated perpendicular to the longer dimension).

From this experimental results, there is a design regime where the ESD robustness of the structure varies with the physical anode width.

4.2.2 p^+ Anode Contacts

Placement of the physical contacts can influence the current in the anode and cathode regions under high current conditions. Non-uniformities in the current distribution lead to local non-uniform heating in the salicide film. The contact design layout can be formed in a Cartesian row formation or skewed. In a Cartesian row formation, the contacts are placed equally spaced in both the x- and y-direction side by side. In this formation, the maximum contact density can be placed on the ESD diode structure. Figure 4.3 shows an example layout of the Cartesian contact configuration.

In an alternative contact design, the contacts are staggered so that each row or column is shifted. In this contact formation, the current uniformity is more evenly distributed. Kreiger proposed the staggered design concept to provide an improved uniformity in the structure. Figure 4.4 shows an example of a staggered or skewed contact design.

4.2.3 p^+ Anode Silicide to Edge Design

In many processes, such as LOCOS processes, where there is a concern that an ESD failure mechanism may occur at the triple point between the metallurgical junction, the salicide, and the isolation, ESD diode structure are designed to avoid formation of silicides near the anode-to-isolation edge [1,14]. In LOCOS processes, etch processes can pull back the isolation structure, leading to the salicide formation being to close to the metallurgical junction. The LOCOS bird’s beak effect can lead to a reduced space between the silicide and

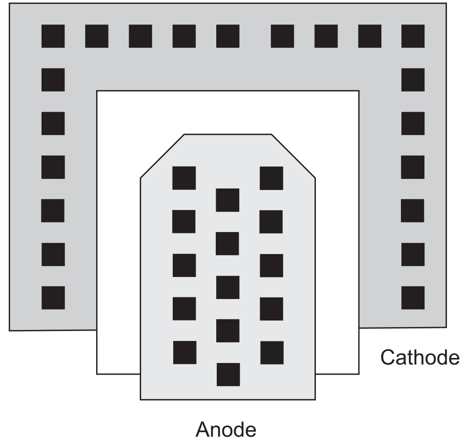

Figure 4.4 Skewed (or staggered) rows of contacts for improved current uniformities

the metallurgical junction. In STI, STI pull-down can also make the silicide depth approach the metallurgical junction depth, decreasing the effective junction depth. This can lead to ESD-induced semiconductor process variation, reduced worst-case ESD robustness, and latent failure mechanisms. These type of ESD failures will be sensitive to salicide junction film thickness, and junction depth variations [1,14].

To avoid semiconductor process from causing early ESD failures, diode designs can be formed by preventing the silicide formation at the junction edges. Figure 4.5 shows an example of a diode design with the silicide formation blocked at the edges of the anode structure. In this fashion, the silicide is formed under the complete diode area to provide a low-series resistance diode structure, and provide a good contact-silicide-contact resistance,

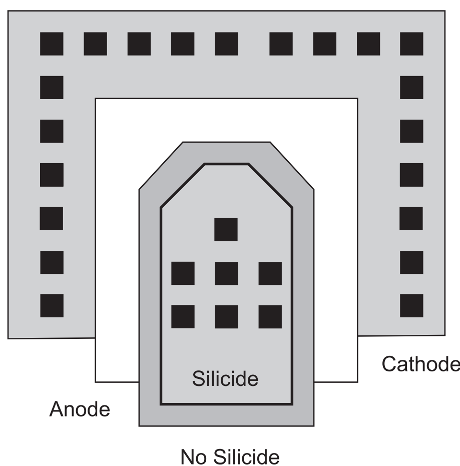

Figure 4.5 Diode design with the silicide formation blocked at the edges of the anode structure

Table 4.1 HBM ESD robustness of a STI-bound diode structure as a function of the isolation width

p^+ to n^+ isolation width (μm)	Reference V_{DD} polarity (+) (kV)	Reference V_{DD} polarity (−) (kV)	Reference V_{SS} polarity (−) (kV)
2.4	4.2	−10	−9.5
2.1	4.0	−10	−9.5
1.8	4.2	>−10	−10

but avoids the isolation edge issues. This can be achieved using a silicide block mask or any other mask, which occurs prior to the silicide formation process step.

4.2.4 p^+ Anode to n^+ Cathode Isolation Spacing

In the ESD design, the p^+ anode and n^+ cathode diffusion spacing are separated and defined by the isolation region. This isolation can be LOCOS or STI isolation regions. In the case of LOCOS isolation, as the spacing between the p^+ anode region and the n^+ cathode contact region decreases, the depletion region can be influenced by the spacing. In the diode structure, the p^+ anode and n^+ cathode contact regions extend below the isolation structure [1]. A metallurgical junction is formed with a lateral $p^+/n^-/n^+$ junction. Hence, as the spacing decreases, it is anticipated that the breakdown voltage of the junction will decrease at small spacings.

In STI-defined diode structures, the doped regions do not extend below the isolation region [1]. As the spacing decreases, the diode series resistance will decrease. Table 4.1 shows experimental results of an STI-bound diode structure as a function of isolation spacing. Based on the understanding of LOCOS isolation, a potential ESD degradation effect at small spacings was anticipated. From the experimental data, this was not evident in the design.

4.2.5 p^+ Anode Diode End Effects

In p^+ anode diode structures, end effects and end failure mechanism are evident in diode design [2–3]. In a design where the p^+ to n^+ spacing is small compared to the lateral dimension, the current flow to first order will be two-dimensional. This assumes uniform current flow in the p^+ anode structure perpendicular to its isolation interface. When the length is large relative to the spacing, this is a good first-order assumption. Along the length of the structure, the contact-to-STI space is uniform. At the end of the p^+ anode diode structure, the last contact is equidistant from three edges on the side of the n^+ cathode. In the case of the corners, current flows in three-dimensions introducing a three-dimensional effect and is the location of the failure mechanism. In LOCOS isolation, the metallurgical junction is cylindrical on the edges and spherical on the corners. In STI-defined diodes, the edges are planar surfaces, and the corners are cylindrical. At the STI-defined corner, the cylindrical region has a higher electric field. Figure 4.6 shows the atomic force microscope (AFM) image damage of the corner of the diode structure [2,3].

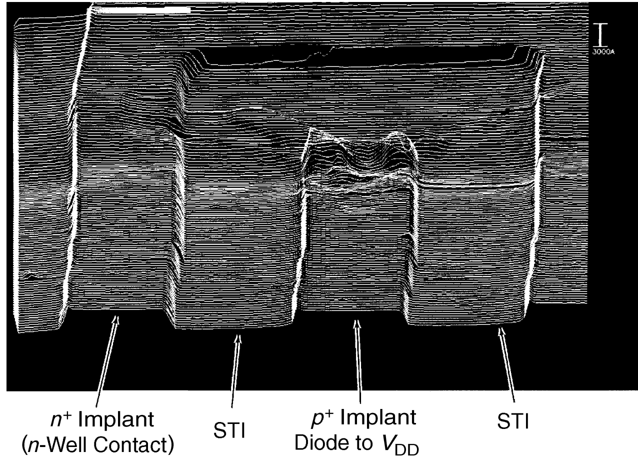

Figure 4.6 Atomic force mapping (AFM) image of diode failure

To eliminate the three-dimensional effect, various ESD design solutions can be introduced:

- Corner rounding of the p^+ anode design using 45-degree chamfers instead of 90-degree corners.
- Reduction of contact density in the n^+ cathode contact.
- Displacement of the last contact away from the p^+ anode/STI edge.
- Salicide removal on the p^+ anode or n^+ cathode contact.
- Increase in the p^+ anode to n^+ cathode contact space (e.g., a wider STI region).
- Increase the total number of diffusion fingers (e.g., total perimeter) to lower the total current density in any given region of the structure.

The first recommendation reduces the sharpness of the corner region. The other items increase the series diode resistance at the corner, which creates a closer matching of the resistance of the corner and the linear region. All the above items were experimentally introduced to eliminate the ESD failure mechanism. The most effective was the displacement of the last contact from the corner of the device. In this case, the current needed to flow through the salicide and p^+ implant region to reach the n^+ cathode contact. Prior to the elimination of the failure mechanism, the ESD failure introduced damage up to three contacts from the corner as well as salicide damage. By removing the last three contacts from the corner, this eliminated the failure mechanism.

Increasing the total perimeter and increasing the number of p^+ anode fingers reduces the total current density in the structure as well as introduces more total number of corner regions. Instead of optimization of the corner region, the addition of many more corners and more total perimeter leads to a reduction of the total current density and the failure mechanism.

As the diffusion width is scaled, the ability to chamfer the corners at 45 degrees is not possible in minimum width anode fingers. Hence, for minimum design width p^+ anode regions, the designs must reintroduce 90 degree corners. Other features, such as the spacing of the last contact to the anode corner boundary, provide adequate resistance, so chamfering is not required.

4.2.6 Circular and Octagonal ESD Diode Design

Alternative ESD diode design are preferred to provide good ESD results and low capacitance. These include non-rectangular design layouts. Non-rectangular ESD designs can include waffle design [39], circular design [40], and *n*-sided polygons [41]. Octagons are common by removal of the corners from a square shape. Non-rectangular designs have the following ESD advantages:

- Lower current density due to the cylindrical and spherical current distribution.
- Avoidance of isolation corner effects.
- Placement in small areas where circles or octagons can be easily placed.
- Self-enclosed structure avoiding isolation issues, wasted guard ring space, or adjacent structure parasitic interactions.

In the non-rectangular implementations, such as in a circular design, the ESD structure can consist of a center circle followed by concentric annulus of regions around the center region. The concentric circles can be anodes, cathodes, isolation, or guard ring structures. The disadvantages of this design style are the following:

- Design width and area limitations.
- Computer-aided designs (CAD) issues exist with non-rectangular shapes (e.g., polygons, non-Euclidean orientations, octagons, and circle shapes).
- CAD design automation convergence and process time.
- CAD device and circuit model issues.
- CAD-parameterized cells for non-rectangular shapes is not always possible.
- Lithography and etch orientation issues.
- Wiring limitations.

To avoid the design layout and CAD limitations, custom ESD designs are utilized with fixed sizes. These fixed design sizes require a custom device and circuit model.

4.3 ESD DIODE DESIGN: INTERCONNECT WIRING

The wiring of an ESD structure is critical to provide current uniformity and achieve a high ESD robustness per unit micron of structure area. The interconnect wiring in ESD design has the following roles:

- Establish current density uniformity.
- Establish a low diode series resistance.
- Produce internal ballasting to self-limit current non-uniformities.
- Avoid ESD design uniformities (e.g., corners, edges) from limiting the ESD robustness of the structure.

Various wiring strategies can be introduced into the diode design. Depending on the metal resistance, the contact resistance, the salicide sheet resistance, and the p^+ anode sheet resistance, the different design patterns may or may not be successful. The metal pattern design can be of the following nature:

- Parallel wiring.
- Anti-parallel wiring.
- Quantized tapered parallel and anti-parallel wiring.
- Continuous tapered anti-parallel and parallel wiring.
- Perpendicular (or broadside) wiring with center-fed design.
- Perpendicular (or broadside) with uniform metal width.
- Perpendicular (or broadside) wiring with H- and T-shape extensions.

4.3.1 Parallel Wiring Design

The ESD p^+ anode and n^+ cathode can be wired in a fashion where the current flows down the wire interconnect of the p^+ anode (Figure 4.7). The current then flows from the wire interconnect and then perpendicularly across the p^+ anode to n^+ cathode STI spacing. In the parallel wire configuration, the current then flows in a parallel fashion down the n^+ cathode metal pattern, which runs the length of the n^+ cathode; this is analogous to the MOSFET (as was discussed in the Chapter 3 on MOSFET current distribution). In this fashion, the ESD current flows from the left-hand-side of the end of the diode, and exits on the right-hand-side of the diode structure. In this design style, the anode or cathode can be mirrored forming a U-shape or horse-shoe design. This will lead to an unequal number of anode and cathode fingers.

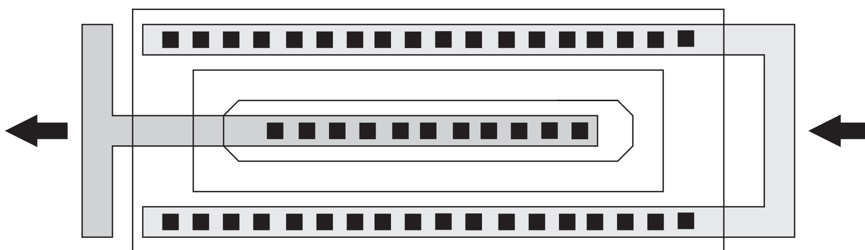

Figure 4.7 Parallel wiring design

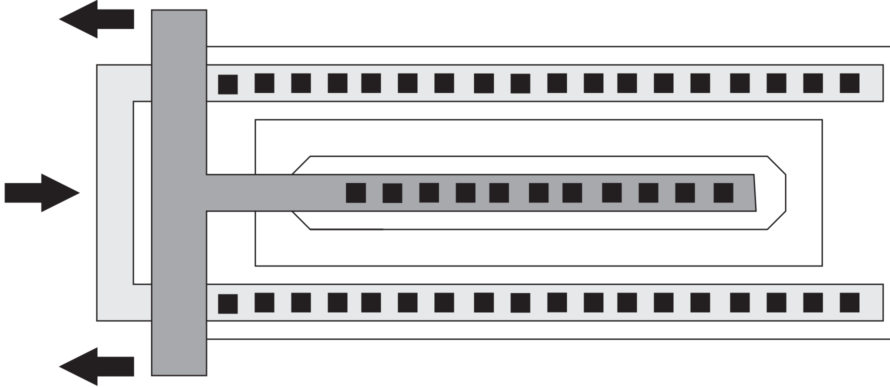

Figure 4.8 Anti-parallel metal wiring design

4.3.2 Anti-Parallel Wiring Design

The ESD p^+ anode and n^+ cathode can be wired in a fashion where the current flows down the wire interconnect of the p^+ anode (Figure 4.8). The current then flows from the wire interconnect and then perpendicularly across the p^+ anode to n^+ cathode STI spacing. In the anti-parallel wire configuration, the current then flows in a parallel fashion down the n^+ cathode metal pattern, which runs the length of the n^+ cathode, but exits the same side as it enters. For example, the ESD current flows from the left-hand side of the end of the diode, and exits on the left-hand side of the diode structure. In this design style, the anode or cathode can be mirrored forming a U-shape or horse-shoe design. For example, in an N finger p^+ anode design, there may be $N + 1$ cathode fingers.

In the concept of parallel and anti-parallel wiring of an ESD diode, the ESD design forms a resistive–conductance (RG) transmission line down the length of the structure [12]. The transmission line can be modeled as a series of resistor elements with diode elements between the top and bottom of the transmission line. The disadvantage of this implementation is that the voltage drops along the length introduce voltage non-uniformities.

4.3.3 Quantized Tapered Parallel and Anti-Parallel Wiring

To minimize the voltage drops along the length of the parallel and anti-parallel configuration, the metal line at the cathode and anode can be widened incrementally along the length. For example, the anode metal can be a given width at the electrical connection and incrementally tapers to a smaller width as the metal continues down the length. Equivalently, as the anode metal width is decreased, the cathode metal width increases, decreasing the voltage drop along the cathode metallization (Figure 4.9).

4.3.4 Continuous Tapered Anti-Parallel and Parallel Wiring

In the above implementation, the wiring was tapered in a quantized fashion to maintain a piece-wise rectangular metal shape. The same concept can be introduced where the metal

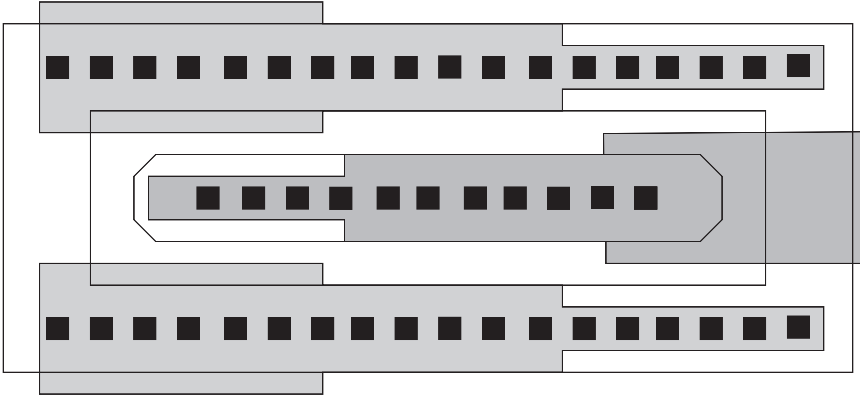

Figure 4.9 Quantized tapered anti-parallel and parallel wiring

width is a uniform function of position [12,13] (Figure 4.10). In this case, the metal width is defined as $W(x)$ where x is the position along the ESD diode anode finger. The advantage of this implementation is a more uniform solution and avoidance of discontinuities.

The disadvantage of these designs is the limited metal width, and at times significant voltage distribution drops along the structure. This can lead to a poor ESD robustness per unit micron of design area. In some cases, the design is limited to a given dimensional range of operation, and if the design remains in the dimensional space, no penalty is observed.

4.3.5 Perpendicular (or Broadside) Wiring with Center-Fed Design

In a perpendicular- or broadside-wiring pattern design, the ESD current flows from the pad to the ESD network along the width of the design (Figure 4.11). The current flows in the

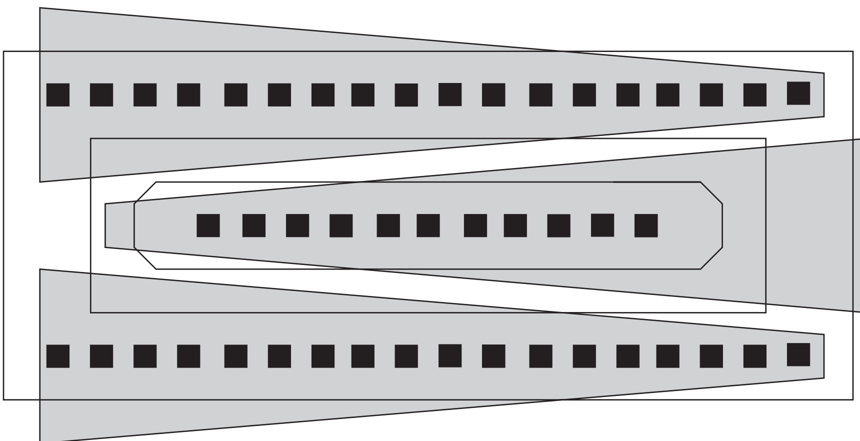

Figure 4.10 Continuous tapered anti-parallel and parallel wiring

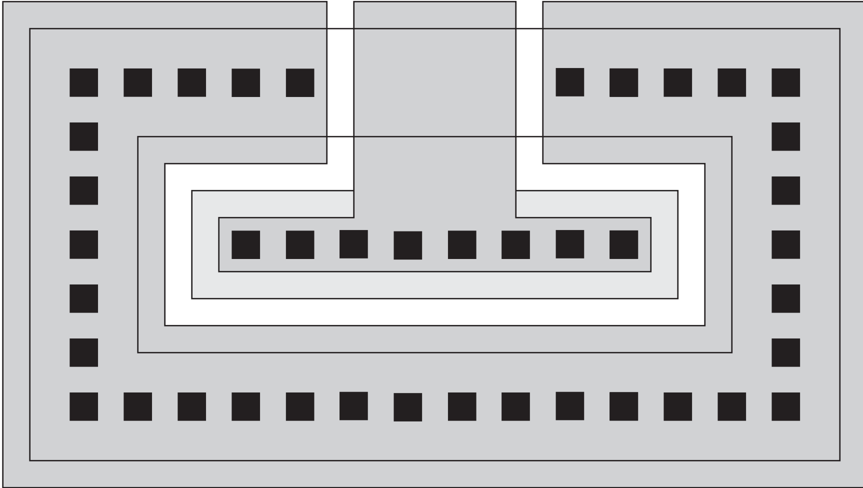

Figure 4.11 Perpendicular (or broadside) center-fed ESD metal design

same direction as the p^+ to n^+ cathode diode region. In a center-fed design, the input wire enters the left-hand side with the wide wire entering the center of the design. The current then flows to the n^+ cathode, which is connected on the top and bottom of the cathode, and exits the right-hand side of the structure. The disadvantage of this design is that the current from the anode has difficulty flowing to the cathode structure, and the majority of the contacted p^+ anode area needs to distribute the current perpendicular to the current flow to be near the n^+ cathode area. This design can be improved by placing a first metal line along the anode and cathode and wire from the second level of metal. Again the disadvantage is that the current must now flow perpendicular along the first level metal to redistribute across to the cathode region. For high perimeter-to-area diode structures, this wiring design style has demonstrated significantly poor ESD robustness in advanced CMOS technology. An additional issue with this method is that there is no self-ballasting within the design due to the wide metal input shape and wide metal output shape.

4.3.6 Perpendicular (or Broadside) with Uniform Metal Width

In a perpendicular- or broadside-wiring pattern design, the ESD current flows from the pad to the ESD network along the width of the design [6–10] (Figure 4.12). The current flows in the same direction as the p^+ to n^+ cathode diode region. In this design implementation, the anode and cathode wiring is alternating across the design of a given width and space. The metal line can be a first or second level of metal. In the case of a single metal level, contacts are placed under either the p^+ anode or the n^+ cathode in an alternating fashion. In this design implementation, when the p^+ anode interconnect passes over the n^+ cathode, no contacts are placed on the n^+ cathode and vice versa. In this fashion, the contact density is less than 50% coverage (e.g., no contacts exist in the metal line to metal line space). A first disadvantage of this design is that as the line width is wider, the spacing between the p^+ anode and n^+ cathode contact increases. In this design implementation, the best design

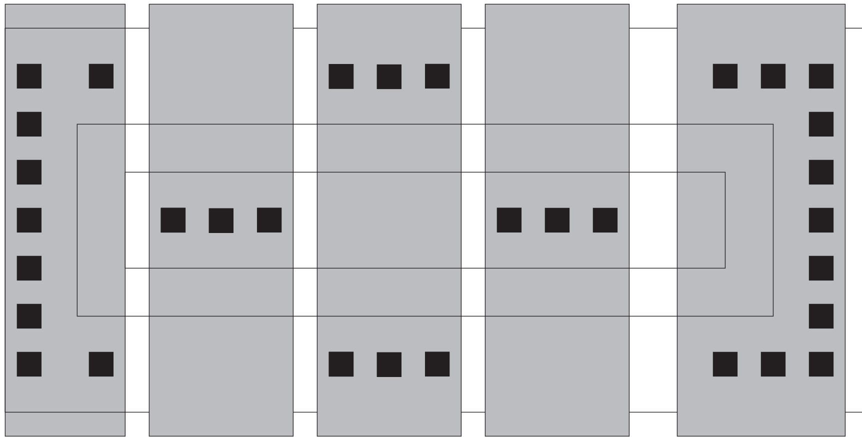

Figure 4.12 Perpendicular (or broadside) with uniform metal width

is achieved by using a large number of narrow interconnect widths. To improve on the contact coverage, a first-level metal with full contact density can be placed on the anode and cathode fingers, with the contacting to the respective wiring is completed on a second-metal level. In this fashion, full contact density as well as a lower lateral resistance is achieved from the first-level metal. Again, the disadvantage is the current must now flow perpendicular along the first-level metal to redistribute across to the cathode region. In this design style, the M2 wiring and M1 wiring patterns introduce some self-ballasting within the design.

4.3.7 Perpendicular (or Broadside) Wiring with T-Shaped Extensions

In a perpendicular- or broadside-wiring pattern design with T-shape extensions, the ESD current flows from the pad to the ESD network along the width of the design [2–5,19–21,42] (Figure 4.13). The current flows in the same direction as the p^+ to n^+ cathode diode region. In this design implementation, the anode and cathode wiring is alternating across the design of a given width and space. A distinction from the other design without the T-shape extensions, this metal design then introduces metallization lateral to the current flow. This wider metal level then allows to contact the p^+ and n^+ cathode region with a large number of p^+ and n^+ contacts at a minimum spacing between them; this produces the lowest lateral resistance and the highest ESD results. The metal line can be a first or second level of metal. In the case of a single metal level, contacts are placed under either the p^+ anode or the n^+ cathode in an alternating fashion. Although the contact density is not 100% of the area, the number of minimum spaced p^+ to n^+ contact spacings is the highest. The ESD electrothermal damage patterns of molten silicon show that the damage occurs between the local anode and cathode contacts. This design can be further improved by introduction of either ‘‘M-zero’’ wiring (e.g., local interconnect) or a two-level metal design with 100% contact density.

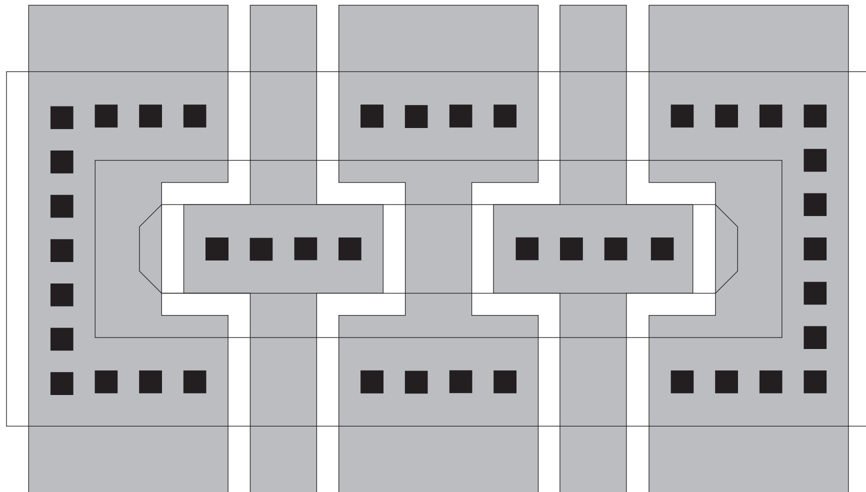

Figure 4.13 Perpendicular (or broadside) wiring with T-shape extensions

4.3.8 Metal Design for Structures Under Bond Pads

The design of ESD diode structures under bond pads can be constrained based on the metallization design rules in a given technology [19–21,42–46]. For structures under bond pads, the metal level and metal width may be constrained to avoid insulator cracking. In an interconnect system with aluminum metallurgy and silicon dioxide, large area regions of metal under insulators lead to the material deflection of the insulator above during loading from bonding processes. The insulator film can be modeled as a material beam with the two ends rigid. The mechanical bond pad load can be modeled as a uniform load along the length of the insulator region. In this case, the mechanical deflection of the film can be determined, with the maximum deflection occurring at the center of the bond pad. As the length of the bond pad increases, the deflection at the center also increases. When the material exceeds the maximum yield stress, cracking occurs in the insulator leading to material failure. The deflection is a function of the bond load, and inversely proportional to the second moment of inertia of about the material axis, and the elastic constant. Additionally, as the insulator film is farther from the region of mechanical loading (e.g., top surface), the lower is the likelihood of failure. As a result, the lower the metal level, the lower is the mechanical failure risk.

ESD designs under bond pads are at time constrained to given metal levels and pattern designs. In the case of aluminum interconnects, low-level metal films are suitable to avoid mechanical failure. Additionally, to minimize insulator deflection, no large area regions are used for metallization patterns. Many of the aforementioned design patterns are suitable. A metal pattern not suitable, for example, is the center-fed metal pattern, which introduces large area metal under the insulator regions.

4.4 ESD DIODE DESIGN: POLYSILICON-BOUND DIODE DESIGNS

Polysilicon-bound anode diode structures were introduced to avoid salicide issues in STI structures [14]. Polysilicon-bound anode structures can be formed in two different fashions.

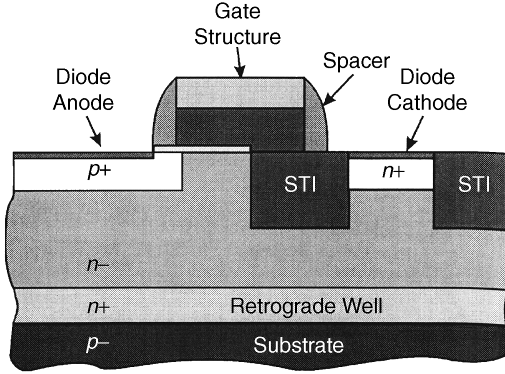

Figure 4.14 Polysilicon-bound anode structure diode

A first structure introduced a polysilicon-bound anode structure where the polysilicon MOSFET gate structure overlaps the STI region to avoid the triple point formed between the p^+ implant, the salicide, and the STI region (Figure 4.14). Note in this structure, the n^+ cathode contact remains bound by STI. This structure prevents the salicide from approaching the perimeter where the polysilicon MOSFET gate structure serves as a salicide-blocking mask. As the silicide is deposited, it extends over the MOSFET spacer and gate region, and not penetrating into the p^+ silicon implant region. The role of the STI shape in this structure serves two purposes. The first purpose is to prevent the flow of surface currents. The STI region forces the current around the isolation to reach the n^+ cathode contact. This forces the current to flow vertically through the heavily doped well region. The second purpose is to define the n^+ cathode contact region.

In a second implementation, as shown in Figure 4.15, the polysilicon MOSFET gate structure defines both the p^+ anode and n^+ cathode regions [14,15]. The advantage of this structure is twofold. First, a higher density diode structure is achieved by elimination of the STI region. Second, the series resistance between the anode and cathode is reduced, since the current can flow laterally across the surface. Given that the surface current leads to high

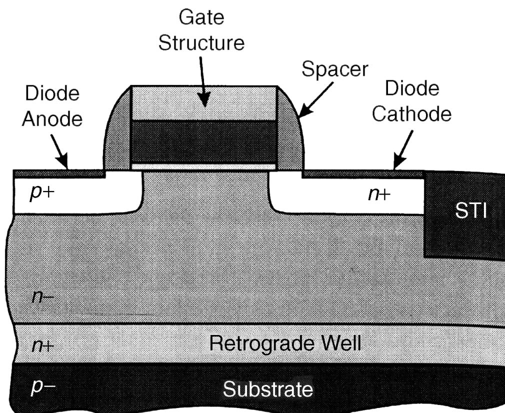

Figure 4.15 Polysilicon-bound anode and cathode structure diode

current density and current crowding, early ESD failure could occur. In the experimental results, there was no concern with this potential issue. In this fashion, the left-hand side of the structure has the *p*-channel MOSFET implants, and the right-hand-side of the structure has the *n*-channel MOSFET implants. A block mask is formed over the top of the structure to form the anode and cathode structure.

In this structure, all of the additional MOSFET implants are present in the ESD design. This ESD design structure will contain low-doped drain (L_{DD}), extension implants, and halo implants. These implants will influence the surface physics and capacitance near the surface of the device. Note that in this structure, the cathode region is either an *n*-well or *p*-well region. As a result, one of the halo implants is the opposite of the cathode region doping polarity. This extra resistance region can be eliminated to lower the ESD diode device resistance. In this implementation, there is a ‘‘good halo’’ and a ‘‘bad halo.’’ The good halo lowers the diode series resistance, and the bad halo counter-dopes the well structure. This polysilicon-bound diode structure can be formed as a $p^+/n^-/n^+$ diode structure or a $p^+/p^-/n^+$ diode structure.

4.4.1 ESD Design Issues with Polysilicon-Bound Diode Structures

In these polysilicon-bound diode structures, there are ESD design issues. The following ESD design issues exist with these diode structures:

- Physical contact to the MOSFET gate structure in the enclosed gate region.
- Choice of electrical connection of the polysilicon MOSFET gate structure.
- Dielectric over-voltage of the polysilicon gate structure.

For the first item, the ESD design encloses the p^+ anode with a polysilicon ring. Electrical contacts of gate structures are not used. Hence, to electrically connect to these gate structures, a STI island must be placed in the channel region. In this fashion, electrical contacts can be placed to electrically connect the structure.

A second issue is the electrical connection of the gate structure. The choice of electrical connection of the gate structure influences the loading, operation, and electrical overstress or ESD failure mechanisms. The gate structure can be connected to the anode, the cathode, power rails, or left floating. The over-voltage and ESD issues can be resolved using circuit solutions, which are less costly. In many technologies, allowing a gate structure to float is a concern for semiconductor manufacturing charging issues and antennae effects. As a result, the use of a floating polysilicon MOSFET gate structure in many technologies is not allowed.

For example, the polysilicon MOSFET gate structure can be connected to the n^+ cathode region. In the case of a double-diode implementation, two polysilicon-bound diode structure can be used. A first polysilicon-bound diode structure is used between the input pad and the V_{DD} power supply, whose anode is connected to the input pad and the cathode is connected to the V_{DD} power supply. A second polysilicon-bound diode structure is placed where the cathode is connected to the input pad, and the anode is connected to the V_{SS} power rail. In this implementation, as the input pad undergoes a voltage undershoot, the voltage across the top diode oxide region is $V_{DD} + V_{under}$, where V_{under} is the undershoot voltage magnitude. As

the input pad undergoes a voltage overshoot over the power supply voltage, the voltage across the gate of the lower polysilicon diode structure is $V_{DD} + V_{over}$, where V_{over} is the overshoot voltage. In this implementation, the gate dielectric is overstressed during the overshoot event. Note that the diode voltage drop will limit the overshoot and undershoot events. If the sum of the diode turn-on voltage and the IR drop across the diode structure is less than the overshoot, the overshoot will be constrained by the structure turn-on. Hence, depending on the size of the overshoot current and the resistance of the ESD element, voltage clamping will occur from the ESD devices. But, as the oxide thickness scales, the allowed voltage across the dielectric will be limited.

4.5 ESD DIODE DESIGN: *n*-WELL DIODE DESIGN

A second diode structure of importance is the *n*-well diode used for negative discharging into the chip substrate [1–15]. *n*-well ESD diodes extend below the surface isolation (e.g., ROX, LOCOS, or STI), making them insensitive to *n*-channel MOSFET source/drain dose and silicide penetration [1]. *n*-well diode structures have been effective solutions for allowing ESD current to flow into the bulk chip substrate. *n*-well ESD design and the wiring pattern are significantly influenced by the substrate material and its doping concentration.

4.5.1 *n*-Well Diode Wiring Design

The wiring pattern in an *n*-well design with the electrical contact to the p^- substrate contact can follow the same design pattern as shown with the STI-bound p^+ anode diode structure.

- Parallel wiring.
- Anti-parallel wiring.
- Quantized tapered parallel and anti-parallel wiring.
- Continuous tapered anti-parallel and parallel wiring.
- Perpendicular (or broadside) wiring with center-fed design.
- Perpendicular (or broadside) with uniform metal width.
- Perpendicular (or broadside) wiring with H- and T-shape extensions.

As was discussed in the case of the STI-bound p^+ anode, similar metal design patterns can be implemented for the *n*-well cathode structure. The identical issues are present with these structures but there are some important differences:

1. The effectiveness of *n*-well diodes in both p^- or p^+ substrates is significant, leading to a lower perimeter requirement. This minimizes the need for a high number of multiple fingers and complex metal patterns.
2. The width of the *n*-well is limited by implant, diffusion, and process limitations. As a result, the width of the *n*-well regions are significantly wider than the minimum width

formed from a STI-defined shape (e.g., n^+ or p^+ region). As a result, the metal width in these designs may not require tapering and other techniques.

3. In a p^- epitaxial/p^+ substrate wafer, the effectiveness of the substrate allows for no need for a surface electrical contact local to the ESD network.

Hence, the ESD effectiveness of these structures allows for a significant smaller perimeter and area with respect to the STI-bound p^+ anode area. As a result, the bussing drops and multi-finger issues are reduced in these implementations. Experimentally, again the broadside center-fed n-well diode performance was significantly lower than the broadside wiring with T-extensions.

In a p^- epitaxial/p^+ substrate wafer, the substrate serves as a good electrical and thermal shunt for the ESD current. As a result, electrical connections to the substrate local to the n-well diode structures are not necessary. As a result, there is no need to have V_{SS} wiring planes or grids interwoven into the ESD design [1–22]. Hence, this simplifies the metal pattern and prevents the need for integration of the V_{SS} wires into the ESD diode network. In the case of the n-well diode, the anode region does not need to be electrically connected locally. Additionally, the ESD robustness of the diode structure in a p^- epitaxial/p^+ substrate wafer is $2\times$ superior to a low doped p^- wafer [1].

As a result, the size of the structure is smaller, making it less of a need to introduce parallel, and anti-parallel connections with quantized steps, or continuous tapering. Experimental results with n-well diode structures in p^- epitaxial/p^+ substrate wafer demonstrated that ESD results were superior when there was no local STI-bound p^+ contact electrical connection to V_{SS} [2–4]. It is postulated that the grounding of the V_{SS} rail leads to local current crowding near the n-well diode structure, limiting the ESD robustness of the n-well diode structure [2–4]. It is believed that a lower current density and less current crowding were achieved using the bulk substrate as the thermal and electrical current shunt during negative pulse ESD testing relative to V_{SS} power rails.

In a p^- substrate non-epitaxial wafer, a local p^+ substrate contact can be introduced. As a result, the different metal patterns can be implemented for the n-well diode structure for the anode and cathode. This lessens the design freedom obtained in the case of the p^+ substrate wafers. From experimental work, the ESD robustness of the n-well diode in a p^- wafer is approximately $2\times$ lower. Hence to achieve comparable ESD robustness as achieved in a p^- epitaxial wafer, the n-well diode structure will require double the design area. In this case, the total area of this structure is still significantly less than that needed for a STI p^+ anode structure. As a result, the metal patterns can remain simple.

In the wiring decision, the choice of the wiring may be defined by the wiring channels and pattern used for the STI-bound p^+ anode design. For example, in a double-diode implementation, using a STI-bound p^+ anode diode and an n-well diode, the same metal pattern (e.g., metal width, level, and metal-to-metal space) may be used for both for wire-ability.

4.5.2 *n*-Well Contact Density

In an n-well diode design, the width of the n-well is limited by the minimum n-well, which can be formed in a technology. Whereas in a STI-defined p^+ anode, a minimum width can be

utilized, and the *n*-well diode will be significantly wider. As a result, multiple rows of contact structures as opposed to a single row can be utilized without additional area penalty.

4.5.3 *n*-Well ESD Design, Guard Rings, and Adjacent Structures

In an *n*-well ESD design, the adjacent structures can influence the function of the *n*-well ESD diode. *n*-well diode structures are typically used for negative pulse ESD events. The negative pulse events lead to the forward bias of the *n*-well to p^- substrate metallurgical junction. Holes from the substrate flow to the input pad, and electrons from the cathode flow into the p^- substrate region. The anode resistance and the current distribution influence the effectiveness of the *n*-well diode structure. For the case when the power supply rail (e.g., V_{DD}) is a ground reference, the electrons discharged into the p^- substrate flow to the grounded reference. In many cases, *n*-doped regions are electrically connected to the V_{DD} power rail.

Guard ring structures can be formed around the *n*-well-to-substrate ESD diode to collect the injected electrons in the substrate [2–5]. When a semiconductor chip is powered, guard rings electrically connected to the V_{DD} power supply, act as a collector of minority carrier electrons in the p^- substrate during undershoot conditions. The *n*-well ESD diode, the p^- substrate, and the *n*-type guard ring form a lateral parasitic bipolar transistor, where the *n*-well-to-substrate ESD diode serves as the emitter region, the p^- substrate serves as the base region, and the *n*-doped guard ring structure serves as the collector region. The guard ring structure can be an STI-defined *n*-implant, *n*-well, or a triple-well isolation *n*-band region. The ability of the adjacent *n*-doped region to collect minority carrier electrons is a function of the collector depth, the width, the spacing relative to the *n*-well diode, the bias condition, and the substrate doping concentration and substrate lateral and vertical profile. The guard ring efficiency to collect minority carriers should increase with increasing collector depth and width, and decreasing spacing between the guard ring and the ESD *n*-well diode. For example, an *n*-well guard ring will serve as a superior guard ring compared to the STI-bound *n*-diffusion due to the physical size and depth of the structure. In the design of the guard ring structure, the choice of the type of structure and the lateral spacing has a large role in its effectiveness.

For ESD events, the placement of the adjacent structure can modulate the ESD HBM robustness. Wafer-level ESD testing of an *n*-well ESD diode on a p^- epitaxy/p^{++} substrate wafer demonstrated a decrease in the HBM robustness as the space between the *n*-well diode and an *n*-well guard ring structure decreased (Figure 4.16). From an electrical perspective, the smaller base width should demonstrate an improved ESD result instead of an ESD degradation; but if the failure of the structure is a function of higher current density, self-heating, and smaller physical volume, then it plausible that the ESD failure for the smaller spacing is logical and not counter-intuitive.

In the physical design of the *n*-well guard ring structure, the STI-defined *n*-diffusion serves as the electrical contact to the well structure, and a maximum contact density is used to allow for a low resistance collector region. When low contact density is used, or one-sided electrical connections, the effectiveness of the collector structure is degraded.

In ESD designs, when an *n*-well guard ring is not placed around an *n*-well ESD diode structure, negative pulse events from chips, cards, cables, or systems can lead to minority-carrier injection, leading to reliability concerns. These concerns can consist of MOSFET

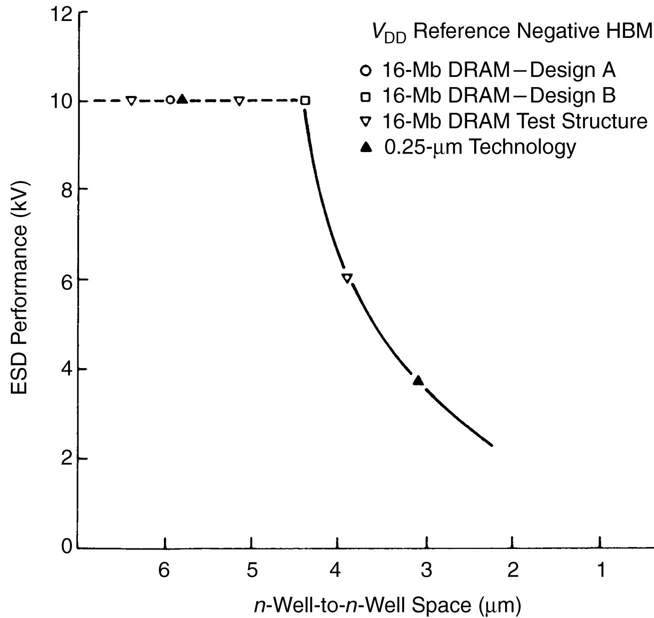

Figure 4.16 ESD HBM results of an *n*-well diode as a function of the lateral spacing to the *n*-well guard ring structure

threshold shifts, noise, or latchup. Additionally, for negative mode ESD testing relative to the V_{DD} power supply rail, poor ESD results can occur if there is no defined current path to the V_{DD} power rail.

Utilizing adjacent structures that contain circuitry (e.g., *n*-well tubs connected to V_{DD} power rails) can also play a role of a region to act as a guard ring or discharge path to the V_{DD} power supply.

This can save chip area in ESD design but the following design practices must be followed to be effective:

- The spacing of the *n*-well ESD diode relative to the adjacent structure and the guard ring should be symmetrically matched to provide uniform current flow to both the adjacent structures on both sides of the ESD *n*-well diode.
- Elements contained in the adjacent structure must be electrically connected or spaced to avoid potential parasitic *pnpn* initiation (e.g., CMOS latchup).

An ESD *n*-well diode can be formed with a guard ring structure on one side, and an *n*-well tub on the other side. From a design symmetry perspective, the spacing between the ESD *n*-well diode relative to the *n*-well tub and the *n*-well guard ring is equal. In this fashion, the two lateral bipolar *npn* base widths and areas are matched preserving symmetry. Electrically, the two *n*-well regions also are connected to the same power supply rail. On the second issue, although the parasitic *pnpn* is physically present, the electrical connections are not in such a fashion that latchup can be initiated within the structure. In this case, the

p^+ n-well diode is electrically connected to the n-well ESD diode. The electrical connections are such that the lateral *pnpn* anode and *pnpn* cathode are electrically connected. From the experimental damage patterns, the molten silicon can be observed symmetrically from the n-well ESD diode to both the n-well guard ring structure and the interior n-well tub.

4.6 ESD DIODE DESIGN: n^+/p SUBSTRATE DIODE DESIGN

In an n^+/p^- substrate diode ESD design, the same issues and characteristics as discussed for the n-well/p^- substrate apply to the n^+ diode region [2–5]. There are some ESD design distinctions between the n-well ESD diode and the n^+ diffusion diode. The n^+ diffusion ESD diode is sensitive to the isolation structure. The isolation structure will influence:

- Silicide penetration.
- Breakdown voltage.
- Lateral thermal dissipation.

n-well ESD diodes extend below the surface isolation (e.g., ROX, LOCOS, or STI), making them insensitive to n-channel MOSFET source/drain dose and silicide penetration. No special silicide masks are needed for n-well diode structures. In n^+ ESD diode structures, these can be sensitive to the MOSFET source/drain dose and energy, refractory metal species, silicide thickness, hot process, and the isolation lateral or vertical control (e.g., LOCOS lateral bird's beak and STI pull-down mechanisms).

As a result, in LOCOS-defined n^+ diffusion ESD diodes, silicide blocking masks can be placed to reduce the sensitivity of silicide penetration into the metallurgical junction from LOCOS pull-back or vertical silicide penetration. Three different silicide masking designs can be used:

- Silicide block mask at the isolation edge.
- Silicide block mask of the n^+ diffusion except under the contacts.
- Full silicide block mask of the full n^+ diffusion.

In the first case, the blocking of the edge reduces the sensitivity of the LOCOS- or STI-isolation issues. In the second case, the vertical penetration risk of refractory metals into the metallurgical junction is reduced, yet contact resistance is maintained. In the third case, no salicide is formed on the structure. The disadvantage of the last case is an undesirable higher contact resistance.

4.7 ESD DIODE DESIGN: DIODE STRING

Where voltage differential needs to exceed a diode voltage, series diodes are the basic building blocks of ESD design for ESD input node devices, ESD rail-to-rail devices, ESD power clamps, ESD trigger elements, and circuit elements. Series diodes or "diode string" configurations introduce some unique device design, circuit, and integration issues [19–21].

The key to ESD series design of diode structures is

- Utilize parallelism of adjacent diode elements in the chip or system design.
- Optimize the successive stages for area to provide minimum loading and the maximum ESD current discharge.
- Reduction or elimination of the vertical parasitic bipolar effects on the turn-on voltage and leakage.
- Eliminate any parasitic interaction between adjacent diode elements.
- Minimize total diode series resistance.
- Minimize the number of diode elements in series to the minimum product application requirement.

On the issue of parallelism, the ability to integrate series diodes of successive stages from adjacent signal pads, groups of adjacent signals, and peripheral "banks" has a significant impact on the design area and the ESD robustness result. A second means of area and ESD optimization is the area optimization within a given signal pad. Optimization of the area of each successive stage allows for some advantage of providing lower capacitance and area reduction as well.

A unique aspect in the ESD series diode configurations is the vertical bipolar parasitic effects and the interactions between adjacent structures. Figure 4.17 shows an example of an ESD diode string circuit. The role of the vertical bipolar transistor influences the turn-on voltage, the "on-resistance" as well as leakage amplification. The diode equation can be simply represented for a diode within the string as

$$I_{Di} = A_i I_{0i}\left(e^{V_f/V_0 - 1}\right)$$

In the on-state, the saturation current can be neglected. From the form above, the forward voltage of the ith stage can be represented as

$$V_i/V_0 = \ln(I_{Di}/A_i I_{0i})$$

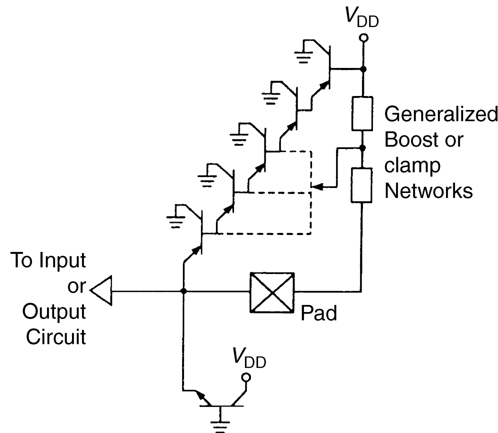

Figure 4.17 ESD diode string design highlighting vertical *pnp* transistor and generalized boost network

In a p^+/n-well "diode" string, in a p^- substrate dual-well technology, a vertical *pnp* transistor exists [19–21]. The collector current can be represented as

$$I_c = \frac{\beta}{\beta + 1} I_{Di}$$

and the base current can be represented as

$$I_b = \frac{1}{\beta + 1} I_{Di}$$

In a series configuration, these form a common-collector configuration. The base of each stage is connected to the emitter of the successive stage. A set of equations exist, which can be represented in the form

$$I_{D(i)} = \frac{I_{D(i+1)}}{\beta_{(i+1)} + 1}$$

Given a set of m diodes, where we define first to equal the current I_D, the successive diodes are a function of the product term [19–21]

$$I_{D(i)} = I_D \prod_{\forall j > i}^{m} \frac{1}{\beta_j + 1}$$

For example, given $m = 5$

$$I_{D5} = I_D$$

$$I_{D4} = I_D\left(\frac{1}{\beta_5 + 1}\right)$$

$$I_{D3} = I_D\left(\frac{1}{\beta_5 + 1}\right)\left(\frac{1}{\beta_4 + 1}\right)$$

$$I_{D2} = I_D\left(\frac{1}{\beta_5 + 1}\right)\left(\frac{1}{\beta_4 + 1}\right)\left(\frac{1}{\beta_3 + 1}\right)$$

$$I_{D2} = I_D\left(\frac{1}{\beta_5 + 1}\right)\left(\frac{1}{\beta_4 + 1}\right)\left(\frac{1}{\beta_3 + 1}\right)$$

$$I_{D1} = I_D\left(\frac{1}{\beta_5 + 1}\right)\left(\frac{1}{\beta_4 + 1}\right)\left(\frac{1}{\beta_3 + 1}\right)\left(\frac{1}{\beta_2 + 1}\right)$$

From the above result, it is clear that the amount of current flowing through each successive stage decreases [19–21]. As the *pnp* bipolar current gain is much less than unity, the current through the successive stages is approximately equal. In the case when the vertical *pnp* bipolar current gain is greater than unity, some percentage of the current flows to the substrate and some current flows along the length of the successive diode stages. In the case when the bipolar current gain is small compared to unity, the majority of the current flows through the successive diode stages. In a diffused well technology, the vertical bipolar current gains typically exceeded unity value (e.g., bipolar current gains exceeded 10) [19–21]. In retrograde well technology, typically the bipolar current gain was well below 10

[19–21]. In many advanced CMOS and BiCMOS technologies, the vertical bipolar current gain approached unity values.

4.7.1 ESD Design: Diode String Current–Voltage Relationship

A key parameter of the series diode configuration is the turn-on voltage, V_T. The diode string turn-on voltage can be represented as the sum of the forward-bias voltages.

$$V_T = \sum_{i=1}^{m} V_i$$

Using the forward voltage expression, we can express this as

$$V_T = \sum_{i=1}^{m} V_0 \ln\left(\frac{I_{Di}}{A_i I_{0i}}\right)$$

Assuming that the diodes are at the same local temperature, the thermal voltage term can be acheived through the summation sign. Replacing the diode current for the ith diode, the above relationship can be expressed as [19,21]

$$V_T = \sum_{i=1}^{m} V_0 \ln\left(\frac{I_D}{A_i I_{0i}} \prod_{\forall j>i}^{j=m} \frac{1}{(\beta_j + 1)}\right)$$

$$V_T = \sum_{i=1}^{m} V_0 \ln\left(\frac{I_D}{A_i I_{0i}} \frac{A_1}{A_1} \prod_{\forall j>i}^{j=m} \frac{1}{(\beta_j + 1)}\right)$$

Assuming the semiconductor process is the same, the saturation current term is equal for all the stages. Separating out a first term, we can represent the term as

$$V_T = \sum_{i=1}^{m} V_0 \ln\left(\frac{I_D}{A_1 I_0}\right) - \sum_{i=1}^{m} V_0 \ln\left(\frac{A_1}{A_i} \prod_{\forall j>i}^{m} \frac{1}{(\beta_j + 1)}\right)$$

Substituting in the forward voltage, V_f

$$V_T = \sum_{i=1}^{m} V_f - \sum_{i=1}^{m} V_0 \ln\left(\frac{A_1}{A_i} \prod_{\forall j>i}^{m} \frac{1}{(\beta_j + 1)}\right)$$

This can be expressed as [19–21]

$$V_T = mV_f - \sum_{i=1}^{m} V_0 \ln\left(\frac{A_1}{A_i} \prod_{\forall j>i}^{m} \frac{1}{(\beta_j + 1)}\right)$$

In this form, it can be observed that the m-diodes in series are equal to the summation of the forward voltage plus an additional term. The turn-on voltage is a function of the number of diodes in series, the forward voltage of each diode, the area parameter, and vertical bipolar current gain. Assuming equal areas of each diode, this can be expressed as [19–21,23–25]

$$V_T = mV_f - V_0 \frac{m(m-1)}{2} \ln(\beta + 1)$$

The significance of this expression is that the turn-on voltage is not the sum of the forward-diode voltages but modified by the second term. In the case that the second term is zero, the operation of the network works as ideal diodes, as if there was no parasitic vertical bipolar element. Hence in the limit that the bipolar current gain approaches zero, the equation approaches an ideal diode representation

$$\lim V_T \,|_{\beta \to 0} = mV_f$$

A second key aspect of the turn-on equation is that each successive diode has less effectiveness. For example, given a diode string of $m + 1$ diodes, the representation can be shown as

$$V_{T(m+1)} = (m+1)V_f - V_0 \frac{(m+1)(m+1-1)}{2} \ln(\beta + 1)$$

The change in the turn-on voltage can then be represented as

$$V_T(m+1) - V_{T(m)} = [(m+1) - m]V_f - V_0 \left[\frac{(m+1)(m)}{2} - \frac{m(m-1)}{2}\right] \ln(\beta + 1)$$

which can be expressed as

$$V_{T(m+1)} - V_{T(m)} = V_f - mV_0 \ln(\beta + 1)$$

As the number of diodes increases, the net forward voltage with the addition of more elements is less effective with each additional element, since the second term decreases the net gain in the turn-on voltage. This decrement is also a function of temperature in the thermal voltage and the bipolar current gain.

A third key aspect of the turn-on equation is that the *pnp* bipolar current gain modulates the turn-on voltage. Different semiconductor processes will have different turn-on characteristics for a common design. Figure 4.18 is a plot of the turn-on voltage as a function of the number of diode stages for two different processes, which have different bipolar current gain. For example, a LOCOS-defined junction with a diffused well will have a *pnp* bipolar current gain on the order of 10 to 30. In a STI-defined diode structure with a retrograde well, the bipolar current gain can be below 10. As the doping concentration of the semiconductor process well increases, the bipolar current gain will decrease.

In the simple case of equal area diodes, we can evaluate the change in the turn-on voltage, assuming a first and second bipolar current gain.

$$V_{T(\beta_1)} = mV_f - V_0 \frac{m(m-1)}{2} \ln(\beta_1 + 1)$$

$$V_{T(\beta_2)} = mV_f - V_0 \frac{m(m-1)}{2} \ln(\beta_2 + 1)$$

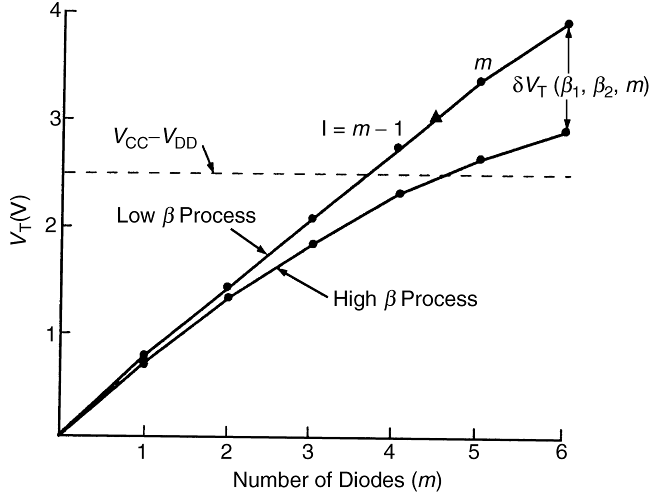

Figure 4.18 Turn-on voltage as a function of stage number for two different semiconductor processes of a first and second bipolar current gain

The turn-on voltage difference can be expressed as

$$\delta V_{\mathrm{T}} = V_{\mathrm{T}(\beta_1)} - V_{\mathrm{T}}(\beta_2) = V_0 \frac{m(m-1)}{2} \ln\left(\frac{\beta_2 + 1}{\beta_1 + 1}\right)$$

In the reverse-biased condition, the turn-on voltage will be a function of the diode and bipolar breakdown voltage conditions. Assuming the base of the last diode stage is at ground potential, and the substrate floats, the voltage drop will occur that can be simplistically assumed as the sum of the reverse breakdown voltage between the p^+ anode to n-well cathode breakdown voltage

$$V_{\mathrm{T_r}} = mBV_{\mathrm{eb}} = mV_{\mathrm{rev}}$$

This is valid when the breakdown voltage remains below the vertical bipolar breakdown voltage of any given stage. At each stage, when the product of the number of stages times the emitter-to-base breakdown voltage exceeds the n-well-to-substrate breakdown voltage or the BV_{CEO} (e.g., open base collector-to-emitter voltage), the breakdown will occur between that stage and the ground potential. Current will flow to the substrate for each successive stage beyond this point.

A second key parameter in the analysis of a series diode string is the effective series resistance. A simple analytical model for the effective series resistance demonstrates its dependence on n-well sheet resistance and the bipolar current gain. An a.c. common-collector model can be defined for the diode string network. Using a hybrid-Π model, the *pnp* transistor can be represented as an emitter resistor, re, a current source, βi_{b}, and base

resistance. The impedance, Z, looking into the first stage is

$$Z = \frac{V_n}{I_n}$$

In the common-collector configuration, the emitter resistor is in series with the base resistor in the series diode ESD network. If the emitter resistor is small compared to the base resistance, this can be neglected. In a p^+/n-well network, the base resistance is a function of the well contact resistance and the n-well sheet resistance. Evaluation of the total impedance

$$Z = \frac{V_n}{I_n} = \frac{1}{I_n} \sum_{i=1}^{i=m} I_{\mathrm{D}i} R_i$$

Solving Kirchoff's current law at each successive node in the circuit, the current through each successive stage is lower than the prior stage by the current gain factor.

$$I_{\mathrm{D}(i)} = I_{\mathrm{D}} \prod_{\forall j > i}^{m} \frac{1}{\beta_j + 1}$$

The effective impedance (e.g., resistance) can be represented as [19–21,23–25]

$$Z_{\mathrm{eff}} = \sum_{i=1}^{i=m} \frac{R_i}{\prod_{\forall j > i}^{m} (\beta_j + 1)}$$

If the n-well resistance is much larger than the emitter, contact, and interconnect resistances, we can assume that the majority of the stage resistance is related to the n-well sheet resistance

$$R_i = \rho_i \frac{L_i}{W_i}$$

From this, we can express the effective impedance of the ESD network as [19–21]

$$Z_{\mathrm{eff}} = \sum_{i=1}^{i=m} \frac{\rho_i L_i}{W_i \prod_{\forall j > i}^{m} (\beta_j + 1)}$$

Given that each successive stage is equal in design length and width, the expression can be represented as an effective sheet resistance

$$\rho_{\mathrm{eff}} = \sum_{i=1}^{i=m} \frac{\rho_i}{\prod_{\forall j > i}^{m} (\beta_j + 1)}$$

This formulation which highlights the effective resistance of the ESD diode string structure is a function of both the *n*-well sheet resistance and the parasitic bipolar current gain [19–21]. The ESD device effectiveness decreases with increasing *n*-well sheet resistance for processes with low bipolar current gain. Assuming the limit that the bipolar current gain approaches zero, the effective resistance approaches the sum of the diode resistances. In the case of high *n*-well sheet resistances, the bipolar current gain will also increase. As a result, the lower current gain term lowers the effective resistance term leading to an improved ESD diode string structure effectiveness.

To show the effect of the bipolar current gain on the sheet resistance, we need to establish a relationship. Assuming a relationship between the vertical bipolar current gain where the bipolar current gain is proportional to a power of the well sheet resistance, expressed as [21,22]

$$\beta = \gamma \rho_0^n$$

where we assume n is a positive number. From this expression, the impedance can be expressed according to the following relationship [21,22]

$$Z_{\text{eff}} = \sum_{i=1}^{i=m} \frac{\rho_i L_i}{W_i \prod_{\forall j>i}^{m} (\gamma \rho_j^n + 1)}$$

Figure 4.19 shows the effective resistance as a function of well sheet resistance. When the *pnp* bipolar current gain is negligible, the effective resistance is linearly proportional to the *n*-well sheet resistance and the slope is proportional to the number of stages (as well as the width-to-length ratio). As the bipolar current gain increases, the effective resistance separates from the ideal resistance asymptotes and converges to a single-stage asymptote. As the effective resistance curves separate from the ideal asymptotes, the circuit is transitioning from being a diode-dominant to a bipolar-dominant operation.

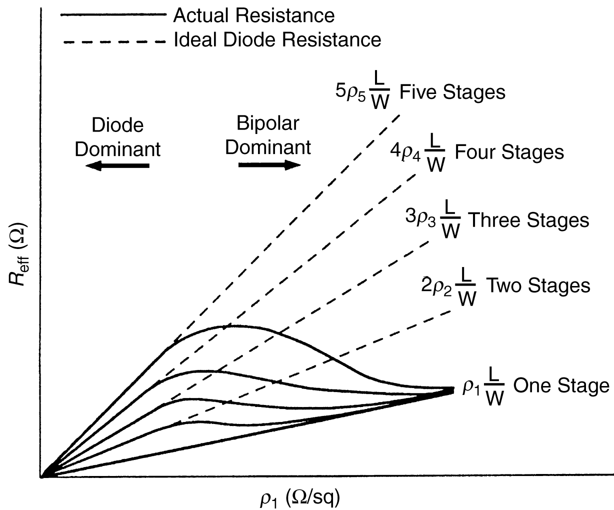

Figure 4.19 Effective resistance as a function of *n*-well sheet resistance and the number of diode stages

4.7.2 ESD Design: Diode String Design—Architecture and the Design

4.7.3 Diode String Elements in Multiple I/O Environments

Signal pin spatial and electrical placement is a function of the chip design and architecture. The placement of the signal pin, power pins, and power rails is a function of the floor planning of the chip design. Diode string ESD design can take advantage of these elements to provide improved ESD design. Diode string ESD design can introduce parallelism to improve the individual pin results. This can be achieved by the following:

- Introduction of sharing of successive diode stages between adjacent signal pads.
- Introduction of metal strapping between local diodes.
- Introduction of metal rails between diode stages to connect adjacent signal pads.
- Introduction of voltage power pins.

Sharing of the diode strings can lead to an improved ESD protection and area reduction. Sharing of the diode strings cannot be done at the first diode element, but can be initiated after the first stage of a diode string design. In this fashion, the second stage and all future stages can be integrated. One means of integration is the second stage of adjacent element which is the same silicon diode element. A second means of integration is that they are independent diode elements which are then electrically connected to a common element. A third mean is instead of a local connection, a metal rail or bus is established across a grouping or bank of elements. A fourth means is to provide a separate power pin and electrically connected all signal pins globally to this physical pin. In this case, all successive elements become a series between the global new power pin and the nominal power rail.

As shown in the diode string development, the effective impedance (e.g., resistance) for each independent signal pin can be represented as [19–21]

$$Z_{\text{eff}} = \sum_{i=1}^{i=m} \frac{R_i}{\prod_{\forall j>i}^{m} (\beta_j + 1)}$$

If the n-well resistance is much larger than the emitter, contact, and interconnect resistances, we can again assume the majority of the stage resistance is related to the n-well sheet resistance

$$R_i = \rho i \frac{L_i}{W_i}$$

From this, we can express the effective impedance of the ESD network as [19–21]

$$Z_{\text{eff}} = \sum_{i=1}^{i=m} \frac{\rho_i L_i}{W_i \prod_{\forall j>i}^{m} (\beta_j + 1)}$$

In the grouping of the signal pins, the first stage must be independent (e.g., the pins will be shorted together if we do not assume this case). Then in general, we can write

$$Z_{\text{eff}} \cong \frac{\rho_1 L_1}{W_1} + \sum_{i=2}^{i=m} \frac{\rho_i L_i}{W_i \prod_{\forall j>i}^{m} (\beta_j + 1)}$$

For all stages after the first stage, the total width of the "*i*th" stage, can be a function of the number of parallel elements.

$$W_i = \sum_{k=1}^{k=n} W_{ik}$$

This assumes a dummy variable *k*, which runs from a single I/O element to *n*-parallel elements which are electrically connected. In the case that one diode is utilized for successive stages, the term reduces to a single width.

For the *i*th element, the summation of the parallel elements will determine the total width. Given the same design style, we can assume the sheet resistance and the "length" are the same. The total effectiveness of utilization of the total width is a function of the ability to distribute or redistribute the current through the given stage or stage-to-stage. This is a strong function of the placement, spacing, and metal design patterns from signal pad to signal pad.

4.7.4 Integration of Signal Pads

Figure 4.20 shows a set of diode string ESD designs. Each diode string is connected to an independent pad. In this case, the ESD designs are independent of adjacent elements. In this fashion, the effective resistance of each stage is higher.

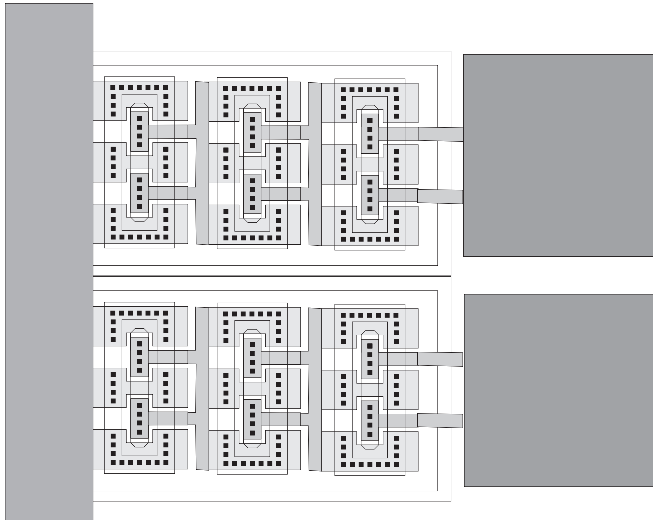

Figure 4.20 Floor plan of adjacent I/O ESD designs

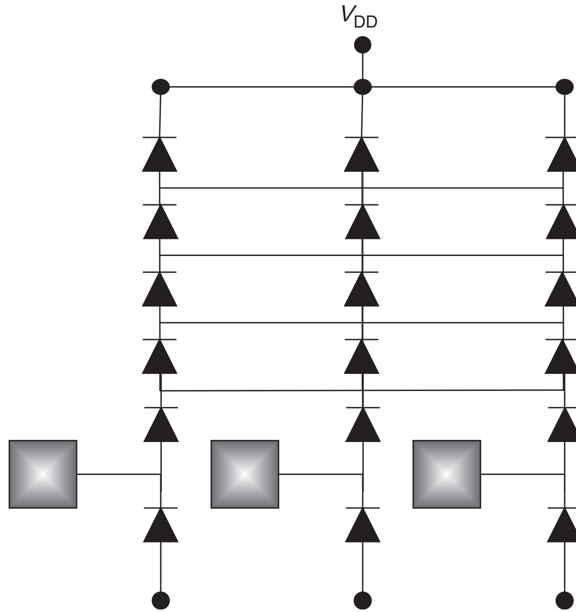

Figure 4.21 Introduction of metal strapping between successive stages

This design can be modified with improved results by integration of all the successive stages after the first element. Figure 4.21 is an example of the introduction of sharing of successive stages using metal connections. In this means, the signal book floorplan remains equivalent. As an example of the effectiveness, two designs were completed. The first design contained five-diode strings in a series configuration with no interconnection between adjacent signal pads. The worst-case ESD robustness of the 0.50-μm technology microprocessor was 3000 V HBM levels. In the redesign of the chip, in the next technology generation, the ESD area was reduced by 50% due to the need to integrate a cascode *p*-channel OCD element. By introducing of the sharing of the diode elements using metal straps across adjacent cells, with 50% of the ESD area, the improvement increased from 3 to 10 kV HBM ESD levels. From this result, it is clear that the reduction of the series resistance in the successive stages significantly reduced the effective impedance in the implementation.

In a second design practice, the successive diode string stages can be integrated in silicon as a common element across adjacent signal pads. Figure 4.22 is an example where the second stage and all successive stages are connected to a common silicon region.

In a second example implementation, four signal pads were placed in a ‘‘nibble architecture.’’ In that implementation, because of the narrowness of the pad pitch, the first stage diodes were placed perpendicular to the pad layout. The second and successive stages were rotated 90° to the first stage, and straddled the four signal pads. In this fashion, the successive stages were four times the pitch of the individual signal pads and integrated across all four signal pads. In order to have the current flow from the first stage to successive stages, metal was introduced to redistribute the current into the second and successive stages. The worst-case ESD results achieved over 6000 V HBM levels in a very small

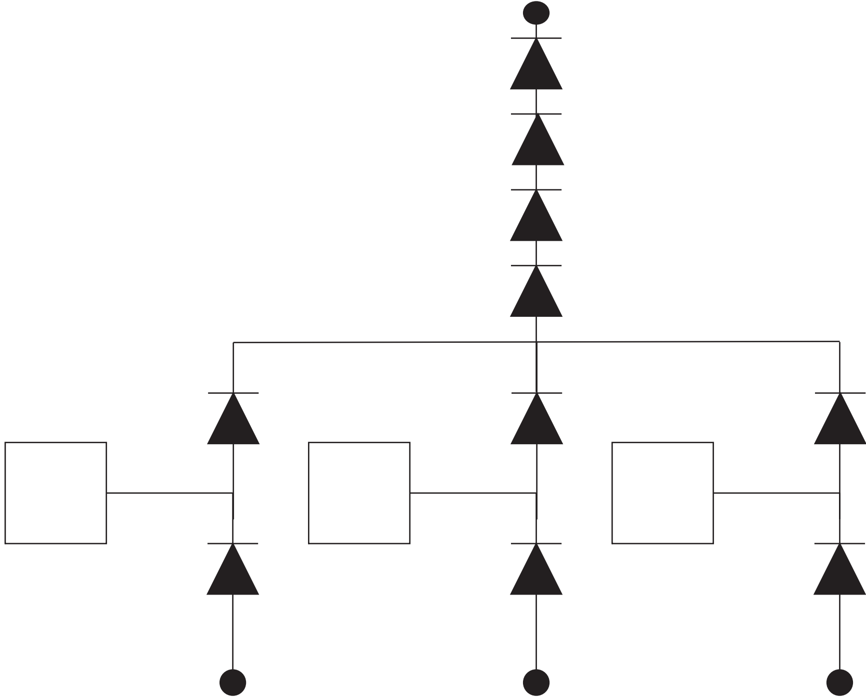

Figure 4.22 Introduction of a common diode region for successive stages

physical area. The interesting result was the area utilized was equal to a single non-mixed voltage application in the 0.35-μm MOSFET channel length technology that achieved only 3000 V.

Additionally, the design modification can be established where new bus rails can be placed to redistribute the current across the larger elements (Figure 4.23). This bus can be local to the connected signals, or continue to all signal pads. In the case where it is connected to a group or all signal pads, this can be connected to a larger dummy ESD bus, or a dummy signal pin.

From this integration design strategy, it should be clear to the reader that the successive stages do not have to be local to the signal pins. For an n-stage ESD diode design, the successive stages from $i = 2$ to $i = n$, can be spatially separated from the signal pin and placed in a separate region of the design. These can be placed near the chip corners, power pads, service functions, or other design locations. The effectiveness will be a function of the bussing resistance, current distribution, and redistribution between the successive elements. As these elements are integrated from signal to signal, the area dedicated to a signal pad begins to migrate from a local pin ESD protection to serving and assisting the global chip ESD protection.

4.7.5 ESD Design: Diode String Design—Darlington Amplification

Leakage, photo-emission, and noise can be a concern in ESD diode elements [21,22,23–25]. In the ESD diode string configuration, the collectors of the successive stages are in a

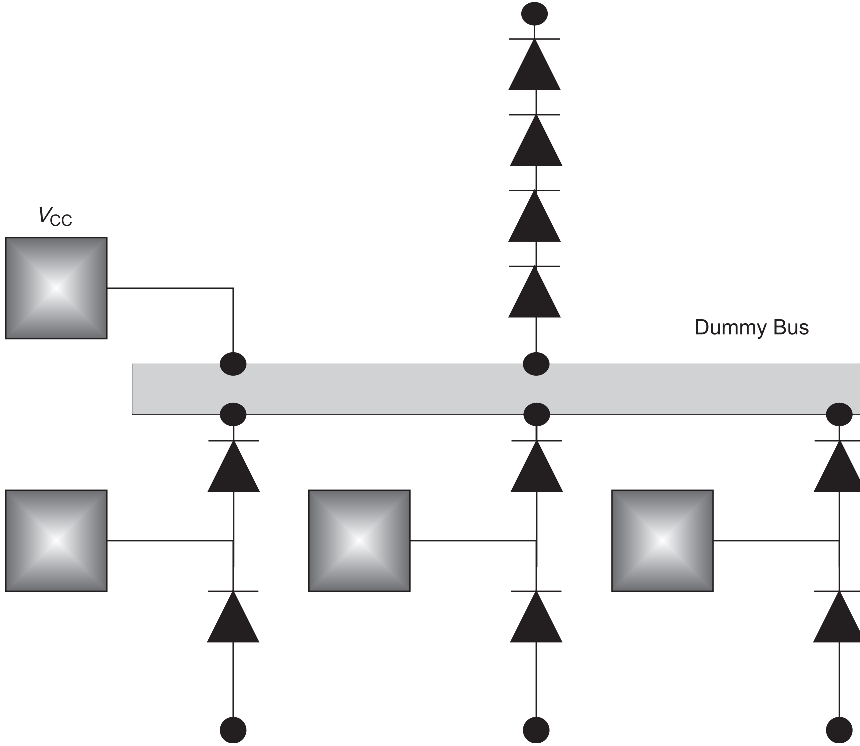

Figure 4.23 Introduction of dummy ESD bus rails into the diode string design

common-collector configuration. The *n*-well region cathode is contained within the chip substrate region. This *n*-well region contains a metallurgical junction between the substrate and the base region. Minority carrier injection, photo-generation, or signals that are transmitted at the *n*-well to substrate junction can be propagated through the diode string configuration. Because of the diode string electrical connections, the collector of the successive stage is the base region of the prior stage. All signals on the collector region is then amplified in the prior stage. The diode equation can be simply represented for a diode within the string as

$$I_{Di} = A_i I_{0i}\left(e^{V_f/V_{0-1}}\right)$$

In the on-state, the saturation current can be neglected. In the case that the diode is not in forward active mode, the diode current is

$$I_{Di} = -A_i I_{0i}$$

In the diode string configuration, the *pnp* bipolar base current is amplified by each successive stage (from the end of the diode string back to the first stage) when each stage is in a forward active mode of operation. Each stage amplifies the base current by the reverse

pnp bipolar current gain, β_r

$$I_{Di} \approx (\beta_r + 1) I_{D(i+1)}$$

For five diodes in series, assuming the leakage is coming from the last diode only

$$I_{D4} \approx (\beta_{r4} + 1) I_{D5}$$
$$I_{D3} \approx (\beta_{r3} + 1)(\beta_{r4} + 1) I_{D5}$$
$$I_{D2} \approx (\beta_{r2} + 1)(\beta_{r3} + 1)(\beta_{r4} + 1) I_{D5}$$
$$I_{D1} \approx (\beta_{r1} + 1)(\beta_{r2} + 1)(\beta_{r3} + 1)(\beta_{r4} + 1) I_{D5}$$

In this fashion, the injection at every collector region is then propagated to the first stage. Leakage or minority carrier generation is then current amplified through each successive stages. This can be represented as a summation expression. As a result, the total reverse current is a function can be assumed to be equal to

$$I_D \approx I_r \prod_{i=1}^{i=m} (\beta_{ri} + 1)$$

From this expression, the leakage amplification can be estimated as the product of the bipolar current gain of the successive stages (or simplified as beta to the power of the number of stages) and the reverse current seen on the last stage

$$I \approx (\beta + 1)^m I_{rev}$$

The amplification is a function of the

- Area of the collector-to-substrate junction of each diode stage.
- Area of the p^+ anode region.
- Reverse bipolar current gain.
- Diode (base) series resistance.
- Magnitude of the forward bias state.

In the case of a Darlington amplifier, it is well known that if each successive stage increases in the physical size, the total current increases. As the diode elements get larger toward the input node, the amplification current will increase. Hence, to eliminate the amplification effect of a diode string element, there are some basic design and process choices

- Reduce the vertical *pnp* bipolar current gain using heavily doped retrograde well implants, sub-collectors, or buried layers.

- Maintain the area of the successive stages as equal, or increase the size of the diode area from the input to the power supply.
- Reduce the total number of diode stages.
- Prevent forward biasing across as many stages as possible in the given application.

In an m-stage ESD diode string design, the Darlington amplification of the leakage current follows the relationship [19–21,23–25]

$$\beta_{\text{peak}} = (\beta_{\max} + 1)^m - 1$$

The first means is to lower the bipolar current gain of each successive stage. One method to reduce the vertical bipolar current gain is to apply this circuit in a technology that can introduce features that lower the parasitic bipolar current gain characteristic. In early CMOS processes, n-well structures were formed using diffusion processes. In these processes, the vertical bipolar gain ranged from 10 to 30. In that case, the amplification of the leakage was increased as 10^m, where m is the number of stages. In these technologies, the power supply voltages ranged from 3.3 to 5 V V_{DD} levels in CMOS applications, and 12 V for non-volatile RAMs (NVRAMs). In these cases, the number of series diodes ranged from 5 to 10 diodes. In these cases, without an alternative solution, the circuits had significant leakage current. Additionally, in the case of flash NVRAM applications, the photon current would be amplified through the ESD network leading to noise spikes during flash operation.

Using retrograde well technology and sub-collector implants, the vertical bipolar current gain can be reduced, eliminating the magnitude of the reverse amplification. For example, in heavily doped retrograde wells, the bipolar current gain can be reduced to $\beta = 2$. In this case, the leakage is amplified by a factor of 64. Hence as the bipolar current gain is reduced toward unity, the reverse amplification is not a significant issue.

Second to lower the amplification is to reduce the number of successive stages. As technology scales to lower power supply voltages, the number of diode elements in series will be reduced.

An alternative strategy is to break the Darlington amplification effect by using circuit techniques instead of area optimization. Three circuit concepts exist:

- Clamping elements across a number of stages to prevent forward bias condition for reverse amplification.
- Boosting elements to prevent forward bias condition for reverse amplification.
- Establish an alternative current path.

The clamping or boost elements concept can be achieved using passive or active elements [19–21,23–25]. Resistors, diodes, or MOSFETs can be used to prevent the initiation of the reverse amplification effect.

Figure 4.17 shows a generalized boosting and clamping network for an ESD diode string for elimination of Darlington amplification. The method of using a simple diode element was first proposed by Kirsch [19]. The operation as an ESD diode string was demonstrated

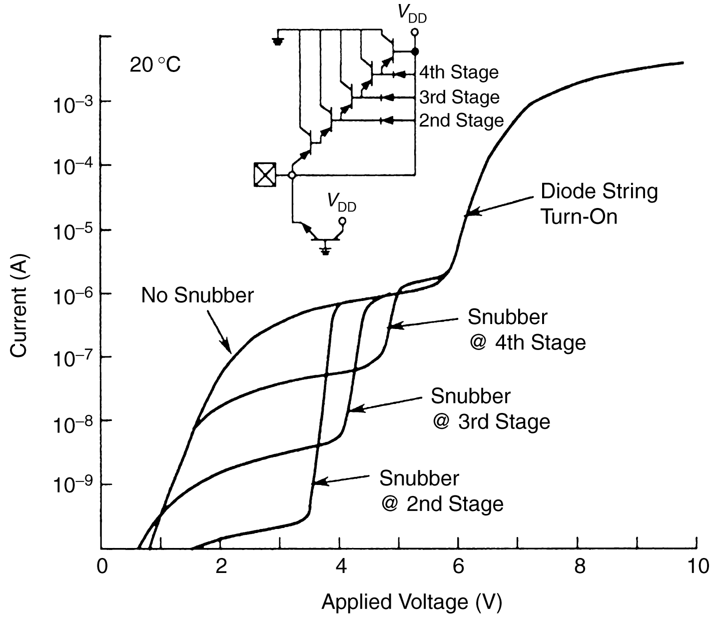

Figure 4.24 Circuit simulation of the input pad current versus applied voltage as a function of Snubber diode stage connections

in conjunction with G. Gerosa [19–21]. The diode (or vertical *pnp* bipolar element) was placed between the last stage of the ESD power clamp and a prior stage. The simplest solution was a diode element which was coined as an "ESD snubber diode" element. To break the Darlington effect of the reverse amplification, an additional ESD snubber diode was placed in the base of a bipolar stage. In essence, the "snubber diode" is a bipolar transistor between V_{DD} and ground (V_{SS}) potential whose base is connected to one of the diode stages.

Circuit simulation was used to determine the most effective location of the "ESD snubber diode" element to eliminate the leakage and not impact circuit functionality. Figure 4.24 shows the circuit simulation results with the "ESD snubber diode" at different stages. In the figure, the case of the diode string without a snubber element is shown in a LOCOS/diffused well technology. In the figure, a large "hump" is evident below the turn-on voltage of the diode string element. The first "hump" in the *I–V* characteristic is associated with the Darlington amplification, and the second current increase is associated with the diode string turn-on voltage. The optimum clamping action was obtained by placing the snubber diode on the second stage. The snubber diode boosts the second stage voltage to $V_{DD} - V_{be}$ (e.g., one forward bias voltage drop from the power supply). When the voltage is boosted toward the power supply voltage, it clamps the forward voltage across the individual stages, which limits the leakage current amplification.

As the snubber element is placed toward the signal pad, the voltage at which the clamping occurs shifts to lower voltages. The optimum effectiveness was evident when the snubber element was connected to the base of the second stage.

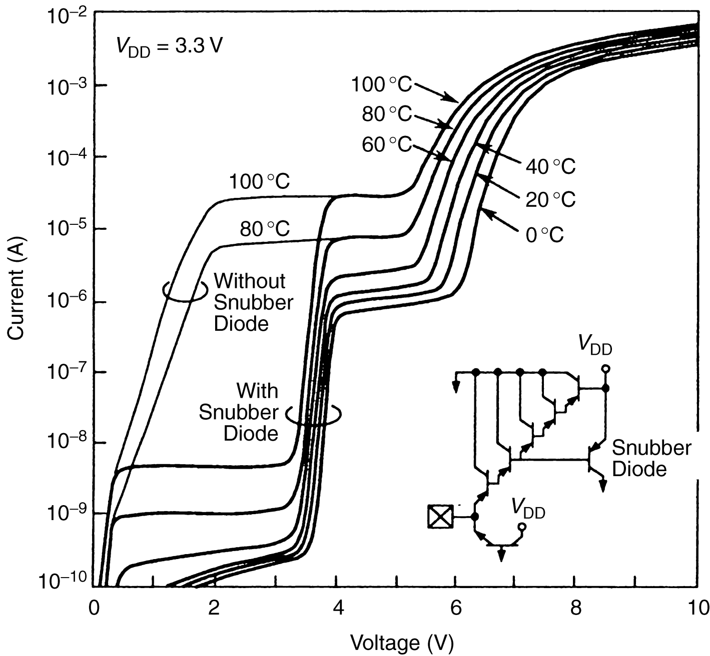

Figure 4.25 Circuit simulation of input pad *I–V* characteristics of ESD structure in a LOCOS technology highlighting Snubber clamp Darlington action clamping as a function of temperature

Figure 4.25 illustrates the circuit simulation of the pad leakage current with and without a snubber diode for the LOCOS/diffused well semiconductor process for different temperatures for the case where the snubber diode is placed on the second stage. The circuit simulation results show that, without the snubber clamp element, the leakage is significantly amplified at elevated temperatures below 3.3 V application voltages. When the snubber clamp element is in place, the leakage is reduced by 4–5 orders of magnitude

Experimental measurements of the snubber diode ESD diode string circuit was demonstrated in a low- and high-bipolar *pnp* current gain process. Figure 4.26 shows the same electrical circuit in two different technologies. In the low bipolar current gain retrograde well technology, there are a few key points of interest:

- The snubber diode lowers the leakage by 1–2 orders of magnitude.
- The turn-on diode string voltage is "ideal."

There are key issues to note in the case of the diffused well case:

- The snubber element provided a 5 order of magnitude reduction of the leakage current at temperature in the high bipolar current gain technology.
- The "hump" is still evident above a given voltage.
- The turn-on voltage is lowered due to the vertical bipolar current gain.

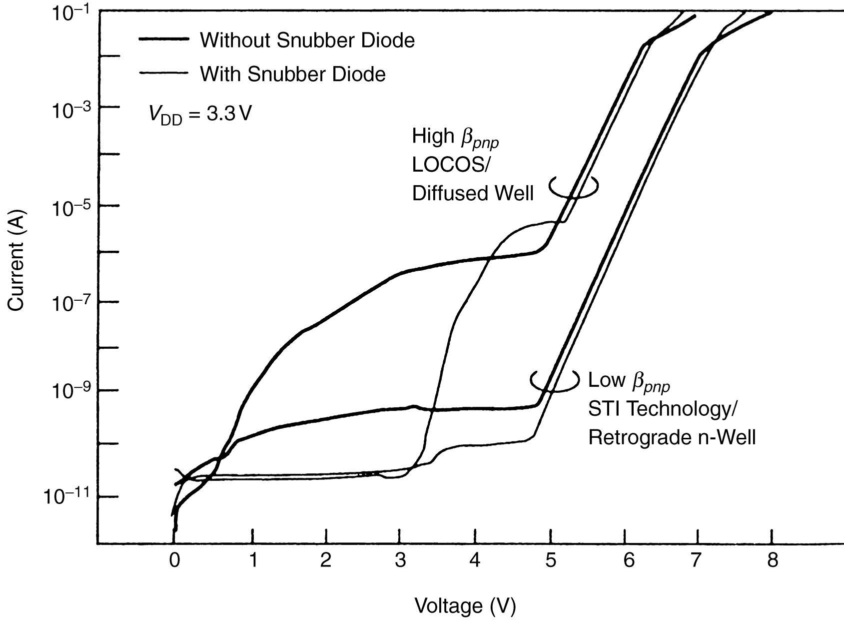

Figure 4.26 Electrical characterization *I–V* characteristics of an ESD diode string with and without a Snubber diode for a low- and high-bipolar current gain technology

In this implementation, for the high bipolar current gain diffused well technology, the Darlington amplification was significantly above a retrograde well technology. This was effectively reduced using the circuit solution. But the third issue is significant. In the two processes, the heavily doped retrograde well process has "ideal diode" turn-on voltage value whereas the diffused well process has a non-ideal condition. From an ESD perspective, the lower turn-on voltage allows for an earlier turn-on of this network. From a functionality perspective, the lower turn-on voltage leads to a higher input leakage current (note: this is not the amplification effect). In the application, the lower voltage increases the input current by two to three decades higher than an "ideal diode string" application. This is a concern for functional applications

4.7.6 ESD Design: Diode String Design—Area Scaling

In the ESD design of diode strings, based on the analysis of a diode string structure, the amount of current flowing through the successive stages is a function of the area of each stage as well as the bipolar current gain. The base of each stage is connected to the emitter of the successive stage. A set of equations exist which can be represented in the form

$$I_{D(i)} = \frac{I_{D(i+1)}}{\beta_{(i+1)^{+1}}}$$

Given a set of m diodes, where we define the first to equal the current I_{D}, the successive diodes are a function of the product term

$$I_{\mathrm{D}(i)} = I_{\mathrm{D}} \prod_{\forall j > i}^{m} \frac{1}{\beta_j + 1}$$

From this relationship, let us assume that the

$$I_{\mathrm{D}i} = A_i I_{0i} \left(e^{V_{\mathrm{f}}/V_{0-1}} \right)$$

and

$$I_{\mathrm{D}(i+1)} = A_{(i+1)} I_{0_{(i+1)}} \left(e^{V_{\mathrm{f}}/V_0 - 1} \right)$$

Let us set the relationship so the current through both diode elements in the successive stages are equal. Then

$$A_{(i+1)} I_{0_{(i+1)}} = A_i I_{0i}$$
$$I_{\mathrm{D}(i)} = A_i I_{0i} \left(e^{V_{\mathrm{f}}/V_{0-1}} \right) = \frac{I_{\mathrm{D}(i+1)}}{\beta_{(i+1)^{+1}}} = \frac{A_{(i+1)} I_{0(i+1)}}{\beta_{(i+1)^{+1}}} \left(e^{V_{\mathrm{f}}/V_{0-1}} \right)$$

Assuming the saturation current of the successive stages are equal, we obtain the relationship

$$A_i = \frac{A_{(i+1)}}{\left[\beta_{(i+1)}{}^{+1} \right]}$$

Hence, in order for the current to be constant through the diode string structure, the area scaling of the successive elements are

$$A_{(i+1)} = \left[\beta_{(i+1)} + 1 \right] A_{(i)}$$

In this design strategy, the area of the stages increase with each stage to carry a constant current through a physical size. This has an advantage in that the first stage is the smallest stage. In this case, the capacitance is lowest near the signal pad. Figure 4.27 shows an example of a diode string with successively larger diode stages.

4.8 ESD DIODE DESIGN: TRIPLE-WELL DIODES

Triple-well technology allows for the isolation of both p-channel and n-channel elements. To form an isolated p-region separate from the p-substrate region, a dopant layer of opposite type is introduced. An n-type dopant layer is placed under the p-well region to isolate the epitaxial region. On the edges of the structure, insulators or metallurgical junction are formed to isolate the physical region. On the edges, shallow trench isolation (STI),

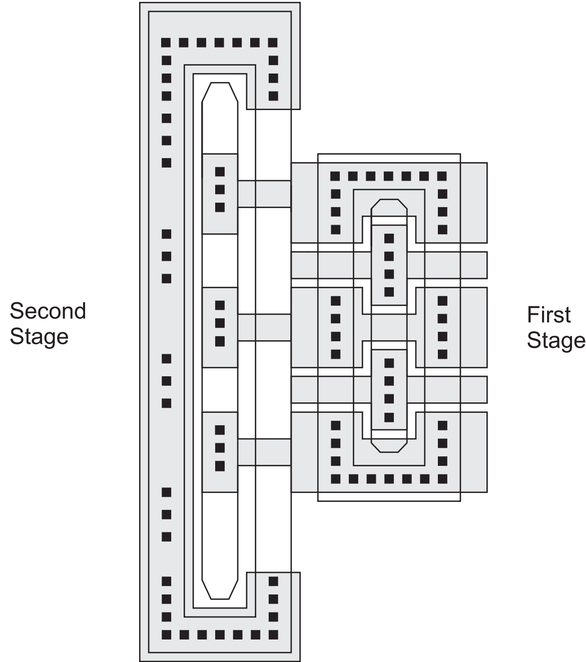

Figure 4.27 Diode string design with successively larger area diode stages

trench isolation (TI), or deep trench (DT) isolation can be used to intersect the epitaxial region to fully isolate the region [32].

With the introduction of the triple-well structure, the ESD diode elements are modified. The structural distinctions are the following:

- A vertical *npn* bipolar is present between the n^+ diffusion diode, p^- isolated epitaxial region, and the *n*-type buried layer.
- A vertical *pnp* element of a p^+ diffusion in a p^- isolated epitaxial region, the *n*-buried layer, and the p^- substrate.
- An *n*-well diode will be modified by the *n*-type buried layer, or cannot be used (e.g., abutting of the layers).
- An *n*-*p* diode can be formed between an *n*-diffusion within the isolated p^- region, and the p^+ substrate contact to the p^- region.

As a result, the operation of the physical elements will differ in that new parasitic elements are introduced. Utilization of these elements will be a function of the doping concentrations, physical depths, spacings, and electrical connections. The electrical connection of the *n*-buried layer (e.g., power supply choice, circuit connection, or floating state) will influence which ESD mode of operation this element will be active in. In triple-well technology, triple-well input node ESD networks can be constructed between the signal

input node and the power supply voltage V_{DD}, as well as elements between the signal pad and the chip substrate or V_{SS} power rail.

In single- and dual-well CMOS series diode ESD power clamps, the p^+/n-well elements, the parasitic bipolar element exists between the p^+ diffusion, the *n*-well, and the substrate region. The successive diode stages are in a *pnp* common-collector configuration. For negative polarity ESD events, *n*-well-to-substrate diodes and *n*-diffusion-to-substrate diodes are used between the signal pad and the electrical ground.

Triple-well CMOS and BiCMOS technologies allow for a buried *n*-type layer to be placed in a fashion to isolate the *p*-epitaxial region or *p*-well region. The separation of the epitaxial layer from the substrate allows for design symmetry between the signal pad and the power supply rails (e.g., V_{DD} and V_{SS}).

A triple-well ESD input network can be formed using a p^+ anode in a *p*-well, with an underlying buried layer implant. Isolated epitaxial regions can be formed using an implant layer or sub-collector implants from bipolar transistor elements. The ‘‘edge’’ structure, to isolate the epitaxial region, can be a diffused region (e.g., *n*-well) or a trench isolation structure. In BiCMOS and BiCMOS Silicon Germanium technology, the sub-collector implant can be placed under a *p*-well region to isolate the epitaxial region. In triple-well CMOS technology, or a BiCMOS technology, the diode structure can be placed in a *p*-well region which is isolated by a lower *n*-type structure and a sidewall edge structure. Forming a triple-well diode structure, the STI-defined p^+ diffusion can be placed in a *p*-well region. The STI-defined cathode is contained within the *p*-well. The triple-well isolating region can be used in two fashions:

- Electrically connected to the successive ESD power clamp stages serving as a second *p–n* junction for improved discharge capability.
- Electrically ‘‘floating’’ in the *p*-substrate region.
- Electrically biased to a separate bias potential.

In the first case, the *n*-band isolation region can be electrically connected and serve as a second cathode structure for the ESD power clamp, as proposed by Sloan, Pequignot, Stout and Voldman [47] (Figure 4.28). In this fashion, the separate band region increases the total diode area forming two parallel metallurgical junctions and two parallel current

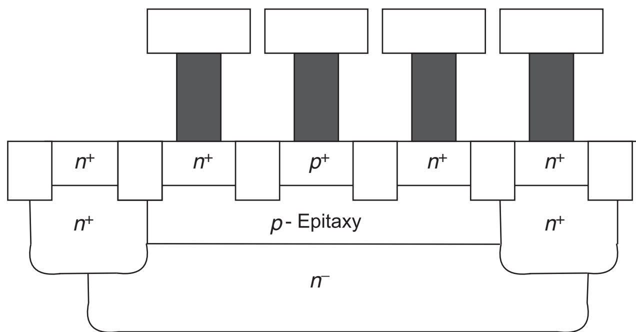

Figure 4.28 Triple-well ESD power clamp with p^+ diffusion in an isolated *p*-well and *n*-band second cathode

paths which converge for each successive stage. An advantage of this implementation is the ability to utilize the deep buried layer region as well as the STI-defined n^+ cathode. But, in this process, the isolation is compromised for improved current discharge capability. Additionally, in this fashion, a parasitic *pnp* is formed between the *p*-well, the *n*-band region, and the *p*-substrate. Although there is a vertical parasitic *npn* transistor formed between the *n*-band, the *p*-well region, and the STI-defined *n*-cathode element, because they are electrically connected, this eliminates any parasitic *npn* interaction. An additional ESD design layout disadvantage is that each successive stage cannot merge the triple-well region together (e.g., note that the spacing between the adjacent wells and buried layers can be significant).

For the single element for negative discharge, a diode can be formed in two fashions. First, the STI-defined n^+ diffusion can be electrically connected to the input node. The p^+ contact within the *p*-well region can be connected to a V_{SS} ground power rail. This forms a diode between the input signal node and the electrical rail that is connected to the isolated epitaxial region. Additionally, the *n*-buried wire can be connected to the same power rail or a second power rail. Electrically connecting the *n*-band isolation region to V_{DD}, the parasitic *npn* formed between the n^+ diffusion, the p^- isolated epitaxial region, and the *n*-band can be utilized for negative polarity input node ESD events.

For positive polarity ESD events, the *n*-band region can remain floating in the substrate region, as proposed by Sloan, Pequignot, Stout and Voldman [47]. A parasitic *pnp* is formed between the *p*-well, the *n*-band region, and the *p*-substrate. Additionally, there is a vertical parasitic *npn* transistor formed between the *n*-band, the *p*-well region, and the STI-defined *n*-cathode element.

In a BiCMOS technology, S. S. Chen *et al.* [48] used a sub-collector region and a deep trench (DT) sidewall to isolate the *p*-well region from the substrate to form a triple-well ESD diode string element. Using the sub-collector region and the DT sidewall isolation, the leakage current is reduced (e.g., compared to the singe- and dual-well series diode CMOS ESD power clamps) (Figure 4.29). S. S. Chen showed that the Darlington leakage

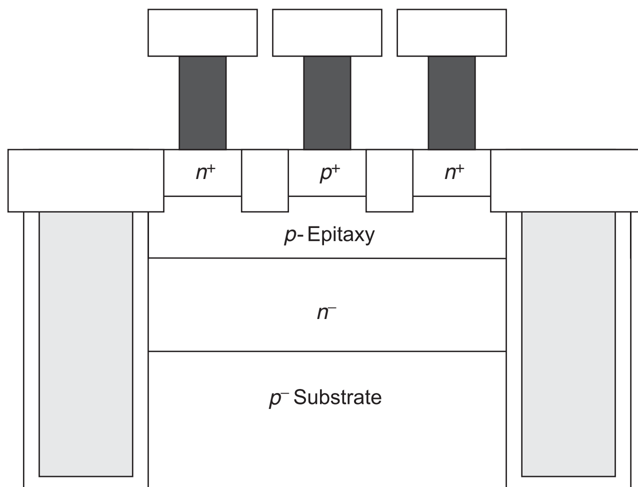

Figure 4.29 Triple-well ESD device with p^+ diffusion in an isolated *p*-well, floating *n*-sub-collector, and deep trench (DT) isolation

amplification effect can be significantly reduced [48]. A first advantage of this triple-well ESD signal network is the elimination of the leakage amplification. A second advantage is the lack of parasitic interaction of adjacent elements due to the isolating sub-collector and DT structure. A third advantage is the ESD design layout density advantages. With the DT structure, the density between the successive stages are limited to DT spacings. Additionally, the usage of DT limits the out-diffusion of the sub-collector, providing a denser triple-well ESD power clamp design. A disadvantage of the DT-bound ESD power clamp is the use of a DT structure that increases the substrate thermal impedance. Hence, the power-to-failure will be impacted by the self-heating in the surface region. This can be reduced by using multiple-finger STI-defined p^+ elements to widen the trench opening, reducing the impact of the trench structure.

Using a bias network, a new triple-well ESD power clamp can be formed. The bias network can electrically connect to the *n*-type isolating structure but is electrically disconnected from the diode string current path through the diode elements. Using a separate voltage biasing network, the triple-well isolation region can be connected to a separate voltage condition. W. L. Wu and M. D. Ker showed that using a bias network, a higher blocking voltage and lower leakage current can be achieved (e.g., compared to the case of a ‘‘floating’’ *n*-band triple-well structure) [49]. W. L. Wu and Ker also showed that a lower turn-on voltage is present when the *n*-band network is not electrically biased in the triple-well ESD power clamp structure. An advantage of this *n*-band-biased triple-well ESD power clamp is the reduction of the excess substrate current (compared to the floating *n*-band ESD power clamp). A second advantage is that by separating the isolation region from the series diode elements, the successive diode stages can be physically merged, reducing design area. The design area between successive stages of the diode elements is limited to the width of the edge isolation region (e.g., *n*-well width) (Figure 4.30).

In many applications, it is not desirable to have a power supply connected to the *n*-band network directly. It was also shown by W. L. Wu and M. D. Ker that it was not desirable to

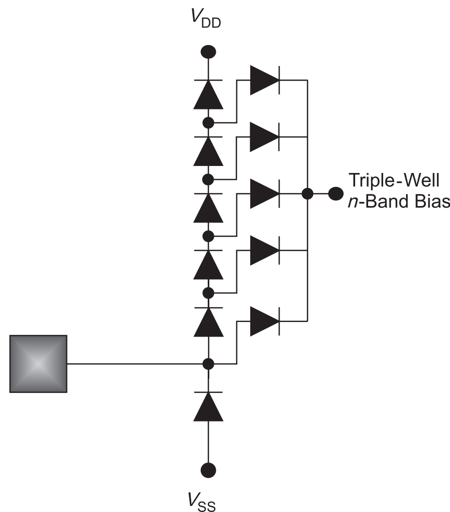

Figure 4.30 Triple-well ESD power clamp network with independent *n*-band voltage dc bias

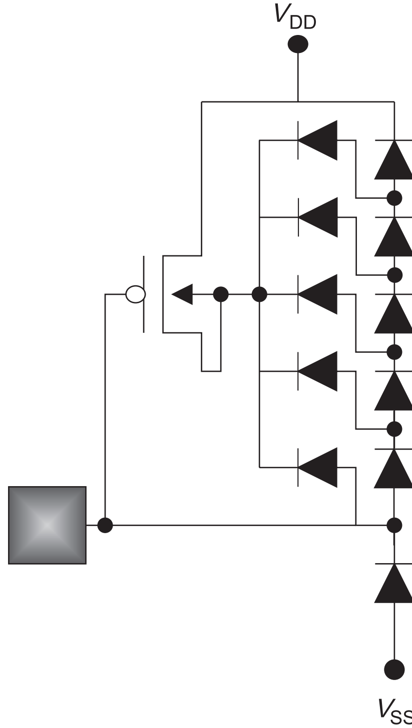

Figure 4.31 Triple-well ESD network with *n*-band bias control network

have the *n*-band region to float during circuit operation due to functional excess substrate current [49]. Hence, a solution proposed by Voldman, Sloan, Pequignot and Stout is a triple-well diode string where the first stage is electrically connected to a *n*-band bias network [48]. Using a *p*-channel MOSFET element, whose source is connected to V_{DD}, whose drain is connected to its own *p*-channel MOSFET body, and whose gate is electrically connected to the input pad. The drain of the *p*-channel device is electrically connected to the *n*-band structure. When the input signal is below the power supply voltage, V_{DD}, the *p*-channel MOSFET is in an "on" state, allowing biasing of the *n*-band structure. In this fashion, the *n*-band structure is biased at the V_{DD} potential. When the input signal rises above the power supply, the *n*-band region floats. In this fashion, the *n*-band is suitable that is biased during functional operation (Figure 4.31).

4.9 ESD DESIGN: BICMOS ESD DESIGN

Mixing CMOS and bipolar structural elements, traditional STI-bound p^+/n-well diode structures and *n*-well-to-substrate diode structures can be modified by utilizing the sub-collector implants, DT, and TI structures [31]. Trench structures can provide reduced capacitance and physical isolation for RF performance, density, and latchup isolation. Utilizing the sub-collector and reach-through implant in an *n*-well structure can provide a low-resistance cathode for a diode structure and prevent substrate hole injection. The

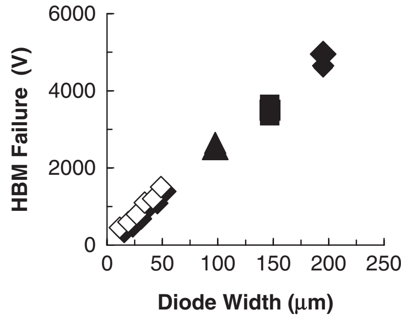

Figure 4.32 HBM failure voltage as a function of diode width for an STI-bound diode in an *n*-well with low-dose implanted sub-collector

enhanced recombination in the cathode of the diode structure also reduces the vertical *pnp* current gain. The physical design of these elements can be identical in nature to the CMOS STI-defined diode structures; in these cases, the sub-collector mask is placed under the *n*-well, the DT and TI structures which border the *n*-well. In this fashion, the implementation is transparent to the p^+ anode, n^+ cathode, and metal design.

4.9.1 p^+/*n*-Well Diode ESD Structure with High Resistance Implanted Sub-Collector

Implanted sub-collectors provide an opportunity to scale the vertical profile of a BiCMOS SiGe HBT as well as lower manufacturing cost. In a technology with an implanted sub-collector, the doping concentration is significantly lower than the pre-epitaxial sub-collector used in BiCMOS SiGe HBT devices. For the implanted sub-collector, the sheet resistance is on the order of 100 Ω /sq. as opposed to the heavily doped sub-collector (e.g., approximately 10 Ω /sq.) [29–31].

HBM and TLP failure value of a STI-bound p^+/n-well diode structure with a low-dose implanted sub-collector (Figures 4.32 and 4.33). The TLP measurements are for single- and

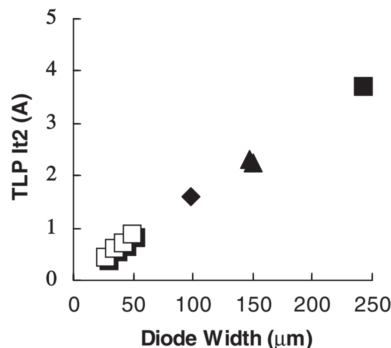

Figure 4.33 TLP critical current as a function of diode width for STI-bound p^+/n-well diodes with implanted sub-collector

multi-finger structures. Single-finger structures were measured between 0 and 50 μm diode width. Multi-finger diode structures with a 0.72×50-μm width for each finger were measured. HBM and TLP measurements do not show string roll-off effects [30,31]

The following table summarizes the HBM, MM, and TLP results of a p^+/n-well diode structure with high-resistance sub-collector implant:

Diode length(μm)	Finger number (#)	HBM (V)	TLP (A)	MM (V)
11.5	1	450		90
19.2	1	600		90
26.6	1	800	0.43	90
34.1	1	1100	0.60	120
41.5	1	1200	0.70	120
48.76	1	1500	0.90	120
97.6	2	2650	1.60	150
146.8	3	3650	2.30	180
195	4	4950		210
243	5		3.70	240

4.9.2 STI-Bound p^+/*n*-Well Diode with Deep Trench (DT) Isolation Structure

Figure 4.34 shows the novel DT-defined collector STI-bound p^+/well diode structure [31]. The anode consists of an STI-bound p^+ region and a *n*-well/STI-bound n^+ cathode structure. Mixing CMOS and bipolar structural elements, traditional STI-bound p^+/n-well diode

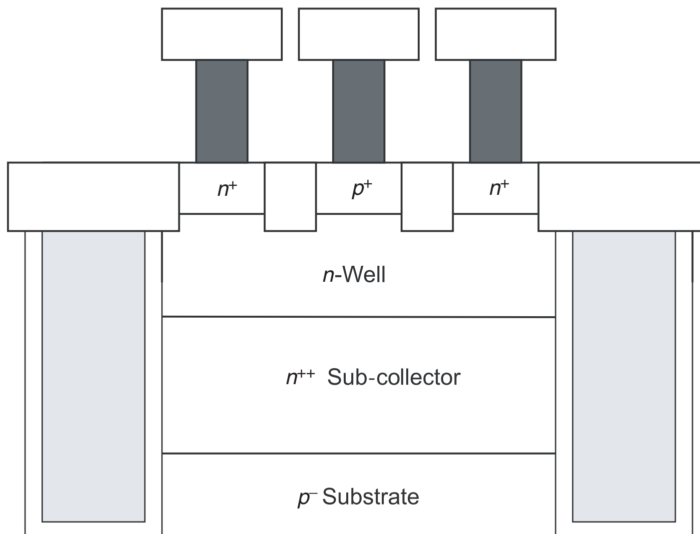

Figure 4.34 Deep trench (DT) isolation and sub-collector defined STI-bound P^+/n-well diode structure

Table 4.2 HBM data of sub-collector-to-substrate diode with and without deep trench (DT) isolation

Sub-collector Substrate diode		
Deep Trench (DT) Structure size (μm)	No DT HBM (V)	DT HBM (V)
2.1	−2600	−1800
4.2	−4100	−2400
8.4	−5500	−3700
16.4	−8400	−5200
33	>−10,000	−8700

structures and *n*-well-to-substrate diode structures can be modified by utilizing the sub-collector implants and DT. DT structures provide reduced capacitance and physical isolation for RF performance, density, and latchup robustness. DT extends below the *n*-well and sub-collector junction eliminating the *n*-well/sub-collector sidewall capacitance. Utilizing the sub-collector and reach-through implant in an *n*-well structure can provide a low-resistance cathode for a diode structure, prevent hole injection, enhanced Auger recombination, and reduced vertical *pnp* current gain.

The presence of the DT structure increases the thermal resistance to the bulk substrate, leading to a higher temperature and earlier failure of the structure due to self-heating. For negative ESD events, a DT-bound *n*-well and a non-DT bound *n*-well show a very significant difference; ESD results show non-DT bound structure, where HBM ESD results are 2× the DT-bound structure (Table 4.2). The advantage of the DT-bound structure is a lower capacitance ESD element, density, and constraint of electron injection into the substrate.

4.9.3 STI-Bound p^+/n-Well Diode With Trench Isolation (TI) Structure

A second type of trench structure is called trench isolation (TI) [31]. This technology utilizes an implanted sub-collector. The implanted sub-collector is significantly shallower than epitaxial-based buried sub-collector. The implanted sub-collector dose and energy are reduced to avoid high capacitance at the base–collector metallurgical junction. With the shallower collector structure, the depth of the adjacent isolation is not as deep as those used in the DT implementations (Figure 4.35). This has an advantage for cost and performance. In this structure, the TI is formed after shallow trench isolation (STI) and all front-end-of-line processing. The isolation structure extends along the sidewall of the collector region

For ESD, latchup, and substrate injection, the TI structure has considerable advantages over non-trench structures. The TI prevents lateral diffusion of the sub-collector toward the *p*-well edge or adjacent n^+ diffusions or sub-collector structures. Hence, lateral parasitic effects are greatly reduced. This lowers the electric field in reverse bias and the isolation breakdown voltages. Second, it prevents lateral current injection minimizing lateral substrate

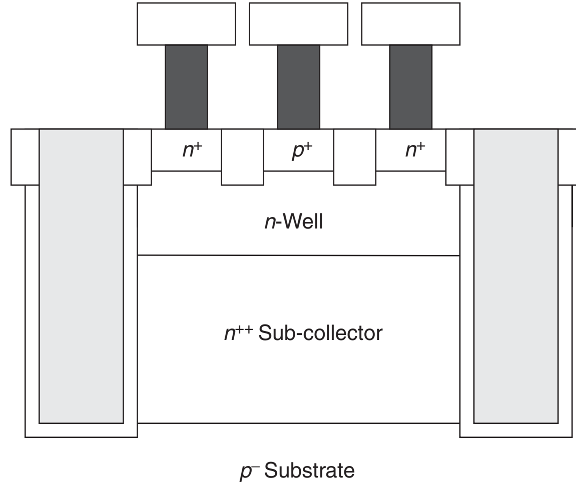

Figure 4.35 TI-bound p^+/n-well diode structure. The TI structure extends to the implanted sub-collector depth

injection and latchup concerns. From an ESD design implementation perspective, this allows the placement of an ESD structure closer to other structures without the concern of parasitic interaction.

For a p^+/n-well diode input node ESD network, this structure will allow for a low capacitance sub-collector-to-substrate metallurgical junction ESD element. The TI-bound cathode and STI-bound anode p^+/n-well diode structure will provide a very low capacitance diode structure.

A BiCMOS SiGe technology p^+/n-well with the low doped sub-collector implant and trench sidewall was designed with variable length and multi-fingers. HBM, MM, and TLP measurements show good ESD linearity within a single finger and in multiple fingers with no clear roll-off implications. TLP measurements of the p^+/n-well structure exceeded the 4.5 A TLP tester limit for structures larger than 300 μm total width (Figure 4.36).

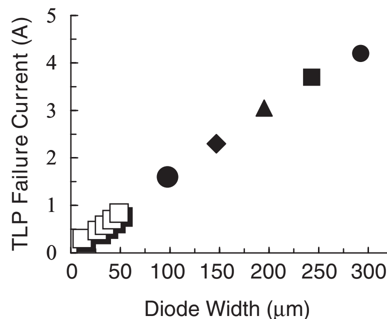

Figure 4.36 TLP measurements of a TI-bound multi-finger BiCMOS p^+/n-well diode (with implanted sub-collector)

4.10 SUMMARY AND CLOSING COMMENTS

In this chapter, the ESD layout, design, and operation of diodes, and diode string ESD networks were discussed. The diode elements discussed were fundamental elements used in CMOS, RF CMOS, and BiCMOS technology. Although the focus was on single-well and dual-well CMOS, the concepts can be extended to triple-well CMOS, triple well BiCMOS, and silicon-on-insulator (SOI) technology.

In Chapter 5, the design and layout of SOI elements are discussed. The chapter will discuss the design of SOI MOSFETs, SOI polysilicon diodes (e.g., Lubistor), and SOI buried resistor elements. The understanding of design and layout of SOI elements is important for the design of ESD elements, receiver networks, and peripheral OCD networks. With the ability to compare bulk CMOS and SOI networks, a better understanding of both bulk CMOS, triple-well CMOS and SOI is achievable.

PROBLEMS

4.1. Assuming a diode string ESD network of *N* successive stages of area A_1, A_2, and A_N, derive a general relationship so that the current is uniform through all successive stages.

4.2. Assuming a first diode string with *N* diode elements and bipolar current gain β_1, and diode area A_1, and a second diode string of *M* diode elements and bipolar current gain β_2, and diode area A_2, derive the general relationship so that the turn-on voltage is equal. Solve for the area A_2.

4.3. Assuming a first diode string with *N* diode elements and bipolar current gain β_1, and diode area A_1, and a second diode string of *M* diode elements and bipolar current gain β_2, and diode area A_2, derive the general relationship so that the on-resistance is equal. Solve for the area A_2.

4.4. Given a circular diode with an annulus first ring of the p^+ diffusion of inner radius R_1, and outer radius R_2, and a second annulus for the n^+-well contact of inner radius R_3 and outer radius of R_4, calculate the diode series resistance. Assume an *n*-well sheet resistance of ρ. Assume that the inner region is not utilized (e.g., inside the inner radius of the p^+ diffusion anode). Given a rectangular *p–n* diode structure with the same *n*-well sheet resistance, what is the width of the rectangular diode to achieve the same diode series resistance? (Note: Assume that the isolation spacing equal to the difference between R_3 and R_2).

4.5. Given a circular diode with a first circle of the p^+ diffusion of radius R_1, and a first annulus for the n^+-well contact of inner radius R_2 and outer radius of R_3, calculate the diode series resistance. Assume an *n*-well sheet resistance of ρ. Given a rectangular *p–n* diode structure with the same *n*-well sheet resistance, what is the width of the rectangular diode to achieve the same diode series resistance? (Note: Assume that the isolation spacing equal to the difference between R_1 and R_2).

4.6. In the above cases, given the linear rectangular diode has the same length as the outer p^+ anode diode edge, assuming the linear diode has a different *n*-well, solve for the

sheet resistance of the linear diode which would achieve the same diode series resistance.

4.7. Solve for the resistance expression derived from the Worley and Bakulin ladder network model where

$$R = \sqrt{\frac{\rho_1}{\sigma_y(1+R_p)}}\frac{4R_p + \left(1+R_p^2\right)D^+ + \alpha l R_p D^-}{(1+R_p)D^-}$$

$$D^+ = \exp\left\{\sqrt{\sigma_y(\rho_1+\rho_2)l}\right\} + \exp\left\{\sqrt{\sigma_y(\rho_1+\rho_2)l}\right\}$$

$$D^- = \exp\left\{\sqrt{\sigma_y(\rho_1+\rho_2)l}\right\} - \exp\left\{\sqrt{\sigma_y(\rho_1+\rho_2)l}\right\}$$

and

$$\alpha = \sqrt{\sigma_y(\rho_1+\rho_2)}$$

$$R_p = \frac{\rho_1}{\rho_2}$$

4.8. From the Worley–Bakulin derivation of the *R–G* ladder network, normalize the resistance expression to the expression to the case of a zero-ohm wire resistance, as well as express as a function of R_p and α

$$R = \alpha l \frac{4R_p + \left(1+R_p^2\right)D^+ + \alpha l R_p D^-}{\left(1+R_p\right)^2 D^-}$$

4.9. Derive the Worley–Bakulin *R–G* diode ladder network assuming the current through the diode network is flowing in and out on the same physical end (e.g., anti-parallel current flow).

4.10. Derive the normalized expression as a function of the zero-resistance wiring case, and as a function of the two parameters.

4.11. Derive the ratio of the resistances for the parallel and anti-parallel wiring cases.

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5 Silicon on Insulator (SOI) ESD Design

5.1 SOI ESD BASIC CONCEPTS

SOI ESD design is distinct from bulk CMOS ESD design as a result of the buried oxide (BOX) film and the MOSFET floating body region [1,2–4]. The BOX decouples the SOI *n*- and *p*-channel MOSFET body region from the silicon substrate [2–4]. The BOX region also separates and isolates the *p*- and *n*-channel SOI MOSFET. Many of the bulk ESD design practices are similar, but new issues need to be addressed in SOI ESD design. In SOI ESD analysis, active areas include SOI electro-thermal simulation and modeling [5–9], experimental work and design integration [11–17,23–24,27], and SOI patents [10,18,19,21,22,25, 26–40].

Although many of the basic concepts of ESD design in SOI and bulk CMOS technology are similar, the actual physical layout of the structures and ESD network integration can be significantly different. This has led to the need for new semiconductor devices, new ESD design layout, and new circuit innovations.

Some of the fundamental distinctions are as follows:

- No vertical parasitic devices exist.
- No lateral device exists without formation of a MOSFET gate structure; hence, SOI MOSFETs, diodes, and resistors utilize gate structures.
- Vertical shallow trench isolation (STI)-bound p^+ anode/*n*-well cathode diode structure does not exist in SOI technology.
- *n*-well-to-substrate ESD diode elements do not exist in SOI technology.
- Parasitic CMOS-based *pnpn* structures do not exist in SOI technology.
- There are no vertical diode elements, hence no advantage to the area dependency in the design of structures.

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- There are no guard ring structures needed in SOI technology.
- There are no local substrate contact guard rings for SOI devices.
- *n*- and *p*-well regions do not exist.
- Bulk “floating gate tie-downs” and well tie-downs do not exist.
- Unique electrical connections need to be established with the substrate region in SOI technology.

As a result of the above issues, although the basic concepts in SOI ESD design are the same, there are significant differences in the physical layout and device choices [1]. Additionally, even with the direct mapping of circuits, the ESD response circuit can be significantly different, leading to new ESD issues and failure mechanisms.

Where at first glance, the presence of the BOX appears to be a serious decrement to SOI ESD design [2–5], the issues above can lead to significant advantages over bulk CMOS silicon ESD design [1].

The lack of vertical parasitic devices leads to a reduction of the complexity of device-to-device interactions. In bulk CMOS, a significant number of ESD failures and concerns are unanticipated interactions between adjacent elements and adjacent circuits; in SOI, this is not true. In bulk CMOS ESD design, the interaction between adjacent elements and circuits leads to complex ESD design rules and logical-to-physical checking computer-aided design (CAD) tools. In SOI, ESD design is significantly simplified because of the elimination of these unexpected interactions and current paths. This simplifies the ESD analysis and prevents undesired interaction.

SOI ESD design will be dependent on library elements and supported structures not parasitic elements, which are not well quantified. In technology development, the parasitic model elements are used, which are not well defined and do not have electrical models. Additionally, they are not present in the schematic design. As a result, the awareness and predictability of ESD results are hampered. In bulk CMOS technology, these limited the prediction and projection capability of ESD robustness of products. Hence, the elimination of bulk CMOS parasitic device interaction has significantly assisted the predictive capability and assurance of SOI ESD results.

The lack of parasitic transistors and the physical isolation of the structures also eliminate the traditional CMOS latchup observed in bulk CMOS technology. This is because there are no parasitic vertical or lateral *pnp* and *npn* elements. In bulk CMOS, the parasitic *pnp* bipolar transistor *pnp* base and collector are formed from the *n*-well and substrate, respectively. The parasitic *npn* bipolar transistor base and collector are formed from the substrate and the *n*-well, respectively. These parasitic transistors share the same physical regions, and are cross-coupled forming a Shockley diode *pnpn* structure. The CMOS parasitic *pnpn* structure can undergo regenerative feedback, leading to CMOS latchup. In SOI technology, the lack of the *n*-well region, *p*-well, and the physical isolation formed from the BOX prevents the coupling of these elements in the substrate wafer. As a result, the spatial separation between SOI *n*- and *p*-channel elements can be minimum without concern with CMOS latchup. In bulk CMOS technology, guard ring structures are used to minimize electrical overshoot, undershoot, and latchup (e.g., *n*-well guard rings and p^+ substrate contacts). In ESD structures, the spacing of these guard ring elements must be separated to avoid interaction between the guard ring structures and ESD elements. As a result, the guard

ring physical structure as well as the physical spacing relative to the ESD element can require a significant percentage of the allocated area for ESD design. As the ESD structure size is scaled or in small ESD networks, the percentage of area dedicated to the guard ring and the physical spacing may increase. In SOI technology, these can be eliminated. The elimination of the ESD guard ring structures has a significant impact on the total ESD area. This area can also be taken advantage of by utilizing for active elements.

The lack of the vertical bipolar also simplifies the understanding of the SOI ESD diode element. In bulk CMOS, the "ESD p^+/*n*-well diode" is a strong function of the physical design and the semiconductor process. From bulk CMOS ESD analysis, the semiconductor *n*-well process has significant effect on the ESD diode response. It was shown that the ESD robustness has a U-shape dependency as a function of the well sheet resistance [1]. At high *n*-well sheet resistance, it has been shown by T. J. Maloney and S. Voldman [1] that there exists a vertical bipolar current gain magnitude where the element responds as a vertical bipolar element. In SOI technology, the complexity of the response of the ESD SOI is significantly reduced because of the lack of the diode-bipolar duality, which exists in the bulk CMOS ESD element.

Another advantage of SOI ESD design is the lack of CMOS bulk floating gate tie-downs. Floating gate tie-downs and well tie-downs can interact with adjacent CMOS devices. In SOI technology, the interaction does not occur because of the physical isolation introduced by the STI and BOX regions.

The physical separation of the *n*- and *p*-channel MOSFET from the bulk substrate allows the ability to bias or isolate the MOSFET body. This allows for symmetrical design practices as well as new opportunities for dynamic threshold MOSFET techniques to be used in circuit design. A second key issue is how this influences the response during ESD events. In bulk CMOS, charged device model (CDM) mechanism ESD failures occur in MOSFET gate structures in the MOSFET gate dielectric between the MOSFET channel region and the gate electrode. In ESD SOI technology, this mechanism does not occur; the disadvantage is that new mechanisms occur in new locations.

In SOI ESD design, there are still some underlying fundamental concepts that one can adhere to in order to have effective ESD results, similar to bulk silicon design:

- Provide a solution that establishes a low-voltage trigger element, which can discharge a high current.
- Provide spatially uniform current density within the trigger element.
- Avoid non-uniform localized Joule heating within the trigger element.
- Avoid electrical connections that exceed the breakdown voltage of the SOI MOSFET gate structure.
- Operate the device under the SOI MOSFET second breakdown voltage.
- Improve thermal stability of the SOI MOSFET structure.

The ability to provide a low-voltage trigger element can be achieved by the following techniques:

- Minimum channel length MOSFETs to provide low SOI MOSFET snapback voltages.

- Low threshold voltage SOI MOSFETs.
- Gate coupling techniques.
- Drain coupling techniques.
- Body coupling [23–26].
- Dynamic threshold SOI MOSFET coupling techniques [23–26].

SOI MOSFET ESD structures can discharge high currents given by the following means:

- Low-resistance salicide films.
- Low-resistance metallurgy (e.g., copper interconnects).
- Low threshold SOI MOSFET for increased MOSFET current drive (e.g., maximize V_G–V_T).
- Dynamic threshold voltage techniques [23–26].

Spatial uniformity is achieved in the MOSFET ESD structure by the following means:

- Provide design symmetry in the metal and contact design.
- Ballasting in the direction of the SOI MOSFET current flow.
- Ballasting perpendicular to the direction of the SOI MOSFET current flow.

Avoidance of localized heating in the SOI MOSFET structure can be achieved by the following means:

- Provide design symmetry in the metal and contact design.
- Ballasting in the direction of current flow.
- Ballasting perpendicular to the MOSFET current flow (e.g., lateral ballasting).
- Introduce external ballasting elements in the SOI MOSFET ESD circuit.
- MOSFET structures with extension implants or deep low-doped drain regions.
- Increase body doping concentration to increase intrinsic temperature.

Avoidance of failure of the SOI MOSFET structure due to dielectric breakdown can be achieved via the following means:

- Avoid SOI MOSFET gate-to-power rail direct connections.
- Avoid MOSFET gate-to-pad direct connections.
- Avoid SOI MOSFET gate-to-drain connections.
- Avoid SOI MOSFET gate-to-source connections.

Avoidance of MOSFET second breakdown can be achieved by the following means:

- Avoid the ESD MOSFET from undergoing MOSFET snapback.
- SOI MOSFET gate-coupling techniques.
- SOI MOSFET body- and gate-coupling techniques.
- Increase doping concentration to raise the intrinsic temperature of the SOI MOSFET channel region.

Although many of the basic concepts of ESD design in SOI and bulk CMOS technology are similar, the actual physical layout of the structures and ESD network integration can be significantly different. Some of the fundamental distinctions are as follows:

- No vertical parasitic devices exist.
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- Vertical STI-bound p^+ anode/*n*-well cathode diode structure does not exist in SOI technology.
- *n*-well-to-substrate ESD diode elements do not exist in SOI technology.
- Parasitic CMOS-based *pnpn* structures do not exist in SOI technology.
- There are no vertical diode elements, hence no advantage to the area dependency.
- There are no guard ring structures needed in SOI technology.
- There are no local substrate contact guard rings for SOI devices.

As a result of the above issues, although the basic concepts in SOI design are the same, there are significant differences in the physical layout.

5.2 SOI ESD DESIGN: MOSFET WITH BODY CONTACT (T-SHAPED LAYOUT)

MOSFET scaling on bulk silicon has been the primary focus of the semiconductor and microelectronic industry for achieving CMOS chip performance and density objectives. Using SOI substrate wafers, many of the concerns and obstacles of bulk-silicon CMOS can be eliminated. CMOS-on-SOI provides low power consumption, low leakage current, low-capacitance diode structures, good sub-threshold *I–V* characteristics, low soft error rate (SER), good SRAM access times, and other technology benefits [12].

One of the barriers of implementing SOI technology is the ‘‘floating body’’ issue [2,3]. In the case of the floating body issue, where no MOSFET body contact exits, the MOSFET body potential will be a function of the capacitive coupling of the MOSFET. The MOSFET body potential will be capacitive coupled to the MOSFET drain, MOSFET source, and MOSFET gate electrodes. Current injected into the MOSFET body will also lead to charging effect. In the case of the ‘‘floating body’’ MOSFET, the SOI MOSFET threshold voltage will

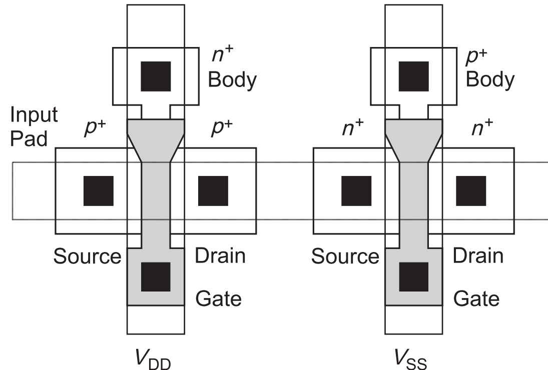

Figure 5.1 H-shaped SOI MOSFET with SOI MOSFET body contact

be modulated by the SOI MOSFET body and channel region. Additionally, the current and voltage history of the SOI MOSFET body will affect the voltage state of the SOI transistor. To address the ‘‘floating body’’ condition of an SOI MOSFET, a MOSFET body contact can be placed to control the electric potential of the SOI MOSFET body. The SOI MOSFET body-contact adds an additional contact to the MOSFET structure (e.g., one additional contact beyond the bulk-MOSFET device). The concern of the SOI MOSFET body contact is twofold: first, the addition of the MOSFET body contact impacts chip area; and second, it impacts remapping of bulk-CMOS to SOI technology [12].

SOI MOSFET body-contact can be formed by defining a T-shaped region of silicon on the SOI BOX region (Figure 5.1). The MOSFET source and drain are formed by using a dielectric and polysilicon gate structure. The SOI MOSFET polysilicon gate structure is contacted on one side that extends beyond the SOI MOSFET source and drain, where an electrical MOSFET gate contact is placed on the gate structure. On the opposite side, the SOI polysilicon MOSFET gate structure extends past the SOI MOSFET source and drain definition edge, but only partially to the end of the T-shaped silicon region to allow for the formation of the SOI MOSFET body contact. An SOI MOSFET body contact region is formed by a dopant implant in the silicon region, followed by an electrical contact. The region under the contact is doped with the same dopant polarity as the channel region, but of a higher doping concentration. The construction of the MOSFET gate, source, drain, and body forms an ‘‘H-shaped’’ structure (e.g., a T-shaped silicon region domain) [12].

To provide ESD protection in SOI technology, one of the concerns was the lack of a vertical diode structure for electrical discharge. With the introduction of the MOSFET body contact, although it was a functional and layout design area and remapping concern, is an advantage for ESD protection. The introduction of the SOI MOSFET body allows for the ability to provide a lateral *p–n* diode structure [12].

Using the T-shaped silicon domains, an SOI lateral diode structure can be formed. For example, using a *p*-channel SOI MOSFET device, the SOI MOSFET source and drain region can serve as the anode, and the SOI MOSFET *n*-type channel and body can serve as the cathode. Using an *n*-channel SOI MOSFET device, the SOI MOSFET source and drain region can serve as a diode cathode, and the SOI *p*-channel MOSFET can serve as the anode.

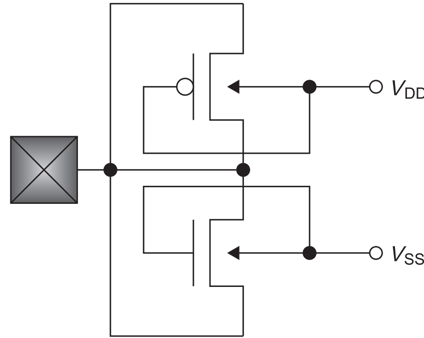

Figure 5.2 SOI double-diode ESD network using CMOS H-shaped (T-shaped) SOI MOSFETs with body contacts

Because both the *p*- and *n*-channel SOI MOSFET bodies are disconnected from the well regions and the substrate, the electrodes can be changed and connected to input pads, power rails, or ground connections to form diode structures. In these cases, the SOI MOSFET gate structures are connected in fashion to avoid dielectric failure during ESD testing.

Figure 5.2 shows an example of the SOI MOSFET design layout for a SOI double diode-circuit that utilizes H-shaped (or T-shaped) SOI MOSFETs in a diode form. Using both a *p*- and a *n*-channel SOI MOSFET, a *p*-channel SOI MOSFET can serve as a ''SOI diode'' to the power supply rail, and the *n*-channel SOI MOSFET can serve as a ''SOI diode'' to the ground power rail. The SOI MOSET layout can be wired across both the SOI *n*- and *p*-channel MOSFETs electrically, connecting the MOSFET source and drain regions. The body and gate contacts can be electrically connected to the respective power supply rails.

An SOI ESD double-diode network can be formed using only SOI *p*-channel MOSFET body-contacted devices (Figure 5.3). A PMOS implementation can use a SOI *p*-channel MOSFET source and drain as the anode of the SOI MOSFET to the power supply voltage, and a second SOI *p*-channel MOSFET whose SOI MOSFET body contact serves as the anode for the diode to the substrate power rail [12].

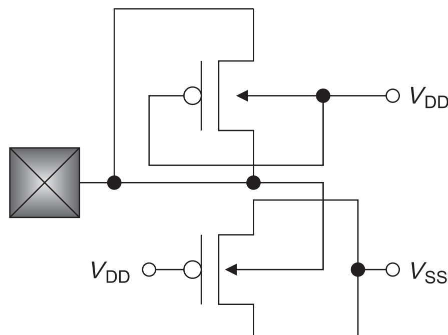

Figure 5.3 PMOS-defined SOI double-diode ESD network using T-shaped body-contacted SOI transistors

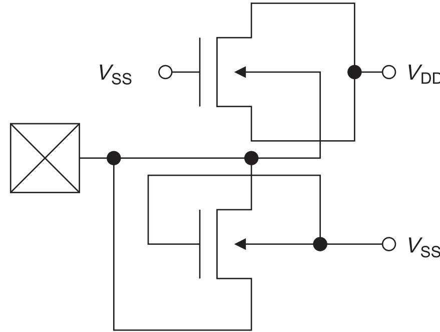

Figure 5.4 NMOS-defined SOI double-diode ESD network using T-shaped body-contacted SOI transistors

An SOI ESD double-diode network can be formed using only SOI *n*-channel MOSFET body-contacted devices (Figure 5.4). An NMOS implementation can use an SOI *n*-channel MOSFET *p*-type body that serves as the anode to the power supply voltage, and a second SOI *n*-channel MOSFET whose SOI MOSFET source and drain serves as the cathode for the diode to the substrate power rail.

An ESD design considerations utilizing the T-shaped SOI MOSFETs with local body contacts are as follows:

- A local SOI MOSFET body contact is needed to avoid lateral resistance effects along the SOI MOSFET channel.
- The SOI MOSFET length should be of the order of the SOI MOSFET width for each unit.

These ESD design considerations limit the effectiveness to use these structures for large SOI ESD diode structures. It is also found that the ability to produce area-compact ESD designs with the T-shaped local body contact structures.

5.3 SOI ESD DESIGN: SOI LATERAL DIODE STRUCTURE

SOI lateral diodes for ESD protection can be constructed using a hybrid device that utilizes both the *p*-channel MOSFET and *n*-channel MOSFET without the use of body contact structure [10,11,13–16]. Using the *p*- and *n*-channel source/drain implants, a mask can be placed on the MOSFET gate structure where the *p*-channel MOSFET source/drain implant forms the anode, and the *n*-channel MOSFET source/drain forms the cathode. This can be formed in either *n*- or *p*-well regions. Source/drain features were defined using STI, which abuts the silicon dioxide (SiO_2) BOX film. Dual work function silicided polysilicon gate electrodes were used for the MOSFET gate conductors. In a first implementation, a *p*-channel transistor used abrupt boron (B) source/drain junctions. The *n*-channel MOSFET source/drain has abrupt non-L_{DD} arsenic junctions. MOSFET source/drain junction depths for both the *n*- and *p*-channel MOSFETs are 0.18 μm. A $TiSi_2$ salicide film is formed on the source/drain junctions. The salicided polysilicon gate structure is placed on a 7.7-nm SiO_2 gate dielectric. In the SOI lateral diode structure, the polysilicon length was set at 1.2 μm.

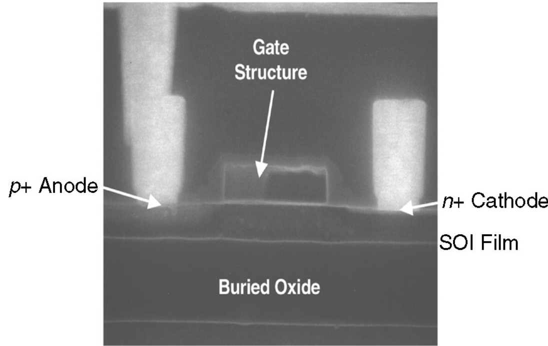

Figure 5.5 Cross-section of an SOI lateral gated diode structure

The mask to define the p^+ and n^+ implants must be placed over the polysilicon-gate structure. In this fashion, the polysilicon-bound diode structure has a polysilicon film with two different dopant types and work functions along the device channel length [13–16]. With the placement of this structure on a BOX, the trench isolation abuts the BOX film, isolating the polysilicon-bound diode structure from adjacent structures. In a 0.25-μm technology, the lateral polysilicon-bound diode structure was studied as a function of the SOI diode perimeter and the polysilicon MOSFET gate structure channel length.

5.3.1 SOI Lateral Diode Design

Figure 5.5 shows a cross-section of the SOI lateral diode structure. Figure 5.6 shows the SOI polysilicon diode ESD layout design. In the design layout, the anode region is enclosed by a polysilicon gate structure. Since the design is an enclosed gate structure, it is necessary to provide an electrical contact to the lateral SOI gate structure. The electrical contact to the gate must be made over the isolation structure [13–16].

5.3.2 SOI Lateral Diode Perimeter Design

Figure 5.7 shows the ESD robustness of a polysilicon-bound gated diode structure as a function of polysilicon perimeter. HBM results show that the ESD results improve linearly with increasing diode perimeter with a design L_{poly} of 1.2 μm. In this structure, the structure size was increased using multiple diode fingers. With no substrate coupling, as the number of fingers increases, the ESD results also increase with the diode perimeter [12,13–16].

5.3.3 SOI Lateral Diode Channel Length Design

The SOI lateral diode design demonstrated a weak sensitivity on the SOI lateral diode channel length. Figure 5.8 shows the HBM ESD results as a function of polysilicon length

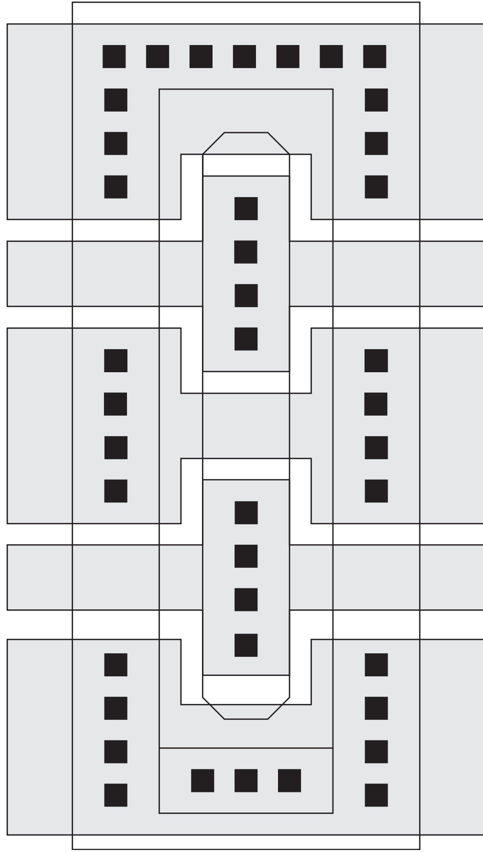

Figure 5.6 SOI lateral diode layout design highlighting the polysilicon gate connection

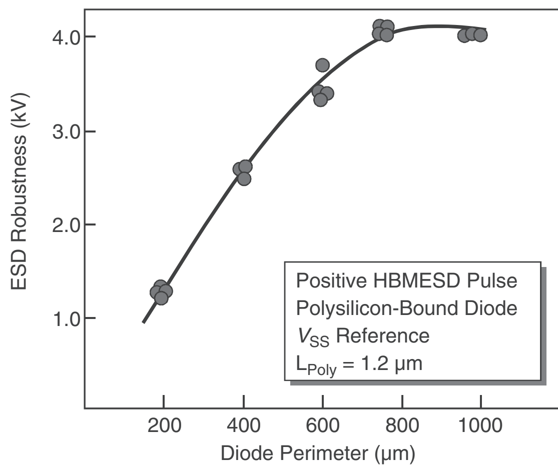

Figure 5.7 ESD results of a ESD polysilicon gated diode structure as a function of polysilicon gate perimeter ($L_{poly} = 1.2\ \mu m$)

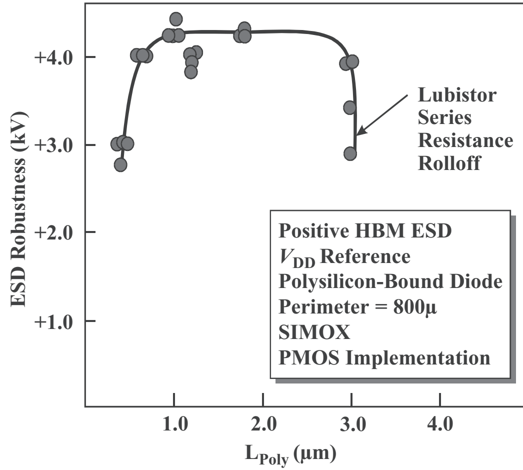

Figure 5.8 SOI lateral diode design ESD results as a function of channel length

for an 800-μm perimeter diode structure. Experimental results demonstrated a large window for channel length operability. In this structure, as the channel length decreases, the p^+ and n^+ diffusion regions approach each other. At some physical distance, the ESD results decrease. Additionally, as the length of the structure increases, ESD results decrease [12–16].

5.3.4 SOI Lateral $p^+/n^-/n^+$ Diode Structure

This structure can be built in either an *n*-well structure or in a *p*-well structure. In the case of an *n*-well structure, the SOI lateral polysilicon-bound diode is a $p^+/n^-/n^+$ implementation. Figure 5.9 shows the cross-section for the SOI $p^+/n^-/n^+$ diode structure. In this structure, the *n*-type halo and *p*-type halo implants are in the *n*-well region. The metallurgical junction is formed at the *n*-well to *p*-channel MOSFET source/drain region [13–16].

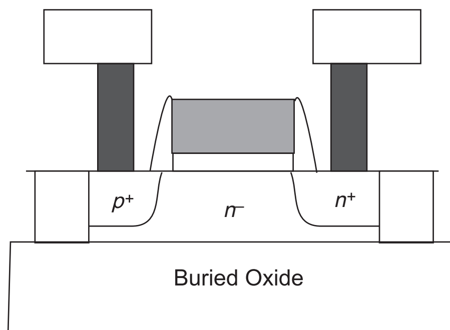

Figure 5.9 SOI ESD lateral diode: $p^+/n^-/n^+$ structure

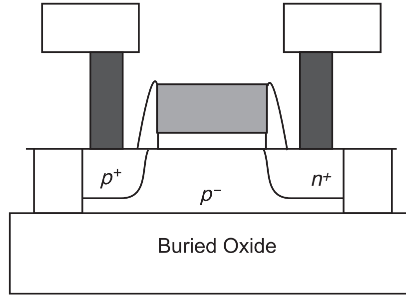

Figure 5.10 SOI ESD lateral diode: $p^+/p^-/n^+$ structure

5.3.5 SOI Lateral $p^+/p^-/n^+$ Diode Structure

Figure 5.10 shows the cross-section for the SOI $p^+/p^-/n^+$ lateral diode structure. In this structure, the structure is formed in a *p*-well. In this structure, the *n*-type halo and *p*-type halo implant are in the *p*-well region. The metallurgical junction is formed at the *p*-well to *n*-channel MOSFET source/drain region [13–16].

5.3.6 SOI Lateral $p^+/p^-/n^-/n^+$ Diode Structure

In the prior implementations, either a *p*-well or an *n*-well was utilized for the SOI lateral diode structure. Using the *n*- and *p*-channel MOSFET source/drain junctions, as well as both *p*- and *n*-well, a SOI lateral $p^+/p^-/n^-/n^+$ diode structure can be formed. Figure 5.11 shows the cross-section for the SOI $p^+/p^-/n^-/n^+$ diode structure. In this structure, the *n*-type halo and *p*-type halo implants are in the *p*-well region. The metallurgical junction is formed at the *p*-well to *n*-well intersection. In this structure, one advantage is that a non-abrupt junction is formed at the metallurgical junction. The structure was first implemented by M. D. Ker and H. Tang and demonstrated superior results compared to the single well lateral SOI structure [17–19].

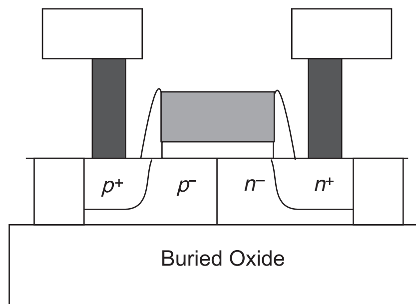

Figure 5.11 SOI ESD lateral diode: $p^+/p^-/n^-/n^+$ structure

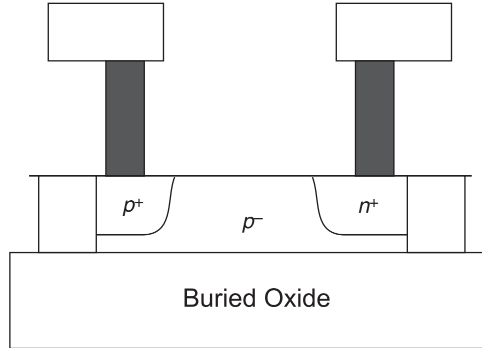

Figure 5.12 SOI ungated lateral diode structure

5.3.7 Ungated SOI Lateral $p^+/p^-/n^-/n^+$ Diode Structure

SOI ESD structures, whether using SOI MOSFETs lateral diode structures or even buried resistor (BR) elements, all contain MOSFET gate structures. One of the key ESD design concerns is the additional loading capacitance of the MOSFET gate structure and its dielectric integrity. An SOI lateral device can be constructed by the removal of the MOSFET gate structure. Figure 5.12 shows the $p^+/p^-/n^-/n^+$ structure without the MOSFET gate structure, first implemented by M. D. Ker and H. Tang [17–19]. The advantage of this implementation is excellent ESD results; the disadvantage is the additional semiconductor processing to remove the SOI MOSFET gate structure.

5.3.8 SOI Lateral Diode Structures and SOI MOSFET Halos

In the design of SOI ESD lateral *p–n* gated diode structures with a single well region, a *n*-type halo is formed near the *p*-channel MOSFET source/drain region, and a *p*-type halo is formed near the *n*-channel MOSFET source/drain region. With the use of a single well dopant type under the gate structure, one of the two halos is the opposite dopant polarity of the well structure. In this case, a ‘‘bad halo’’ is present that adds additional resistance to the SOI diode structure [21]; this was first observed by N. Zamdner [21]. To provide a good SOI ESD protection structure, the ‘‘bad halo’’ is masked to prevent placement in the channel region [21].

5.4 SOI ESD DESIGN: BURIED RESISTORS (BR) ELEMENTS

In SOI circuit design, a high tolerance resistance element is desired for circuit design point accuracy and circuit matching. SOI resistor passive elements are also needed for analog applications and ESD design. The SOI buried resistor (BR), as used in CMOS technology, can be implemented into SOI technology using either an additional silicide block mask

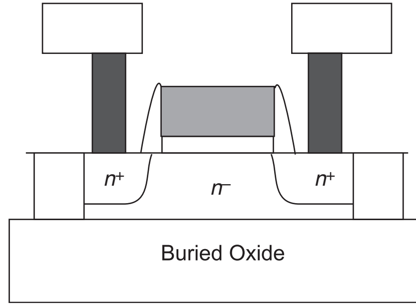

Figure 5.13 An SOI buried resistor (BR) structure utilizing a separate implant and a MOSFET of the same dopant polarity

or the SOI MOSFET gate structure as the silicide block mask (Figure 5.13). The structure is formed by either implanting through the SOI MOSFET polysilicon gate structure, or placing an implant in an isolation region and placing a MOSFET of the same dopant type over the implanted region. In this fashion, the electrical contacts of the BR input and output are formed by the MOSFET source and drain region. The BR implant is typically a lower doped implant below the doping concentration of the SOI MOSFET source and drain [21].

This element is of significant interest for ESD design and its methodologies. BR elements can be used as ballasting elements, diodes, and lateral *npn* devices for ESD design applications. As in bulk CMOS, BR resistors can be used as ballasting elements for off-chip driver (OCD) networks and receiver networks. For SOI technology, there are a few key distinctions in the ESD response of the SOI BR element compared to the bulk BR element:

- SOI BR elements have higher thermal resistance to the substrate leading to a different thermal response during ESD events, and hence will have a different thermal response.
- SOI BR elements do not form a diode structure with the substrate; this prevents current flow in negative polarity ESD events leading to different ESD failure mechanisms and responses.
- SOI BR elements are isolated from the bulk and do not form a metallurgical junction with the substrate; CDM current flow from the substrate to the BR dopant region does not occur.
- SOI BR elements must remove halo implants to avoid higher series resistance during both functional and ESD events.

On the first issue, because of the BOX region, the self-heating will be of a higher magnitude in the SOI BR element compared to the bulk CMOS BR element. This will lead to a different functional as well as thermal response.

SOI BR elements do not form a diode structure with the substrate; this prevents current flow in negative polarity ESD events, leading to different ESD failure mechanisms and responses. During negative HBM and MM events, the ability to discharge current from the input pad to the substrate is typically achievable using bulk BR elements; in SOI, the SOI BR element cannot discharge the negative polarity event to the substrate, leading to a failure

mechanism within the BR, or the need for an alternative ESD solution. Consequently, SOI BR elements are isolated from the bulk and do not form a metallurgical junction with the substrate; this leads to the lack of interaction during CDM events from the substrate. As a result, the CDM current will find an alternative current path.

SOI BR elements are formed by placing an *n*-channel MOSFET into an *n*-well or alternative *n*-implant; this leads to a series *p*-type halo implant in the resistor structure, and a higher series resistance during both functional and ESD events [21].

5.5 SOI ESD DESIGN: SOI DYNAMIC THRESHOLD MOSFET (DTMOS)

SOI dynamic threshold MOSFET (DTMOS) has the advantage of low trigger voltages, high current drive, and high I_{on}/I_{off} current ratio [23]; SOI DTMOS devices have natural advantages for ESD protection. S. Voldman first demonstrated the use of DTMOS networks for ESD protection in 0.22-μm SOI technology [1,24,25]. For the optimization of the SOI DTMOS structure, three basic designs were used [24–28]. Three different structures were constructed where in all cases a polysilicon ring was formed about the n^+ drain, and the polysilicon MOSFET gate structure enclosed the body contact and the n^+ drain (Figure 5.14) [24–28].

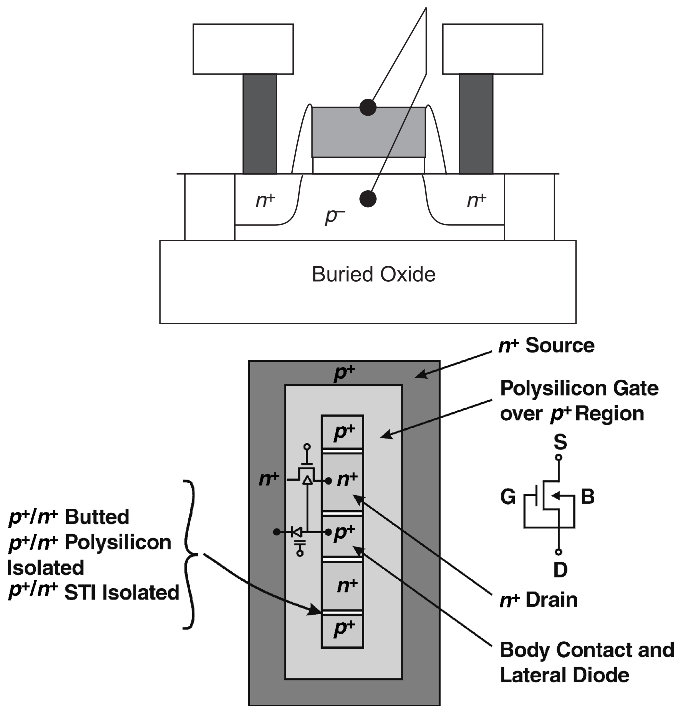

Figure 5.14 Dynamic threshold MOSFET device

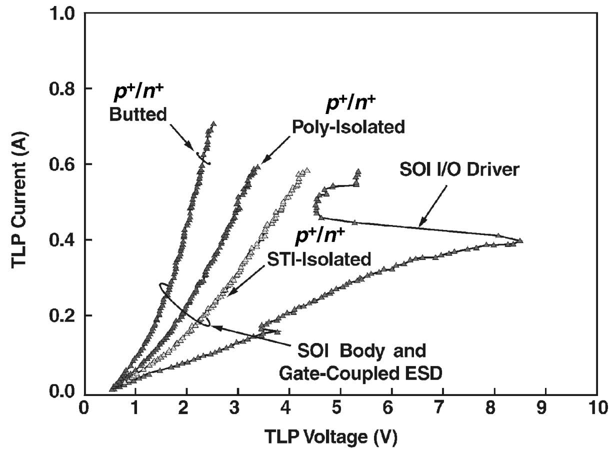

Figure 5.15 Transmission line pulse (TLP) *I–V* characteristic of a SOI off-chip driver (OCD) only, and the I/O OCD with three different SOI DTMOS ESD elements (10 finger structures)

The n^+ MOSFET source enclosed the polysilicon ring MOSFET gate structure. In all these structures, the p^+ body contact (at the drain side) abuts the polysilicon MOSFET ring that serves as a body contact for the MOSFET and forms a lateral SOI gated *p–n* diode structure (SOI Lubistor) adjacent to the MOSFET structure. In the first design, the p^+ body contact abuts the n^+ drain. In this implementation, it was believed that the butted structure would provide the lowest dynamic resistance, and is the most space efficient. The butted structure also is bridged by cobalt salicide. In the second design of the DTMOS device, the p^+ body contact is separated from the n^+ drain region. This design will avoid any technology-related concerns of butted structures and allows for STI of the body-contacted region from the MOSFET drain region. In the third structure, the p^+ body contact is separated by a polysilicon gate structure from the n^+ drain. The third implementation provides polysilicon isolation of the body and the MOSFET drain region, avoiding any STI pull-down mechanisms, independent biasing capability, and introduces an additional lateral diode between the body and the source [25–28].

Our first point of interest was to determine which structure provided the lowest R_{ON}, and avoided any reliability issues. Figure 5.15 shows transmission line pulse (TLP) results of an SOI OCD network and the three different large dynamic threshold body- and gate-coupled ESD diode networks.

In Figure 5.15, a cascaded SOI driver with the first transition of the first MOSFET triggering at 4 V is followed by the second MOSFET triggering at 8.4-V SOI MOSFET. In the measurements, the body- and gate-coupled DTMOS ESD device is configured with the drain, gate, and body connected to the input node and the source connected to V_{DD} power supply. The results show that the SOI body- and gate-coupled DTMOS ESD network with STI between the p^+ and n^+ region provide a higher R_{ON} relative to the other two designs (e.g., $R_{ON} \approx 4\,\Omega$). This can be understood in that the STI does not provide any means of conduction and causes more current crowding and resistance. In the second implementation, where the polysilicon gate region is used between the body and the drain, the addition of the extra diode region provided a lower lateral body resistance providing a lower R_{ON} in the ESD network ($R_{ON} \approx 2.8\,\Omega$). In the third implementation, where the p^+ body and n^+ drain are

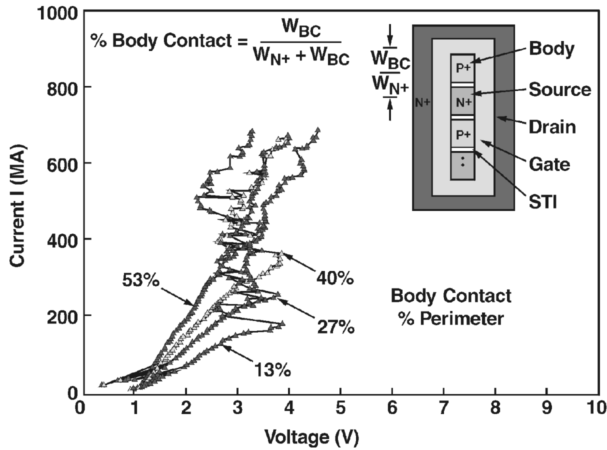

Figure 5.16 TLP *I–V* characteristic of a SOI DTMOS element for various body contact width-to-DTMOS device width

abutted, the $R_{ON} \approx 1.2\,\Omega$. In this structure, the lowest voltage is established at the I/O OCD because of the steep on-resistance. In conclusion, this study showed that the most suitable and efficient structure for a dynamic threshold SOI ESD structure is the structure where the p^+ and n^+ implants are abutting.

To better understand the operation of these structures, it is important to evaluate a matrix where the ratio of the MOSFET drain width and the body width are varied while the total length of the structure remains fixed. In our experimental matrix, as the body width was increased, the MOSFET width was decreased so that the total perimeter of the source is the same width.

Figure 5.16 shows an example of the body- and gate-coupled DTMOS ESD network, where the ratio of the body and drain width are varied. Defining the body contact width, W_{BC}, and the drain width W_N we can form a ratio or percent body-contact as W_{BC} / (W_{BC} + W_N). In Figure 5.16, TLP *I–V* measurements are taken for devices as a function of the percentage of body contact (e.g., for the cases of 13%, 27%, 40%, and 53% body contact). With the observation of the 13% body contact, the first TLP *I–V* characteristic shows that it follows a monotonically increasing current from 0 to 4 V, and this is followed by snapback of the DTMOS device. As the body voltage rises, the diode formed between the body contact and the MOSFET source first turns on, and at the same time, the MOSFET threshold voltage decreases. As the gate voltage exceeds the threshold voltage, the dynamic threshold MOSFET device also turns on, with a high I_{dsat}. When the voltage across the structure approaches the snapback voltage, this structure undergoes a snapback state. As the percent body contact ratio increases, the dynamic on-resistance also increases. With lower on-resistance, the discharge current capability improves.

5.6 SOI ESD DESIGN: DUAL-GATE (DG) MOSFETs

With the continued struggle to scale MOSFET devices to the Sub-tenth Micron Era, semiconductor engineers have been pursuing new directions in MOSFETs. To achieve

both high density and high performance, the MOSFET is leaving the paradigm of the MOSFET evolution in two-dimensions and must address a new revolutionary move to the third dimension. A potential evolutionary path for the MOSFET was a two-dimensional (2-D) bulk CMOS planar MOSFET device, to the 2-D single-gate (SG) SOI MOSFET, to the 2-D dual-gate (DG) SOI MOSFET device. SOI ESD circuit implementations in SG-SOI devices can be extended into DG-SOI [26–28,30].

The DG-SOI MOSFET was to provide a means to produce more current for a given planar device. In the case of a DG-SOI MOSFET structure, a second gate is formed either within the BOX region or below the BOX region. The problem with the DG-SOI MOSFET is processing costs and alignment of the second gate. The formation of the second gate structure within the BOX region will require either growth over the first gate, or bonding and etch-back style process integration. A second gate can be formed under the first gate structure using an implanted gate structure, but this suffers density, loading capacitance, leakage issues, and too thick of a gate oxide for the second gate structure. As a result, the progress in the area of a buried second gate has had little success of implementation.

5.7 SOI ESD DESIGN: FINFET STRUCTURE

Because of the progress in the DG-SOI MOSFETs, new directions have been taken to move in "surround" gate or "wrap-around" gate structures [41–46]. In 1986, Takahashi *et al.* [41] proposed the Surround Gate Transistor (SGT) device with the objective of achieving a smaller transistor structure. D. Hisamoto *et al.* [42] proposed the Fully Depleted Lean-Channel Transistor (DELTA) device, which was a novel vertical ultra-thin SOI MOSFET structure. This evolution has progressed toward a silicon pillar device with a wrap-around gate in both bulk CMOS and in SOI technology. Tang *et al.* [46] developed a quasi-planar double-gate device known as a "FinFET." Concepts of surround gates, wrap-around gates, and non-planar dual gates were all different strategies on constructing the non-planar MOSFET into narrow width silicon pillars, leaving the wafer surface to form the 3-D MOSFET structures [41–46].

In a FinFET structure, the key design parameters is the fin height H, fin thickness, T_{si}, and the effective channel length, L_{eff}, and the number of parallel fin structures, N_{Fin}. For analysis of the FinFET, we can define an effective channel length as

$$L_{eff} = L_{poly} - \Delta L$$

In a double-gated (DG) FinFET device, the contours merge, at

$$T_{si} \cong -2\frac{\varepsilon_{si}}{\varepsilon_{ox}}T_{ox}$$

and we can define an effective film thickness as

$$T_{eff} = T_{si} + 2\frac{\varepsilon_{si}}{\varepsilon_{ox}}T_{ox}$$

A more accurate solution derived the following relationship [41]

$$T_{\mathrm{eff}} = \sqrt{T_{\mathrm{si}}^2 + 4\frac{\varepsilon_{\mathrm{si}}}{\varepsilon_{\mathrm{ox}}} T_{\mathrm{ox}} T_{\mathrm{si}}}$$

The SOI FinFET structure forms a parallel-piped surrounded by isolation material below and above the conducting region, and the thermal sinks formed by the boundary conditions. For evaluation of a parallel-piped in an infinite insulating medium, let us assume a source has the dimension of a SOI FinFET width $W = T_{\mathrm{eff}}$ in the x-dimension, and L_{eff} in the y dimension, and FinFET height H in the z-dimension, but applying a parallel-piped displaced distance D below the boundary condition $z = 0$ and an image source of equal and opposite strength above the $z = 0$ plane at $z = \mathrm{D}$

$$T(x, y, z; t) = \frac{1}{8\rho c V(\kappa)^{3/2}} \int_{t'=0}^{t'=t} \frac{P(t')\mathrm{d}t'}{[(t - t')]^{3/2}} F(x - x', y - y', z - z', t - t')$$

with

$$F(x - x', y - y', z - z', t - t') = F_x(x - x' : t - t') F_y(y - y'; t - t') F_z(z - z'; t - t')$$

where

$$F_x(x - x', t - t') = \int_{-W/2}^{W/2} \exp\left\{-\frac{(x - x')^2}{4\kappa(t - t')}\right\} \frac{\mathrm{d}x'}{\sqrt{\pi}}$$

$$F_y(y - y', t - t') = \int_{-L/2}^{L/2} \exp\left\{-\frac{(y - y')^2}{4\kappa(t - t')}\right\} \frac{\mathrm{d}y'}{\sqrt{\pi}}$$

$$F_z(z - z', t - t') = \int_{-(D+H)}^{-D} \exp\left\{-\frac{(z - z')^2}{4\kappa(t - t')}\right\} \frac{\mathrm{d}z'}{\sqrt{\pi}} + \int_{D}^{D+H} \exp\left\{-\frac{(z - z')^2}{4\kappa(t - t')}\right\} \frac{\mathrm{d}z'}{\sqrt{\pi}}$$

The integral expression can be expressed as error functions using a transformation of variables. The expression for temperature in an infinite medium can be put in the form

$$T(x, y, z; t) = \frac{1}{8C} \int_{t'=0}^{t'=t} P(t') H(x, y, z; t - t') \mathrm{d}t'$$

where $V = L_{\mathrm{eff}}\ T_{\mathrm{eff}}\ H$ is the volume of a single FinFET region, and letting $C = \mathrm{c}\ \rho V$, we can write the function containing the spatial dependence as the product of the error functions

$$H(x, y, z; t - t') = H(z; t - t') \prod_{i=x,y} \left[erf\left(\frac{(L_{x_i}/2) + x_i}{\sqrt{4\kappa(t - t')}}\right) + erf\left(\frac{(L_{x_i}/2) - x_i}{\sqrt{4\kappa(t - t')}}\right)\right]$$

and

$$H(z; t - t') = \left[erf\left(\frac{z + D + H}{\sqrt{4\kappa(t - t')}} \right) + erf\left(\frac{-D - z}{\sqrt{4\kappa(t - t')}} \right) + erf\left(\frac{z - D}{\sqrt{4\kappa(t - t')}} \right) + erf\left(\frac{D + H - z}{\sqrt{4\kappa(t - t')}} \right) \right]$$

From this solution, assuming the FinFET is surrounded by insulating regions, the solution for self-heating within the SOI FinFET can be obtained. For electrostatic discharge (ESD) phenomena, there are two issues. The first issue is how the current distributes between multiple parallel FinFET devices. A second issue is the relative width of a current constriction to the effective fin width and height. The first issue is similar to any other parallel configuration in that the current distribution is a function of the ballasting and matching between any two parallel elements during second breakdown. The second issue is the volumetric nature of the current constriction and relative scale length compared to the dimension fin height H and fin width T_{eff}.

From our earlier analysis of current constriction in planar MOSFETs, we can anticipate that the relationship may have a one-to-one equivalency of planar MOSFET width to the fin height, of N parallel FinFETs, assuming that there is conduction in some number M where M is equal to or less than N

$$W_{\text{eff}} \approx \sum_{i=1}^{i=N} (2H_{\text{eff}})i = \sum_{i=1}^{i=N} \frac{(\mathrm{I_m})_i}{\int_{T_{\max}}^{T} \mathrm{d}T \left[\frac{4\rho K}{\sqrt{2\left\{ \int_{T_{\max}}^{T} \rho(T')K(T')\mathrm{d}T' \right\}}} \right]}$$

When the fin height and width are of the same order of magnitude, it is possible that the arithmetic mean may serve as a better metric, where the H_{eff} and the T_{eff} are the ESD effective widths based on the percentage of the fin height and the electrical effective FinFET width [1]

$$W_{\text{eff}} \approx \sqrt{H_{\text{eff}} T_{\text{eff}}} = \sum_{i=1}^{i=N} \frac{(\mathrm{I_m})_i}{\int_{T_{\max}}^{T} \mathrm{d}T \left[\frac{4\rho K}{\sqrt{2\left\{ \int_{T_{\max}}^{T} \rho(T')K(T')\mathrm{d}T' \right\}}} \right]}$$

5.8 SOI ESD DESIGN: STRUCTURES IN THE BULK SUBSTRATE

In ultra-thin film SOI (UT-SOI), fully depleted SOI (FD-SOI), and highly scaled partially depleted SOI (PD-SOI), the ability to provide ESD protection will be more difficult.

Additionally, in mixed signal application, where some circuits are on SOI and others are in the bulk, there is the possibility of producing ESD structures in the bulk substrate. M. Chan and C. Hu demonstrated a reduction in the ESD robustness of MOSFET structures formed on SOI wafers, and proposed a hybrid process where some circuits are formed on the SOI and other are formed in bulk CMOS wafer [4]; this is achieved by removal of the SOI BOX region on some sections of the substrate wafer. A disadvantage of this method is the topography issues and cost. Alternative methods were proposed forming dual SOI films vertical ESD SOI structures with uniform topography [38] above the BOX, and three-dimensional (3-D) SOI ESD structures and contact structures below the buried oxide [39,40]. The dual SOI film will lessen the impact of scaling and allow vertical SOI structures, and the 3-D SOI ESD under the BOX will allow for vertical integration, uniform topography, reduce chip area, and allow utilization of the SOI bulk region.

5.9 SOI ESD DESIGN: SOI-TO-BULK CONTACT STRUCTURES

In SOI wafer, the substrate region, the BOX, and the thin silicon film and corresponding interconnects form a capacitor-like structure, where the BOX serves an an insulator. In the case of no electrical connection between the front and back of the wafer, the electrostatic potential of the substrate wafer will modulate the SOI electrical circuitry. S. Geissler showed that by charging or discharging the substrate wafer, the logic state of the functional circuits could be modified during functional testing; it was shown that by handling the wafer backside, the logic state of SOI microprocessors could be altered. Additionally, failure of the BOX region can be observed from CDM-like ESD events in the case of no electrical connection. Without a means to provide the ability to shunt the electrical charge between the front and the back of the wafer, it is anticipated that electrical discharge will occur along the edge of a SOI semiconductor chip (e.g., surface discharge) or failure of the BOX. To address both the functional and this ESD issue, electrical contact structure can be formed by etching through the BOX to establish a contact structure [35–37]. SOI contact structure consists of metal or polysilicon contact structures. These contacts serve two roles: a first role is an electrical contact to bias the backside and prevent electrical discharge, and a second role for the formation of ESD structures under the BOX.

5.10 SUMMARY AND CLOSING COMMENTS

In Chapter 5, an introduction of SOI ESD device structures highlighted the use of a MOSFET and lateral SOI diode structures, which have been used to allow the integration of SOI into a mainstream applications, such as microprocessors. The focus of this chapter was on SOI lateral-gated diode structures, since these are the primary vehicle of ESD protection today in partially depleted SOI, ultra-thin SOI, and radio frequency SOI (RF-SOI). DTMOS SOI was also discussed; these elements were utilized as prototypes for future applications. Extension of these concepts can be utilized for dual gate SOI (DG-SOI) and 3-D SOI structures.

In Chapter 6, the design and layout of off-chip driver (OCD) networks is discussed, where OCD design and layout for single-MOSFETs and stacked (e.g., series cascode) MOSFETs is discussed. Chapter 6 will discuss the issue of separated versus integrated series cascode

MOSFET design. The understanding of design and layout of OCD networks is important for achieving good ESD results in bulk CMOS, triple well CMOS, and BiCMOS Silicon Germanium applications.

PROBLEMS

5.1. Given an SOI double-diode network on an input node. Assume that the gate of the SOI p^+/n^+ element is connected to its cathode. Assume the top element is connected to a V_{DD} power supply, and the second element is electrically connected to V_{SS} power supply. Assume an oxide breakdown voltage of V_{OX}, derive a relationship for the maximum pad voltage when gate oxide breakdown occurs. Evaluate all positive and negative polarity cases.

5.2. For the network in Problem 1, assume that the circuit is used to interface with a second power supply voltage V_{DD2}, which exceeds V_{DD}. Derive the voltage conditions across the gate oxide of the ESD network. Derive the condition for breakdown to occur for all positive and negative states where the input can be varied from V_{DD2} to ground potential.

5.3 To avoid electrical failure of SOI ESD networks, the gate electrode can be de-coupled from the SOI diode cathode region. This can be electrically connected to an inverter circuit whose input is zero, and whose output is the power supply voltage V_{DD}. Assuming a long channel inverter network with a *p*-channel resistance and *n*-channel resistance, derive the voltage across the gate electrode for the mixed voltage states (e.g., V_{DD2} and V_{SS}) on the input pad. Derive when failure will occur in the oxide.

5.4. For resistor ballasting, an SOI MOSFET is to be used as a ballasting resistor. How can you design an SOI MOSFET in order to use the body and channel as a ballast resistor? How can you integrate the SOI MOSFET ballast resistor with an SOI MOSFET for a OCD network?

5.5. An SOI MOSFET is used to form a resistor using two-body contacts and the channel region. Derive an equation for the SOI body resistor element. Assume we desire the resistor to be a pinch resistor by biasing of the SOI MOSFET source and drain junctions. Derive a model for the resistor based on a source and drain voltage condition.

5.6. For an SOI network, an SOI half-pass transmission gate is used in an SOI MOSFET receiver network. Assume a semiconductor chip is charged through the substrate. Assume the substrate region under the BOX is electrically connected to the V_{SS} power rail. Assuming that during an CDM event, the charge does not flow through the SOI MOSFET receiver network, but instead transfers from the V_{SS} to the V_{DD} power rail through the chip capacitance. The charge is transferred from the V_{DD} power supply to the input pad through the SOI half-pass transmission gate through the gate structure. Derive the voltage conditions across the half-pass transistor when the signal pad is grounded. How do you provide an ESD design solution to avoid SOI half-pass transistor failure?

5.7. SOI ESD networks can be placed under the BOX region. Estimate the capacitance loading of an ESD device under the BOX region for a minimum design rules, and compare this to an equivalent element above the BOX region.

5.8. SOI lateral *p–n* ESD devices can be constructed using the polysilicon gate electrode as the block mask between the p^+ region and the n^+ region. Using a mask, the gate region can be removed. Compare the capacitance loading effect of a gated and ungated SOI lateral *p–n* diode. Assume the region between is the same implant type.

5.9. Using Green's function analysis, derive a model for the SOI BR element, assuming the resistor element is a parallel-piped region.

5.10. Derive a thermal model for the BOX using a thermal resistor and thermal capacitor. Derive the change in the temperature as a function of BOX scaling.

5.11. Given an SOI FinFET structure, how many parallel FinFETs are needed to discharge a 1 kV HBM pulse? Assume the SOI FinFET conduction is the full width of the structure and evenly ballasted through all parallel elements.

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6 Off-Chip Drivers (OCD) and ESD

6.1 OFF-CHIP DRIVERS (OCD)

Electrostatic discharge (ESD) design of a transmitter circuit, also known as OCD, is a fundamental piece of providing ESD protection for a semiconductor chip design. In system environments, OCD networks transmit the signals between semiconductor chips as well as from the semiconductor system to outside of the system. These semiconductor chips can have different power supply voltages, different technology generations, and different technology types; in this environment, it involves both mixed-signal and mixed-voltage interface conditions. Additionally, standards are established for signal transmission to allow standardization of the signal levels being transmitted between logic, memory, analog, and other support circuitry. At the same time, there are also application requirements. These requirements can include the following concepts:

- Power supply-to-power supply sequence independence.
- Input pin-to-power rail sequence independence.
- ‘‘Power boundary’’ conditions.
- Cold sparing requirements.
- Fail safe requirements.
- ‘‘Hot socket’’ or ‘‘hot plug’’ requirements.

The first concept of power supply-to-power supply sequence independence is the requirement that there are not sequencing conditions on the states and rates of the different power supply within a given chip or system; the second condition is the same condition that applies between the signal pins and any power supply rail. The third condition, ‘‘power boundary constraints’’ is a general concept of power flow in or out of any section of a system

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when certain elements are in powered or unpowered states. Cold sparing is a concept that some segments of a system are powered or unpowered, and the system must not use power to the unused or unpowered sections of a system; this language is used in redundant and power-managed segments of a system (e.g., redundant segments of a space application, microprocessor, or even the voltage island concept). The concept of "fail safe" is similar—the capability to "fail" without detriment to other devices that remain powered. A fail safe OCD prevents failure when a receiver is not connected, whereas the unconnected receiver shows no detriment to the system. Hot plugging is the ability to remove or insert a chip or board into a system without having to power up or power down a chip, board, or system without destruction to signal integrity or system failure. As a result, a large plethora of OCD circuits exist, which satisfy these applications, and a large number of ESD design issues and ESD circuit topologies are associated with these OCD network conditions.

6.1.1 Off Chip Drivers I/O Standards and ESD

In peripheral I/O design, different logic levels exist for the different power supply voltages for receiving or transmitting signals. These logic levels will be a function of the transmitted power supply voltage, and the receiving power supply voltage of the two system components.

TTL standard was valuable for 5.0 V peripheral I/O interfaces. The TTL standard took advantage of bipolar transistors as well as CMOS technology. The TTL standard uses large current levels to drive logical "1" above the 3.5 V level, as well as logical "0" below 1 V levels. A characteristic of TTL signals is that the inputs to a gate rise toward a logical "1" if unconnected; this requirement for driving a TTL input is to "pull-down" the level to near 0 V. The current levels used for TTL drivers are typically of a milliamperes (mA) level for a given input; this results in significant power consumption and limited speed for fast applications. The response time of TTL gates is on the order of tens of nanoseconds (ns). As a result, applications are limited to clock speeds of 50–100 MHz.

From an ESD perspective, the response of TTL networks is on the same time scale as ESD phenomena. The speed of TTL networks are on the order of the rise time of the HBM impulse, but slower than the rise time of machine model (MM) and charged device model (CDM) events.

As MOSFET transistors were scaled, the power supply voltage level decreased. With the lowering of the power supply voltage and the need for faster data rates, new logic standards are established. Some of the voltage standards established are as follows:

- LVTTL.
- GTL [1, 2].
- HSTL [3].
- SSTL [4–6].

TTL, LVTTL, GTL, HSTL, and SSTL logic levels will require different circuit topologies in order to receive and transmit signal [7]. As a result of these logic level standards for transmission or receiving, the mixing of levels will lead to new circuit innovations and new ESD requirements [8–41]. As the standard voltage levels decrease (e.g., the expected data rates increase), the requirement on the ESD protection strategy will be modified [17–21,

31–33,37–41]. As the logic standard performance increases, the desire to have a lower capacitance ESD network will be more significant; this will influence the ESD input device type and size, the power bussing, and the type of ESD power clamp and its placement requirements. As the I/O evolution transitions take place from 100 MHz TTL applications to 1–10 GHz applications, new ESD scaling requirements will occur. Additionally, as the speed of the I/O becomes faster, the circuitry will be more responsive to the ESD events (e.g., HBM, MM, and CDM). This will inevitably change the nature of how the devices, the circuits, and the semiconductor chip react to the ESD events.

6.1.2 OCD: ESD Design Basics

ESD design of OCD networks, independent of the circuit or structure, have some fundamental design concepts and objectives:

- Buffering: Provide an ESD design strategy that buffers the OCD network and have an independent ESD network discharge the ESD current.
- Current sharing: Provide an ESD design strategy that utilizes the OCD to assist in the ESD current discharge additional to the ESD network.
- Ballasting: Provide an ESD design strategy that utilizes the OCD network, and uses resistor ballasting to distribute the ESD current through the network to maximize the ESD efficiency in the discharging structure.
- Self-protection: An ESD strategy that uses the OCD network as the ESD protection network with no additional elements.

A first ESD strategy is to provide ESD protection in OCD networks by preventing the flow of current into the network. This can be achieved by using resistive elements. Resistors can buffer the OCD network to avoid avalanche breakdown and second breakdown. Whether MOSFET or bipolar OCD networks, using series resistor elements can achieve this objective.

A second ESD strategy is to allow the OCD to participate in discharging the ESD current. This ESD design practice can be implemented in such a fashion to utilize the area of the OCD as well as the ESD element.

A third ESD strategy is to allow the OCD to participate in the discharging the ESD current, but maximize the current distribution within the OCD network. In this fashion, this prevents failure of the OCD network, and yet allows the ability of the OCD to discharge the ESD current.

In a fourth ESD design practice, the OCD network provides the ESD protection. In this fashion, no additional area is used for the ESD network, and the physical OCD network is optimized for performance and ESD objectives.

6.1.3 OCD: CMOS Asymmetric Pull-Up/Pull-Down

In CMOS OCD networks, *p*-channel MOSFET devices are used as pull-up elements, and *n*-channel MOSFETs are used as pull-down elements [37]. In a CMOS OCD network, the

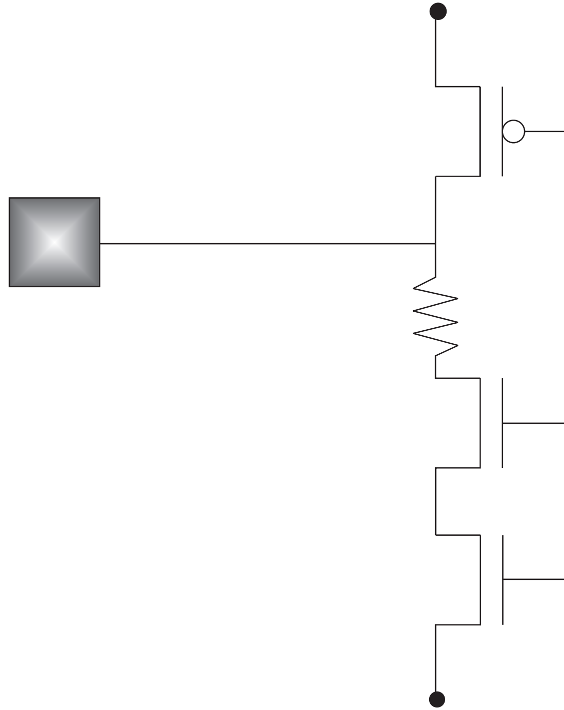

Figure 6.1 Assymetric pull-up/pull-down CMOS OCD with pull-down resistor ballasting

n-channel MOSFETs are sensitive to positive-polarity ESD events. *n*-channel MOSFET pull-down elements undergo MOSFET snapback followed by MOSFET second breakdown during HBM, MM, and TLP ESD events, leading to OCD failure. *p*-channel MOSFETs pull-up elements do not undergo MOSFET snapback or MOSFET second breakdown during positive-polarity ESD events. As a result, the *n*-channnel MOSFET pull-down of an OCD is typically the cause of ESD failure.

To protect the *n*-channel MOSFET pull-down stage, resistor elements are placed in series to prevent MOSFET snapback and MOSFET second breakdown (Figure 6.1). These can be integrated as a single resistor or a set of ballast resistor elements. The ballast resistor elements can be either configured as a bank of resistors or integrated with the *n*-channel MOSFET source and drain regions.

In the case of the *p*-channel MOSFET pull-up element, no resistor elements are used for ESD protection. With the use of a resistor element in series with the *n*-channel MOSFET pull-down without a resistor element in series with the *p*-channel element, the MOSFET driver has an asymmetric switching condition; this can be an undesirable characteristic for the OCD transitions.

From an ESD perspective, the lack of a resistor element in series with the *p*-channel MOSFET pull-up element can lead to an improvement in the ESD robustness of the OCD network [17,33,37]. In the *p*-channel MOSFET pull-up element, the *p*-channel MOSFET drain and the *n*-well region form a parasitic *p–n* diode between the input pad and the power supply. During a positive polarity ESD event, this parasitic element serves as a means to discharge current from the input pad to the power supply rail.

The effectiveness of the use of the *p*-channel MOSFET pull-up to provide ESD protection is a function of the *p*-channel MOSFET design layout and the *n*-well contact design. By the placement of *n*-well contacts regions adjacent to the *p*-channel MOSFET pull-up drain regions, the series resistance formed between the *p*-channel MOSFET drain and the *n*-well contact can be minimized. The effectiveness of the structure is a function of the MOSFET width (e.g., diode perimeter), the *p*-channel MOSFET drain to *n*-well contact spacing, and the *n*-well sheet resistance of the technology. The optimum design is achieved by placement of *n*-well contact regions between the *p*-channel MOSFET drains in a multi-finger *p*-channel MOSFET pull-up element.

In this fashion, the MOSFET pull-up element serves as a p^+/*n*-well diode element between the input pad and the power supply voltage. Given there is an p^+/*n*-well ESD diode between the input pad and the power supply voltage, both the ESD diode and the *p*-channel MOSFET will be in a parallel configuration. Given there is no additional ESD element, the *p*-channel MOSFET pull-up will serve as an ESD element, providing protection for the asymmetric OCD network. Experimental results in semiconductor chips have demonstrated over 10-kV HBM protection levels without failure in 0.35-μm technology in a self-protecting asymmetric driver, which utilized a resistor-ballasted *n*-channel MOSFET pull-down, and an *n*-well contact integrated *p*-channel MOSFET pull-up with no additional ESD device.

The placement of *n*-well contacts can also be integrated between *p*-channel MOSFET pull-up stages where the *p*-channel MOSFET is multiple stages for improved slew rate control. In this case, the *n*-well contacts can be placed between the different stages of the MOSFET pull-up. In this case, the *n*-well contacts were placed between the successive stages of the MOSFET pull-up. Receiver networks with an ESD double-diode element, but without the OCD, demonstrated 4.2-kV HBM levels [17]. The addition of an asymmetric OCD network (e.g., single resistor in series with the *n*-channel MOSFET pull-down, and no resistor element in series with the *p*-channel MOSFET) demonstrated 9.4-kV HBM [17]. The integration of the *n*-well contacts with the *p*-channel pull-up stage improved the HBM ESD results because of the parallel operation of the ESD p^+/*n*-well diode element, and the *p*-channel MOSFET parasitic p^+/*n*-well diode.

The key ESD design practices for asymmetric OCD networks are as follows:

- Resistor ballasts of the *n*-channel MOSFET pull-down, utilizing a single resistor, a resistor bank, a or integrated resistor element.
- Utilize the *p*-channel MOSFET drain to *n*-well parasitic diode by integration of the *n*-well contacts between the *p*-channel MOSFET fingers.
- Minimize the *p*-channel MOSFET parasitic *p*–*n* diode by maximizing the *p*-channel MOSFET width, and decrease the MOSFET drai*n*-to-contact space.

6.1.4 OCD: CMOS Symmetric Pull-Up/Pull-Down

For switching symmetry in OCD networks, resistors are used in series with the *p*-channel MOSFET pull-up and the *n*-channel MOSFET pull-down [37]. In a CMOS OCD network, the *n*-channel MOSFETs are sensitive to positive-polarity ESD events [17,32,33]. *n*-channel MOSFET pull-down elements undergo MOSFET snapback followed by MOSFET second breakdown during HBM, MM, and TLP ESD events, leading to OCD failure. *p*-channel

MOSFETs pull-up elements do not undergo MOSFET snapback or MOSFET second breakdown during positive-polarity ESD events. As a result, the *n*-channnel MOSFET pull-down of an OCD is typically the cause of ESD failure. But, for negative-polarity ESD events, the *p*-channel MOSFET can undergo MOSFET avalanche breakdown, but without a negative resistance transition. ESD failure of *p*-channel MOSFET devices can be observed in negative-polarity ESD events. Additionally, CDM failures can also be evident between the *p*-channel MOSFET pull-up *n*-well and the *p*-channel MOSFET drain. Although these have been observed, it is fairly uncommon in most applications.

The placement of a resistor element in series with the *p*-channel MOSFET pull-up will impact the effectiveness of the *p*-channel MOSFET pull-up in improving the ESD robustness of an OCD. Whereas, the OCD may have achieved better switching symmetry, the ESD results may degrade. One significant result of the series resistor is that the OCD will no longer serve as a self-protecting structure, and will require an ESD network (e.g., ESD double-diode element). Additionally, the *p*-channel MOSFET pull-up will no longer assist in the positive polarity ESD event. To compensate for the ESD robustness degradation, a larger ESD element will be required to provide ESD protection for the symmetric OCD. Figure 6.2 (a) is a circuit schematic of a symmetric series-cascode MOSFET *p*- and *n*-channel MOSFET with resistor ballasting only in series with the *n*-channel pull-down.

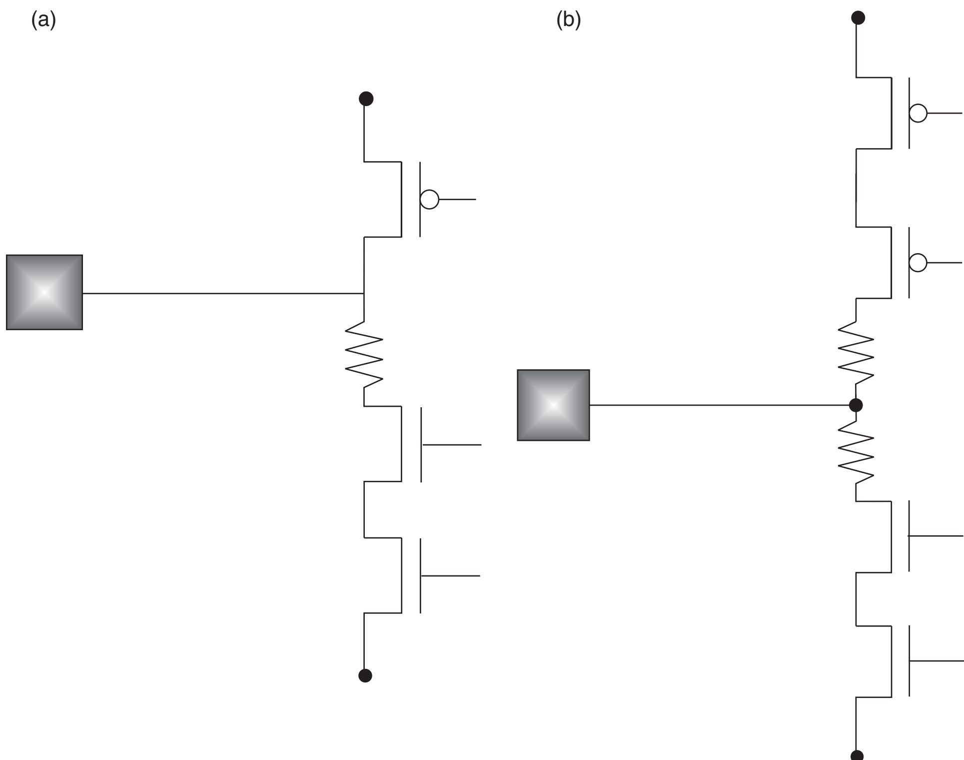

Figure 6.2 (a) CMOS symmetric pull-up/pull-down OCD with pull-down only ballasting; (b) CMOS symmetric pull-up/pull-down OCD with resistor ballasting

Figure 6.2 (b) is a circuit schematic of a symmetric series-cascode MOSFET *p*- and *n*-channel MOSFET with resistor ballasting for both pull-up and pull-down components.

The key ESD design practices for a symmetric OCD networks are as follows:

- Resistor ballasts of the *n*-channel MOSFET pull-down utilizing a single resistor, a resistor bank, or a integrated resistor element.
- Resistor ballasts of the *p*-channel MOSFET pull-up, utilizing a single resistor, a resistor bank, or a integrated resistor element.
- With the ballasting of the *p*-channel MOSFET pull-up, the utilization of the interwoven *n*-well contacts may provide no additional ESD advantage.

6.1.5 OCD: Gunning Transceiver Logic (GTL)

GTL was established by B. Gunning to address a low power standard that allows for low electromagnetic interference at high data rates [1,2]. This is achieved by using a small signal swing to differentiate between a logical "0" and logical "1." The GTL signal swings between 0.4 and 1.2 V with a reference voltage of about 0.8 V; a small deviation of 0.4 V from the reference voltage is required. The low terminating voltage of 1.2 V leads to reduced voltage drops across the resistive elements. GTL has low power dissipation and operates at high frequency. The GTL scheme is established by having the transmission line termination at the far end; in this fashion, it is similar to an "open" drain.

In the GTL OCD implementation, a low-resistance, active "pull-down" element is required. This is typically achieved using a low-resistance single large *n*-channel MOSFET device. In many implementations, a resistor termination is used as a "pull-up" element. The logic levels swing does not undergo "rail-to-rail" transitions but limited about a given dc current level. In some implementations of GTL, an *n*-channel MOSFET "pull-up" is used in the OCD network [17]; this element mimics a resistive load for a "pull-up" transition.

In the "open drain" or a GTL OCD, the *p*-channel MOSFET is not mandatory. In this case, there is no physical element in the OCD to provide protection from positive-polarity human body model (HBM) events and the positive-polarity swing of a machine model (MM) event. Additionally, since a low logic level as well as a low-resistance MOSFET pull-down, is required, a single *n*-channel MOSFET is only used; as a result, the GTL OCD will undergo MOSFET snapback during positive-polarity ESD events.

In some implementations of a GTL OCD, the network contains both an *n*-channel MOSFET pull-up and an *n*-channel MOSFET pull-down element. In this implementation, there are some unique ESD differences compared to a standard CMOS OCD network:

- An *n*-channel MOSFET exists between the input and V_{DD}.
- An *n*-channel MOSFET exists between the input and V_{SS}.
- A series-cascode MOSFET is formed by the GTL network between the V_{DD} and V_{SS} at all input pins.

The interesting feature of this architecture from an ESD perspective is that in a positive-polarity pulse, the *n*-channel MOSFET will undergo MOSFET snapback relative to the V_{DD}

and the V_{SS} power supply [17]. Second, as it discharge to a given power rail, the other parallel pins create a series-cascode MOSFET pair, serving as "pseudo-ESD power clamps" along the chip. The other pins will limit the level of the power rail to the sum of the MOSFET snapback voltages of the pull-up and the pull-down element.

ESD protection can be achieved using the following ESD solutions:

- Low-resistance double-diode networks [31,33].
- MOSFET devices [42].
- Low-voltage trigger Silicon controlled rectifier (LVTSCR) ESD elements.

6.1.6 OCD: High Speed Transceiver Logic (HSTL)

HSTL is a logic standard established for voltage-scalable and technology-independent I/O circuitry [3]. HSTL nominal switching range is from 0 to 1.5 V; this allows for faster I/O response, lower power consumption, and lower sensitivity to electromagnetic interference (EMI). HSTL does not specify the power supply voltage, but is established around a reference voltage condition; this leads to a technology-independent standard. As a result, the HSTL standard is free from the technology generation (which is constrained by MOSFET constant electric field scaling law, dielectric thickness, and power supply condition). The HSTL interface standard is one of the only logic level standards for a single-ended interface at higher speeds; LVTTL, GTL, and SSTL can not achieve the same performance levels. HSTL uses an adjustable voltage reference trip point (V_{REF}) and an output voltage (V_{CCO}). Four classes of HSTL interfaces exist; these are a function of the load and termination conditions. The HSTL standard is valuable for memory applications, such as high-speed static-rams (SRAMs), which require both the noise immunity, low power, small signal swing, and high performance. Since the memory applications are typically at a lower power supply than the control processor unit (CPU), it is a natural solution and I/O standard. In HSTL I/O, matching of the I/O circuit with the termination and load conditions is important.

In the HSTL I/O standard, the ESD protection networks must conform to the impedance matching conditions between the I/O network, the termination and load to avoid transmission line reflections, ringing, and sensitivity to EMIs. Traditional ESD solutions, such as series resistor elements and resistor-ballasted MOSFET networks, interfere with the impedance matching, signal swing, and output drive levels. Additionally, resistor-ballasting elements and resistors do not improve the signal drive but increase the power consumption within the I/O.

In SRAM application, an interface was constructed that has the ability to comply with both the HSTL and GTL standards [17]. In this chip application, two I/O drivers were integrated into a common signal pin. In this implementation, there was a pull-up stage of two parallel *n*-channel MOSFET elements and a pull-up stage of two parallel elements, consisting of a *p*-channel and an *n*-channel MOSFET. In the application, the I/O was able to undergo transition from HSTL to GTL mode, by initiating the pre-drive of the corresponding I/O network.

From an ESD perspective, the integration of both HSTL and GTL standards into a common I/O has some ESD design advantages:

- Increases the effective size of I/O network.
- Provides both a *p*-channel and *n*-channel MOSFET pull-up.
- Increases the size of the *n*-channel pull-down network.

As previously discussed in the GTL application, the integration of a *n*-channel MOFSET pull-up allows for MOSFET snapback between the input and the power supply voltage when the power supply voltage is the ground reference. When the substrate is the ground reference, MOSFET snapback will occur in the two parallel MOSFET pull-down network elements. Additionally, the *p*-channel MOSFET will discharge current to the I/O power supply rail; and the *n*-channel pull-up MOSFET element in the adjacent pins will allow for current flow to the ground reference, when the voltage between I/O power rail and the ground exceeds the sum of the MOSFET snapback voltage of the *n*-channel MOSFET pull-up and pull-down elements.

For ESD protection solutions, the following are possible for this application:

- Diode-based ESD elements.
- Poly-bounded diode ESD elements.
- LVTSCRs

6.1.7 OCD: Stub Series Terminated Logic (SSTL)

SSTL standard was developed to support high-band width DRAM applications. SSTL standards have been developed for a wide range of power supply voltages from 3.3 to 1.8 V [4–6]. SSTL standards have a 3.3, 2.5, and 1.8 V centered power supply level. SSTL3 and SSTL2 are general purpose 3.3 and 2.5 V memory bus standards, respectively. The standards require a push-pull OCD and differential amplifier input buffer, and have two general classes of application. SSTL_18 is a SSTL standard for the 1.8 V centered power supply levels. SSTL3 and SSTL2 Class I and II are single-ended output buffers. SSTL OCD networks are typically a CMOS OCD with a single *p*-channel MOSFET pull-up and a single *n*-channel MOSFET pull-down. As the power supply voltage decreases, and as the performance objectives of the SSTL I/O increase, the ESD solutions have low voltage turn-on and low capacitance.

ESD solutions used for 1.8-V SSTL input have included the following:

- ESD diode to V_{DD} [41].
- Low-voltage RC-triggered silicon controlled rectifier in series with diode string [41].

ESD solution used for 1.8-V SSTL OCD has included the following:

- Low-voltage RC-triggered silicon controlled rectifier in series with diode string [41].

C. H. Chuang and M. D. Ker implemented an ESD input network that included a diode element to the power supply, and a LVTSCR element to the ground plane [41]. In this implementation, the LVTSCR MOSFET gate was triggered by an RC-trigger network whose response was obtained from both the V_{DD} power supply and the signal pad. The LVTSCR

was also in series with a set of two diode elements to prevent early initiation during functional operation. Excellent HBM and MM results were demonstrated into the input circuitry even without power rail implementations.

Additionally, diode-based elements can achieve excellent ESD protection for the SSTL standard. Diode elements will not impact the signal levels, reflections, and transmission characteristics other than in the loading condition at the OCD end. The ESD choice must have a low resistance and must not impact the matching characteristics or the performance of the SSTL OCD network.

6.2 OFF-CHIP DRIVERS: MIXED-VOLTAGE INTERFACE

With MOSFET constant electric field scaling, density and performance objectives continue to scale MOSFETs to smaller physical dimensions. This leads to the lowering of power supply voltages within a system. Within a system or multi-chip environment, the scaling of all segments does not occur concurrently; for example, memory chips are typically designed in the scaled technology, whereas the logic chips are in a prior technology generation. With mixed-voltage applications, new OCD networks need to satisfy this condition [8–16,22–24]. Additionally, the introduction of multiple power supply voltage levels within a chip introduced complexity in the chip architecture, bussing, sequencing, and ESD protection schemes [17–21].

6.3 OFF-CHIP DRIVERS SELF-BIAS WELL OCD NETWORKS

MOSFET constant electric field scaling theory requires to maintain dielectric reliability, the power supply voltage must be scaled with the dielectric thickness. As a result, the high-performance applications and semiconductor chips using advanced lithography tools will have the thinnest dielectric thicknesses and the lowest power supply voltages. In a system environment, mixed-voltage interface OCD networks are required to address the interaction between the older technologies at higher power supply voltages and the microprocessor and memory semiconductor chips at the lower power supply voltages.

Mixed-voltage interface off-chip drivers (MVI-OCDs) were first developed to address the transition from 5 to 3.3 V interfaces between logic and memory. R. Flaker, H. Kalter, K. Gray and R. D. Adams first addressed the MVI OCD with the introduction of the self-bias well network for the *p*-channel MOSFET [10–12]. The pull-down network and pull-down networks consisted of two *n*-channel transistors and two *p*-channel transistors in a series-cascode configuration, respectively. In the pull-down transistor network, the first *n*-channel MOSFET has its gate connected to the internal voltage power supply; this first *n*-channel MOSFET serves as a transmission gate that limits the voltage condition on the *n*-channel MOSFET pull-down element. The unique feature of the implementation was the self-bias well network; a *p*-channel transistor serves a control network that decouples the pull-up network well region from the power supply voltage of the low-voltage semiconductor chip. As the input signal rises above the power supply voltage, the well-bias control network allows the well to undergo a floating state, preventing the pinning of the *n*-well to the V_{DD} power supply voltage. The use of the *n*-well bias network provides a means of decoupling the input signal from the power supply rail.

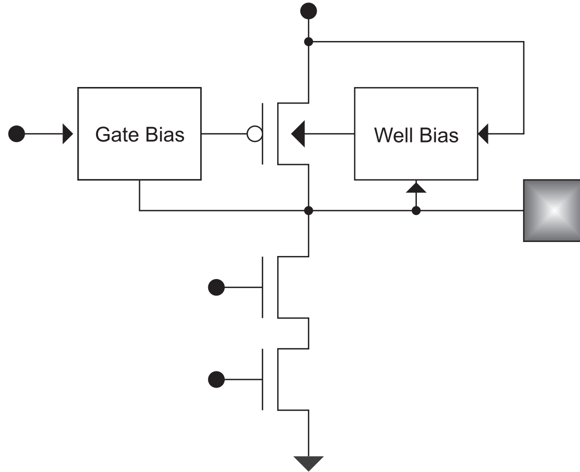

Figure 6.3 Self-bias well OCD networks

This concept was extended to other self-bias well and mixed-voltage interface networks: Austin, Piro, and Stout [13]; Hoffman [14]; Dobberpuhl [15,16]; Shay [22]; Dunning [23]; and Churchhill [24]. In these other implementations, additional transistor elements were added to provide improvements to provide electrical overstress protection of the *p*-channel MOSFET pull-up, improved *n*-well voltage level, and improved *n*-well voltage control. Figures 6.3 shows the basic architecture of a self-bias well. Figure 6.4 (a) and (b) show examples of the implementation of Austin, Piro, and Stout implementation, and the

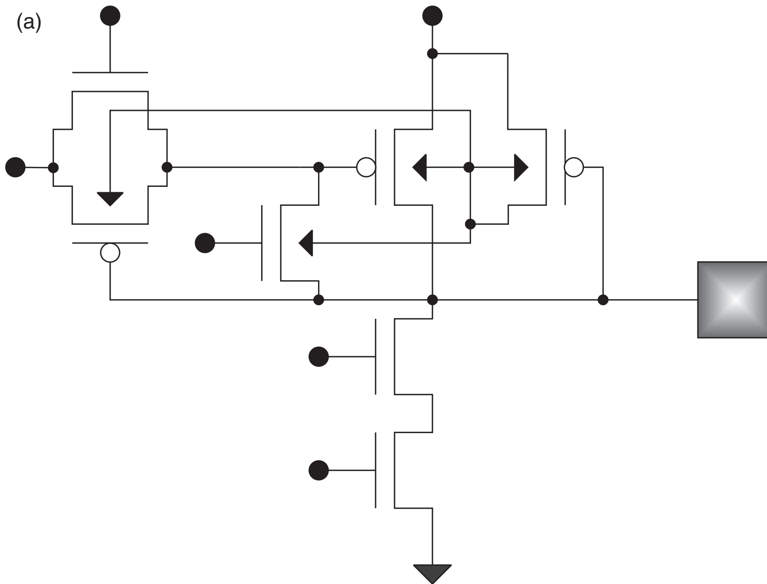

Figure 6.4a Self-bias well OCD networks

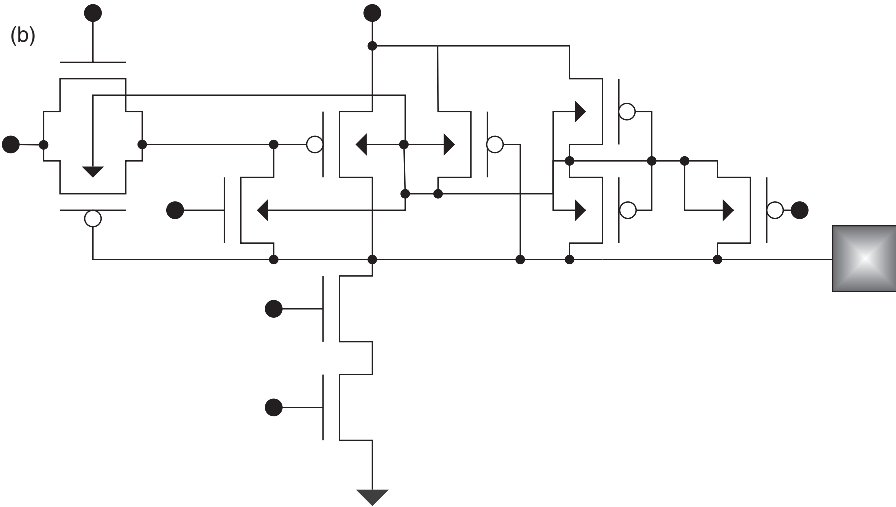

Figure 6.4b Self-bias well OCD networks

Dobberpuhl implementation for a series-cascode self-bias well network respectively. These networks were initiated in a 0.5- and 0.35-μm technology generation.

From the ESD perspective, a first significant observation was the ESD robustness of the upper *p*-channel transistor with the auxiliary *p*-channel self-bias well elements that demonstrated HBM ESD robustness levels of 6–8 kV HBM [17]. With the self-bias well pull-up element, the upper segment of the self-bias well driver demonstrated significantly high HBM ESD robustness due to the decoupling means and electrical overstress protection elements. A second observation noted that although the upper segment was ESD robust, the turn-on voltage was not adequate to provide protection for a non-ballasted *n*-channel pull-down network in the floating well segment. A third observation was that the ESD robustness did not scale with future technology generations. A fourth observation was that without the discharge means to the V_{DD} power supply, the response was dependent on the lateral *pnp* response [17].

These OCD networks were interesting in that they contained circuit concepts, which were useful for ESD design, as follows:

- Electrical decoupling of the *n*-well prevented electrical overstress of the *p*-channel element.
- Electrical decoupling of the *n*-well prevented dielectric gate overstress.
- Inherent robustness was exhibited using the lateral *pnp* of the *p*-channel element with a self-biased *n*-well.

6.3.1 OCD: Self-Bias Well OCD Networks

6.3.2 ESD Protection Networks for Self-Bias Well OCD Networks

In the mixed-voltage interface environment, the self-bias well OCD is utilized to allow the receiving of voltage levels above the native power supply voltage of the low-voltage

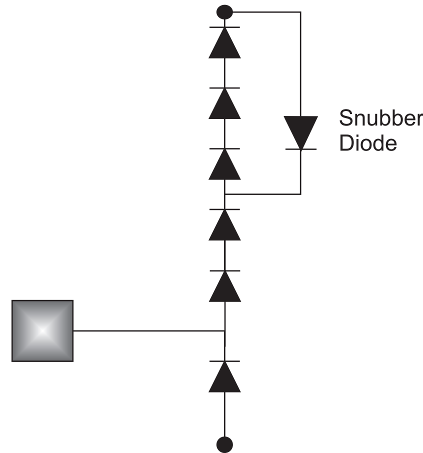

Figure 6.5 Snubber-clamped diode string ESD network

semiconductor chip. ESD input protection solutions consist of three different solutions [17–21]:

- Snubber-clamped ESD diode string network [19–21].
- ESD diode string with a second power supply pin added after the first diode.
- Self-biased well ESD protection network [17].

The first implementation utilized a Snubber-clamped ESD diode string [19–21]. As discussed in the prior section, this consisted of a five-diode string between input and the V_{DD} power supply pad (Figure 6.5). With the Snubber-diode element, the Darlington amplification was eliminated [19–21, 34–36, 39]. But, in high bipolar current gain semiconductor processes, the vertical *pnp* effect leads to an *I–V* characteristic shift approximately 1 V lower than the ideal characteristic; this leads to a sub-''turn-on'' leakage characteristic level, which is not acceptable near the higher temperature and voltage specification (this was demonstrated by G. Gerosa and S. Voldman in a microprocessor CPU with a retrograde well technology process [19–21]). ESD HBM levels of 8 kV were achieved in this implementation.

A second ESD circuit used for mixed voltage applications was the self-bias well ESD protection network developed by S. Voldman [17]; this ESD circuit incorporated the self-bias well concept of R. Flaker [10,11], and utilized a lateral pnp element for ESD current discharge. Figure 6.6 (a) and (b) show the network circuit schematic and layout, respectively. This network achieved excellent results when utilized with a mixed-voltage interface self-bias well OCD network (this was demonstrated by Gerosa and Voldman in a second microprocessor CPU with a diffused well technology process). HBM ESD protection levels over 4 kV were achieved in this implementation.

A third ESD input strategy was to add a extra power pin to the lower voltage chip application; an extra power pin was added after the cathode of the first diode of the ESD

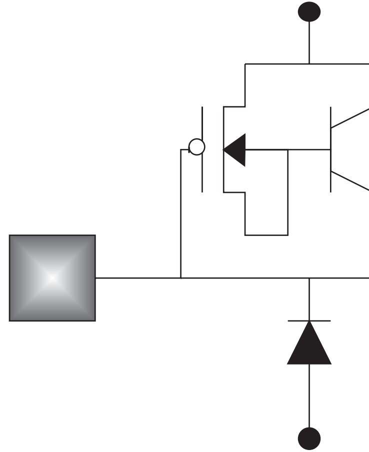

Figure 6.6a Self-biased well ESD network schematic

diode string, and the rest of the diode elements were then between the first higher voltage power pin and the native power supply voltage. As a result, a Snubber-diode was not needed (this was incorporated by A. Correale and S. Voldman into an embedded controller architecture). ESD HBM levels of over 5 kV were achieved in this implementation.

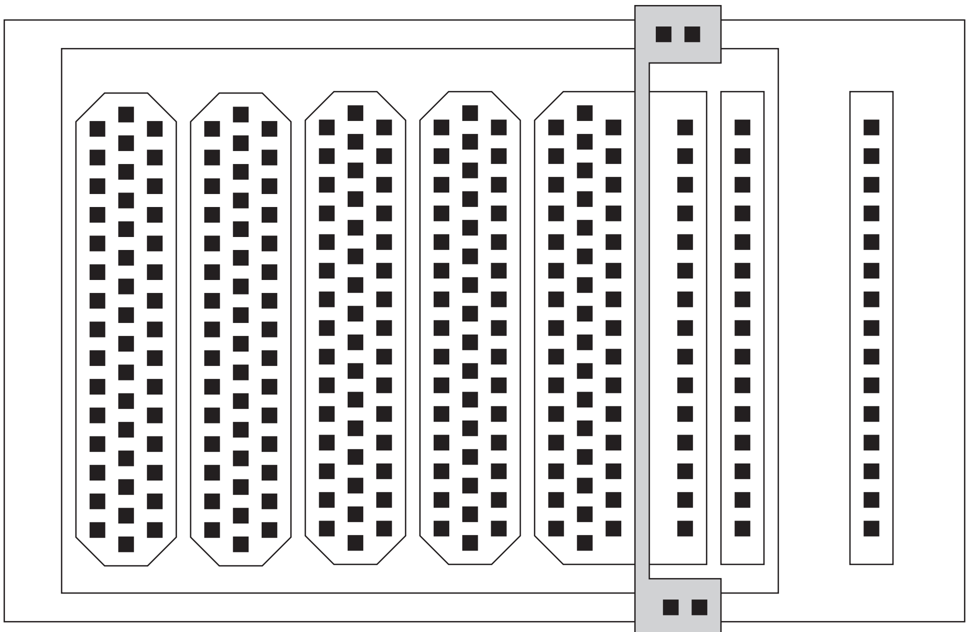

Figure 6.6b Self-biased well ESD network layout

6.4 OFF-CHIP DRIVERS: PROGRAMMABLE IMPEDANCE (PIMP) OCD NETWORKS

PIMP OCD networks are used as a mean to match impedances with external loads [26–28]. To avoid ringing, an output OCD can be set with a given voltage level, drive strength, and impedance that matche the I/O device and transmission line. Low I/O drive strength need an OCD with a high impedance, and a high I/O drive strength will require a low-impedance OCD. Since the load can vary, it is desirable to have an OCD, which can be modified according to the required load needed to be driven. In semiconductor manufacturing, process variations also can lead to variation in the output impedance of an OCD element. Additionally, power supply and temperature variations can modify the OCD impedance. Hence an OCD, which can be self-tracking and provide matching with a transmission line and an external load, is important for many semiconductor chip and system applications.

T. J. Gabara and S. C. Knauer addressed the problem by providing an OCD network with a digitally adjustable resistor element [26]. In this method, a variable resistor external to the OCD allowed for a fixed OCD design but addressed the impedance by providing a variable matching resistor element that was digitally adjustable. A user may change the external resistor of the driver to reflect the voltage/impedance, needed to drive an external load element. The OCD has an impedance that matches the transmission line; the OCD transistor width is adjusted by digital methods. In this concept of Gabara and Knauer, the overall impedance of the OCD circuit is obtained through the circuit's counter circuit networks that provide a digital ‘‘count.’’ Digital counter circuits are used to ‘‘lock’’ in that final count value. From an ESD perspective, as the resistor element increased in physical size, the OCD was buffered from the input pad, reducing the risk of ESD damage. In this implementation, the resistor element is modified.

In another method of providing a PIMP OCD network, the impedance of the OCD is modified using digital ‘‘counters’’ that modulate the size of the *p*- and *n*-channel MOSFET driven segments [27,28]. By using the MOSFET OCD, the amount of power consumption, predictability, and accuracy is better obtained. H. Pilo, F. Towler, M. J. Schneiderwind, and S. Lamphier provided an output driver circuit that included the following [27]:

- An external impedance element.
- Voltage comparator circuit.
- Control logic circuit.
- An evaluate circuit.
- OCD output element.

Figure 6.7 (a) shows the PIMP OCD network. Voltage from the ‘‘external resistance device’’ is compared with voltage created from an evaluate circuit by the voltage comparator; the control logic digitally adjusts the ‘‘count’’ until they are equated. After the ‘‘counting’’ process is complete by the control networks, the OCD MOSFET is increased or decreased in size to achieve the appropriate drive impedance [27].

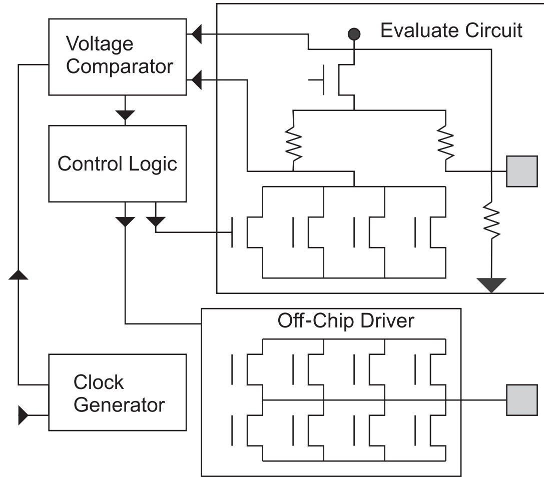

Figure 6.7a PIMP driver network

In this implementation, there are unique ESD design issues, as follows:

- Single MOSFET element: The pull-down *n*-channel MOSFET and pull-up MOSFET are not cascaded but single elements.
- Series resistor elements: No resistor elements can be placed in front of the OCD MOSFET for ESD protection.
- MOSFET design and layout: The MOSFET layout has a fixed channel length for all MOSFET finger segment but variable MOSFET finger width.
- Ballasting elements: Resistor ballasting elements are not acceptable in the MOSFET fingers since they are matched with the adjustable counter network.

First, since only a single MOSFET element is utilized, MOSFET snapback voltage is a function of the channel length of a single MOSFET element. This provides a low turn-on voltage.

Second, since matching is required between the external load, the transmission line, and the internal MOSFET driver, no series resistance elements are acceptable. This prevents the buffering of the OCD MOSFET from ESD current.

Third, the width of the OCD MOSFET output device size is modified by adjusting the number of MOSFET fingers that are driven, which is established by the counting networks. Figure 6.7(b) shows an example of the programmable impedance driver MOSFET output device. In the physical layout, the width of the different fingers are of different widths for each finger grouping. This introduces an interesting issue: the asymmetry of the MOSFET fingers in the width leads to non-uniform bussing considerations and distribution issues during MOSFET snapback and MOSFET second breakdown. Experimental work by Pilo and Voldman showed that in this implementation, the smallest width fingers fail first, starting from the smallest width fingers, to the largest width fingers.

Fourth, the MOSFET finger elements must be of the same physical design as the adjustable counter structures. As a result, resistor-ballasting cannot be integrated into the MOSFET physical design of the output device unless ‘‘mirrored’’ in the adjustable counter network.

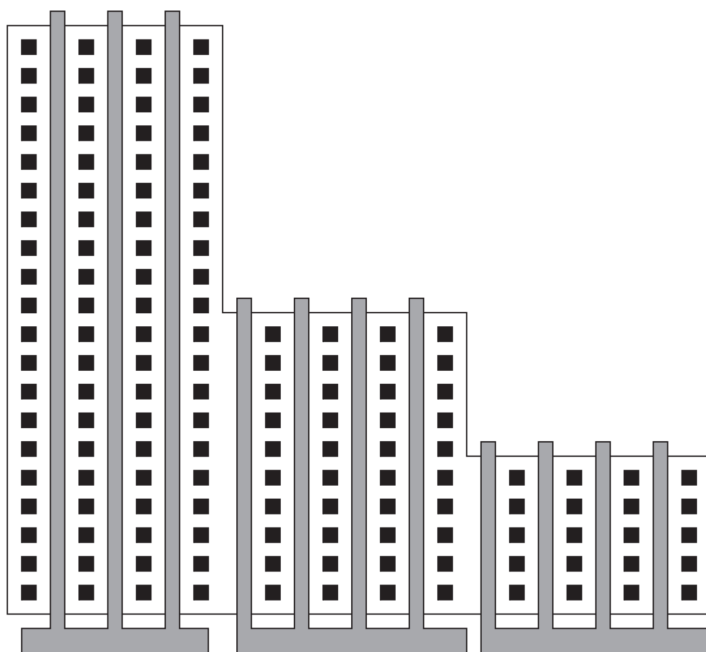

Figure 6.7b MOSFET layout in a PIMP driver network

With these three issues, it is found that this is a difficult OCD to provide good ESD protection. Solutions for improvement are as follows:

- Introduce ballasting elements in the adjustable counter network and the OCD elements with each finger element.
- Utilize low-resistance ESD networks.
- Utilize low-trigger voltage ESD power clamps.

Programmable impedance OCDs are important, as the need to efficient power transfer from driver to load and improved *dI/dt* control increases. Other circuit networks also exist that achieve the same objective. Hansen and Pilo developed another method using analog biases to provide the matching between the output and the load impedance; this was achieved using a digitally controlled current mirror network [28]. PIMP OCDs will continue to provide challenges for ESD protection, as new implementation are developed.

6.4.1 OCD: Programmable Impedance (PIMP) OCD Networks

6.4.2 ESD Input Protection Networks for PIMP OCDs

ESD input protection networks for PIMP circuits is limited as a result of the nature of this circuit. With the constraints of no series resistance element, a OCD final stage of a

single MOSFET pull-down, and the minimum-channel length and variable width MOSFET layout, PIMP circuits, the ESD input protection network must have the following features:

- An ESD trigger voltage below the minimum channel length MOSFET snapback voltage.
- A low series resistance.

To provide ESD protection for this application, the most successful solution was achieved using very low-series resistance ESD double-diode networks on the input pad nodes and RC-triggered MOSFET power clamps. Additionally, a low-resistance power bus was established using the stacking of multiple metal levels in the perimeter I/O design. In the perimeter I/O architecture, the metal bus resistance could compromise the ESD element and the RC-triggered power clamp. As a result, wide metal busses and the use of multiple stacked metal lines were "stitched" to lower the bus resistance.

6.5 OFF-CHIP DRIVERS: UNIVERSAL OCDs

With the wide variety of logic levels of receiving and transmitting signal, the concept of a single receiver or OCD circuit that can interface without a new circuit but employs a suitable means of interfacing has significant advantages, where the system environment is either reconfigurable dynamically or for a wide range of applications. The desire has a "universal interface"; that is, to establish a "variable voltage CMOS OCD" and receiver interface that can send and receive signals at different logic levels. Additionally, a second objective is to have a constant output impedance independent of the output voltage. This concept of a "universal OCD" would avoid the constant redesign of OCDs with each change in technology logic levels, as well as be able to interface with higher or lower power supply environments. P. Coteus, D. Dreps, G. Kopcsay, H. Bickford, C. Chang, and R. Dennard pursued the concept of the universal driver, where the different levels states were established using an integrated three-input multiplexor (MUX) [29,30]. In this fashion, the logic levels of receiving and transmitting were achievable with a single OCD circuit. To achieve a constant output impedance, different series resistance elements were used in series with the OCD output devices.

From an ESD perspective, the universal OCD produces a unique challenge as a result of the variable voltage levels. The universal OCD network must establish a constant impedance, and hence the resistor elements in the different segments of the network must be set by the different segment requirements. ESD protection can be established using the following circuit concepts:

- ESD double-diode network.
- Silicon controlled rectifier (SCR).

With the changing voltage levels, it is not possible to use a MOSFET ESD implementation, unless the MOSFET element exceeds the maximum MOSFET gate dielectric condition.

6.6 OFF-CHIP DRIVERS: GATE-ARRAY OCD DESIGN

6.6.1 Gate-Array OCD ESD Design Practices

In gate-array OCD environment, the design methodology and practices are distinct from a non-gate array environment. The gate-array design methodology provides opportunities and advantages for ESD design.

6.6.2 Gate-Array OCD Design: Usage of Unused Elements

ESD design practices can be implemented into gate-array OCD design to utilize segments of the OCD design book for ESD protection. In OCD design, MOSFET pull-up and pull-down stages are modified in drive strength by changing the elements, which are driven by the pre-drive circuitry or modification of the gate connections.

An example, given a MOSFET pull-down network, where a fixed MOSFET width is contained within an OCD design book, the MOSFET gate connections can be modified so that segments of the MOSFETs are used for the OCD application. For example, given a MOSFET of width, *W*, where there are *N* MOSFET gate fingers, in a given application, only *M* fingers are used for the circuit application; this leaves *N-M* fingers unused in the OCD design book. In the network, the *M* gate fingers are electrically connected to the pre-drive circuitry, and the *N-M* MOSFET gate fingers are electrically disconnected from the pre-drive circuitry.

An ESD design practice in ESD OCD design is to utilize the unused portions of the MOSFET for ESD protection. A common ESD design practices are as follows:

- Substrate grounding unused MOSFET elements: Electrically ground the *N-M* MOSFET gate fingers to the substrate.
- Dummy pre-drive element for unused MOSFET elements: Electrically connect the *N-M* MOSFET gate fingers to a "dummy circuit."
- Input gate-coupled network for unused MOSFET elements: A gate-coupled network is electrically connected to the input pad node to activate the unused segments of the MOSFET pull-down element.

In the first case, the unused MOSFET gate elements are electrically grounded (Figure 6.8). In this fashion, as the input node voltage approaches the MOSFET snapback voltage, the unused portions of the MOSFET *n*-channel pull-down element serve as the "grounded-gate MOSFET" ESD protection elements. As the pad voltage rises, the MOSFET drain voltage increases, until the MOSFET undergoes MOSFET snapback. The *N-M* unused MOSFET gate structures begin to conduct current to the MOSFET source, discharging the ESD current. The MOSFET gate fingers driven by the OCD pre-driver network do not undergo MOSFET snapback at the same voltage level. As the voltage continues to increase, the MOSFET fingers connected to the pre-drive network will also undergo MOSFET snapback. Note in this implementations, the *N-M* fingers, which are grounded, will undergo snapback at a lower voltage. This has the disadvantage that the

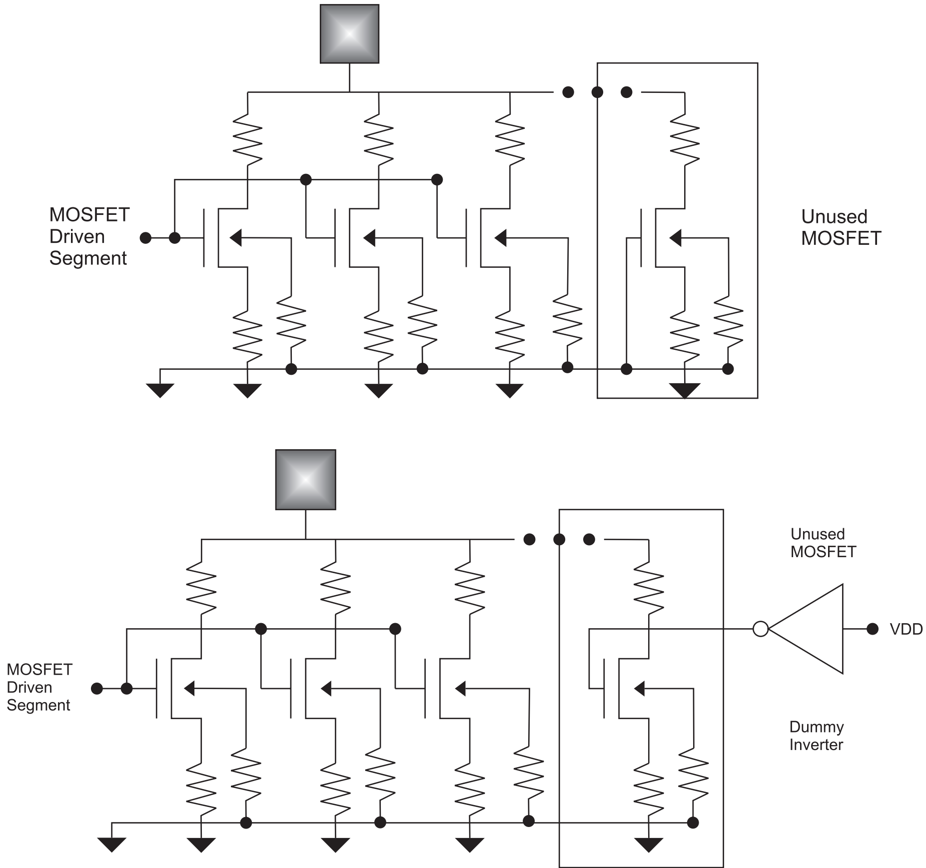

Figure 6.8 (a) Gate-array MOSFET with grounded-gate unused fingers for ESD protection (b) gate-array MOSFET with unused fingers connected to dummy pre-drive network

"used" portion of the MOSFET pull-down does not turn on at the same condition, making the ESD results a function of the number of fingers that are used or unused.

In a second case, the unused portions are coupled to the input pad. In this fashion, the unused portions can be triggered using the following methods:

- Gate-coupling.
- RC-coupling.
- Gate- and body-coupling.

Using these methods, the unused portions are utilized for ESD protection and to provide the earliest turn-on possible, and not for addressing the size of the "used" segment. This will be successful, given that a minimum number of fingers are defined (e.g., *N-M* fingers are above some design limit to guarantee the "smallest" number utilized for ESD protection).

6.6.3 Gate Array OCD Design: Impedance Matching of Unused Elements

An ESD design practice in ESD OCD design is to utilize the unused portions of the MOSFET for ESD protection. Some ESD design practices are as follows:

- Impedance match the used and unused MOSFET elements: Electrically connect the *N-M* MOSFET gate fingers to a dummy circuit that mimics the impedance of the "used" portions of the MOSFET.
- Dummy pre-drive element for unused MOSFET elements: Electrically connect the *N-M* MOSFET gate fingers to a "dummy circuit."

A method that allows for an improvement is to provide impedance matching of the MOSFET gate fingers of the used and unused segments of a multi-finger MOSFET structure in an OCD circuit. This can be done with a simple network or a more complex network that mimics the pre-driver network.

In this ESD design practice, the unused MOSFET gates are not grounded but electrically connected to an auxiliary circuit or a "dummy pre-drive network." In the prior discussion, it was noted that the driven and the undriven segments of the MOSFET pull-down have different electrical drain-to-gate voltage conditions, leading to different MOSFET snapback conditions. A dummy "pre-drive" network can mimic the impedance condition on the undriven *N-M* MOSFET gate segments (Figure 6.8(b)). This can be done by using the following:

- A dummy inverter network is connected to the unused MOSFET gate segments. The input of the receiver inverter is set at "1" to set the unused MOSFET gate segments to a "0" state.
- A dummy pre-drive network sets the unused portions into a "tri-state" mode.

In this method, the objective is to have the impedance state of the used and the unused MOSFETs to undergo MOSFET snapback at the same voltage level, utilizing the full *N* fingers concurrently; whereas in the first method, the ESD results will vary according to the number of unused versus used MOSFET fingers; this methodology aims at fully utilizing all elements at the same time, making it also gate-array implementation-independent.

6.6.4 OCD ESD Design: Power Rails Over Multi-Finger MOSFETs

The placement of the power rails and electrical connections influences the ESD robustness of a multi-finger MOSFET due to thermal heating of the inter-connect and inter-level dielectric (ILD) insulators. In a single pull-down or cascoded series MOSFET structure, the current flows from the pad to the V_{SS} ground rail. The ESD current that flows to the V_{SS} ground rail is then redistributed through the V_{SS} ground network or to the local V_{SS} pad.

Experimental results showed that when the multi-finger MOSFET pull-down is electrically connected to a V_{SS} ground rail that exists on a second metal level (M2), the

MOSFET second breakdown occurs under the V_{SS} metal bus. As the current flows from the MOSFET to the local V_{SS} bus connections, the heating of the metal and the surrounding insulating regions influences the underlying MOSFET structure. The failure of the MOSFET fingers occurs directly under the metal bus as opposed to the location anticipated by voltage distribution of a parallel- or anti-parallel configured multi-finger MOSFET. The influence of the local heating is a function of the ESD pulse width and current magnitude, the vertical spacing of the metal bus to the MOSFET silicon surface, the type of the ILD material, and the interconnect metallurgy. The local self-heating within the metal bus is a function of the metal width, as well as the metal via connections. In the design, the local heating can be evaluated. The ESD design practices to avoid this issue are as follows:

- Avoid passing the power and ground bus directly over the multi-finger MOSFET pull-down network, where the power bus or ground is within one to two metal levels of the MOSFET metal connections.
- Use a large number of metal vias and adequate metal bus width to distribute the current from the MOSFET to the power rail.

6.7 OFF-CHIP DRIVERS: GATE-MODULATED NETWORKS

6.7.1 OCD Gate-Modulated MOSFET ESD Network

An important ESD concept in ESD networks is the role of the gate potential during ESD events. D. Krakauer, K. Mistry, and H. Partovi in the analysis of operation of a MOSFET ESD protection network discovered some unusual response of the OCD network and the ESD devices [42]. Using a simple grounded-gate MOSFET network to protect an OCD network, it was found that the ESD current that discharges to the I/O power rail initiated the pre-drive circuitry attached to the pre-drive network (e.g., the output stage and the OCD pre-drive were connected to the external power supply voltage). The initiation of ESD current flow to the pre-drive network increased the gate voltage on the output drive stage; this in turn led to turn-on of the MOSFET pull-down transistor prior to the turn-on of the grounded-gate MOSFET ESD element. Krakauer, Mistry, and Partovi utilized this concept (as shown in Figure 6.9 (a,b)) to develop a ‘‘gate-modulated ESD network’’ consisting of the following:

- A discharge MOSFET whose drain is connected to the pad, and whose source is grounded.
- An inverter network whose *p*-channel MOSFET source is connected to the input signal pad, and whose inverter output is connected to the discharge MOSFET gate.
- An ‘‘ESD reference’’ signal pad that establishes a logic state for the inverter network.
- An *n*-channel limiter MOSFET whose gate is connected to a resistor element, and whose drain is connected to the discharge MOSFET gate.
- A resistor connected between the signal pad and the gate-voltage limiter element.

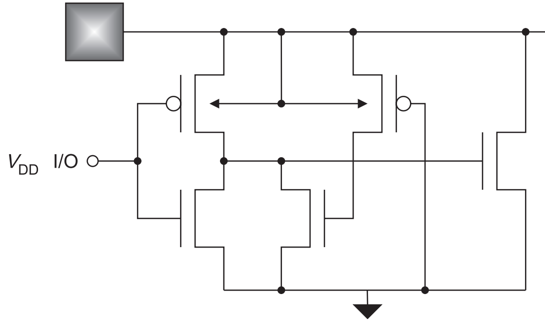

Figure 6.9 (a) Gate modulated OCD network

The important ESD design concept in this network is the following:

- ESD discharge current can activate the pre-drive circuitry of an OCD if the pre-drive is connected to the external I/O power rail.
- Gate modulation of the OCD pull-down can play a role in the ''current sharing'' with a parallel MOSFET-based ESD element.
- The OCD pull-down can introduce ''current robbing'' during an ESD event if the MOSFET pull-down gate voltage state, coupling, or impedance to the ground plane is favored over the MOSFET ESD element.
- Utilizing gate-modulation networks, a ''gate-coupled'' ESD MOSFET can provide a good ESD protection.

6.7.2 OCD Simplified Gate-Modulated Network

From the prior implementation, Krakauer, Mistry, and H. Partovi utilized this concept (as shown in Figure 6.9 (b)) to develop a ''simplified gate-modulated ESD network'' consisting of the following [42]:

- A discharge MOSFET whose drain is connected to the pad, and whose source is grounded.

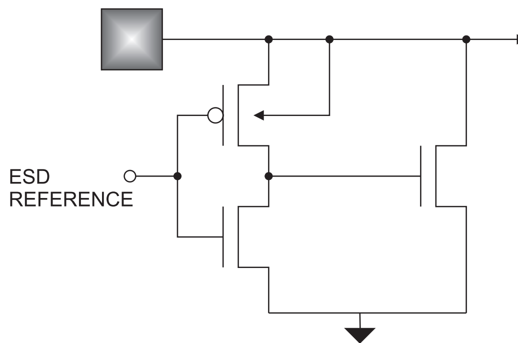

Figure 6.9 (b) simplified gate modulated OCD network

- An inverter network whose *p*-channel MOSFET source is connected to the input signal pad, and whose inverter output is connected to the discharge MOSFET gate.
- An "ESD reference" signal pad that establishes a logic state for the inverter network.

The advantage of this ESD design concept is the ability to match with the technology generation, and the ability to simulate and model the circuit responses. The disadvantage of this ESD methodology is that it must be tuned for each I/O, each design, and each technology generation.

6.8 OFF-CHIP DRIVER ESD DESIGN: INTEGRATION OF COUPLING AND BALLASTING TECHNIQUES

A fundamental ESD concept in OCD networks is that to provide good current uniformity in a multi-finger MOSFET structure. With utilizing ballasting, coupling, and biasing techniques, the MOSFET second breakdown voltage, Vt_2, can exceeds the MOSFET first breakdown voltage, Vt_1, leading to MOSFET current uniformity in a multi-finger OCD network. Multi-finger MOSFET ESD design utilizes both coupling and ballasting concepts to improve the current uniformity during high-current events in the OCD networks [44]. Coupling and ballasting techniques can be integrated together to provide improved ESD robustness in MOSFETs. Some of the implementation can be utilized for OCDs but others are only suitable for "unused gate array" MOSFET segments, which are undriven by the pre-drive circuitry. The following implementations can be used for "unused MOSFET gate array":

- Substrate grounded-gate (with gate resistor) resistor-ballasted multi-finger MOSFET.
- Substrate grounded-gate (with gate resistor and capacitor element) resistor-ballasted multi-finger MOSFET.
- Soft substrate grounded-gate resistor-ballasted multi-finger MOSFET.
- Domino source-to-gate coupled resistor-ballasted multi-finger MOSFET.

The following OCD ESD design methodologies can be used in OCD and driven by the pre-drive circuitry:

- MOSFET source-initiated gate-bootstrapped resistor-ballasted multi-finger MOSFET with MOSFET.
- MOSFET source-initiated gate-bootstrapped resistor-ballasted multi-finger MOSFET with diode.

6.8.1 Ballasting and Coupling

6.8.2 MOSFET Source-Initiated Gate-Bootstrapped Resistor-Ballasted Multi-Finger MOSFET With Diode

MOSFET source-initiated gate coupling can be implemented in a fashion, where one MOSFET source initiates a common MOSFET gate electrode. Utilizing a MOSFET source

with two series resistor ballast elements and a center tap, MOSFET gate coupling can be initiated through a diode element. In the case that a MOSFET bootstrap element is used, this bootstrap element requires additional space as well as impacting capacitance loading on the signal pad. With the utilization of a diode element between the MOSFET source and the MOSFET gate electrode, no additional loading capacitance occurs on the signal pad, and less area can be utilized. In this network, the first conducting MOSFET finger source senses the ESD event, leading to a rise in the MOSFET source potential. This first MOSFET finger source rises. The electrical potential of the MOSFET source resistor divider leads to an increase in the anode of the bootstrap *p–n* diode element. The bootstrap *p–n* diode element charges the MOSFET gate electrode when the *p–n* diode element becomes forward active. When the MOSFET gate electrode rises, MOSFET channel conduction occurs in all MOSFET finger elements providing uniform current flow. The advantages of this method allow for electrical connection of the MOSFET gate to a pre-driver network for utilization in OCD networks or in other circuits. This method also prevents the additional loading on the signal node compared to other bootstrap methods. A disadvantage of this method is that the diode elements must charge the complete MOSFET gate electrode. As a result, this method may be limited by the diode current drive, and the number of MOSFET fingers that can be driven by the bootstrap element (Figure 6.10).

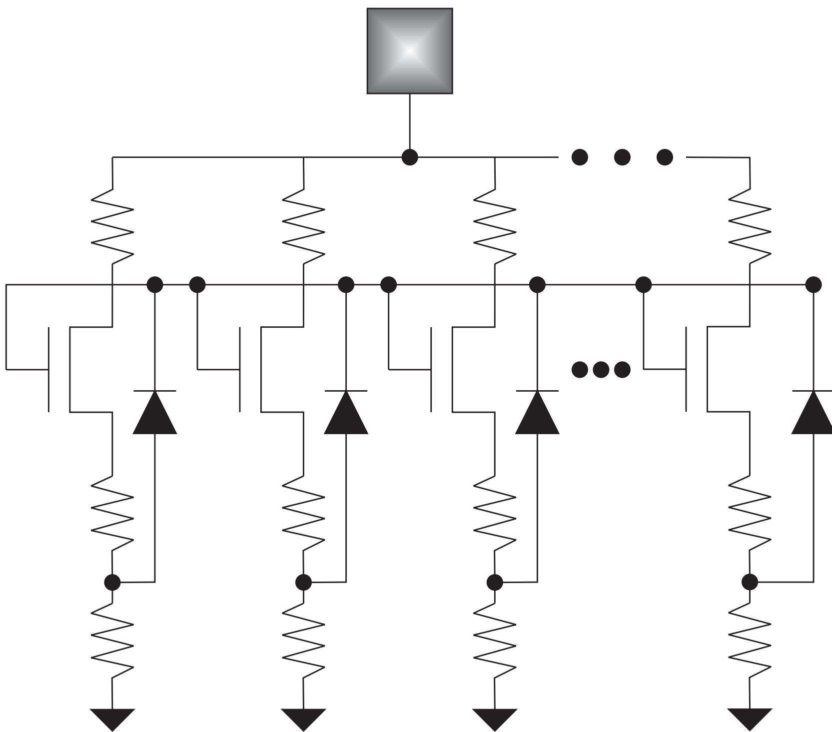

Figure 6.10 MOSFET source-initiated gate-bootstrapped resistor-ballasted multi-finger MOSFET with diode Bootstrap element

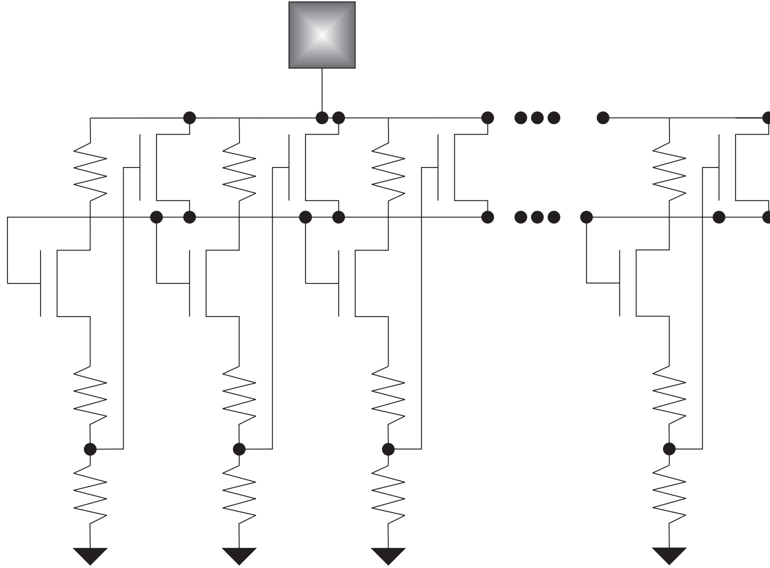

Figure 6.11 MOSFET source-initiated gate-bootstrapped resistor-ballasted multi-finger MOSFET with MOSFET

6.8.3 MOSFET Source-Initiated Gate-Bootstrapped Resistor-Ballasted Multi-Finger MOSFET With MOSFET

MOSFET source-initiated gate coupling can be initiated to individual MOSFET fingers sequentially or all MOSFET fingers simultaneously. In an domino style implementation, the MOSFET fingers are gate-coupled in a sequential manner (Figure 6.11). In the soft-grounded gate MOSFET, all fingers are initiated simultaneously. In the case of the individual sequential coupling technique, the response of the individual gate structures will have a faster RC time response for each individual fingers. But the disadvantage is the electrical disconnection of the MOSFET gate structure for utilization as a MOSFET off-chip pull-down. Hence, these other implementations may be only implemented in a ‘‘gate-array’’ OCD design environment. But in this implementation, it can be integrated into a MOSFET pull-down network of an OCD.

MOSFET source-initiated gate coupling can be implemented in a fashion, where one MOSFET source initiates a common MOSFET gate electrode; the MOSFET source is electrically connected to two series resistor elements. The center node of the two resistor elements is electrically connected to initiate MOSFET gate coupling element. With a common gate electrode, the MOSFET source connection cannot be electrically connected to the MOSFET gate. Hence, an additional bootstrap MOSFET is placed between the signal pad and the MOSFET gate electrode.

The bootstrap MOSFET drain is connected to the signal pad, and its source is connected to the primary MOSFET gate electrode. The MOSFET source resistor center-tap is electrically connected to the gate of the bootstrap MOSFET.

In this network, the first conducting MOSFET finger source senses the ESD event, leading to a rise in the MOSFET source potential. This first MOSFET finger source rises. The

electrical potential of the MOSFET source resistor divider leads to an increase in the gate of the corresponding bootstrap MOSFET element. The bootstrap MOSFET undergoes MOSFET conduction when the MOSFET threshold voltage is exceeded. The bootstrap MOSFET element charges up the MOSFET gate electrode, leading to MOSFET conduction in the other adjacent MOSFET fingers, which were not undergoing MOSFET snapback. The advantages of this method allows for electrical connection of the primary MOSFET gate to a pre-driver network for utilization in OCD networks or other circuits. The disadvantage of this structure is the need for an additional resistor and MOSFET for every segmentation of finger elements. This adds extra capacitance loading and space impact.

6.8.4 Gate-Coupled Domino Resistor-Ballasted MOSFET

As discussed on the chapter on multi-finger MOSFETs, Mergens *et al*. [44] introduced a ‘‘domino’’ method in a multi-finger MOSFET structure by electrically connecting the MOSFET gate of a second MOSFET finger to the MOSFET source of a first MOSFET finger (Figure 6.12). In this domino source-to-gate coupled resistor-ballasted multi-finger MOSFET, the MOSFET source ballast resistor is split into a first and second resistor element. An electrical connection is established between the two resistor elements and electrically connected to the MOSFET gate of a second finger. This is initiated *ad infinitum* to all the finger elements. The ‘‘*n*th finger’’ MOSFET source connection is electrically connected to the MOSFET gate of the first MOSFET finger. In this fashion, the

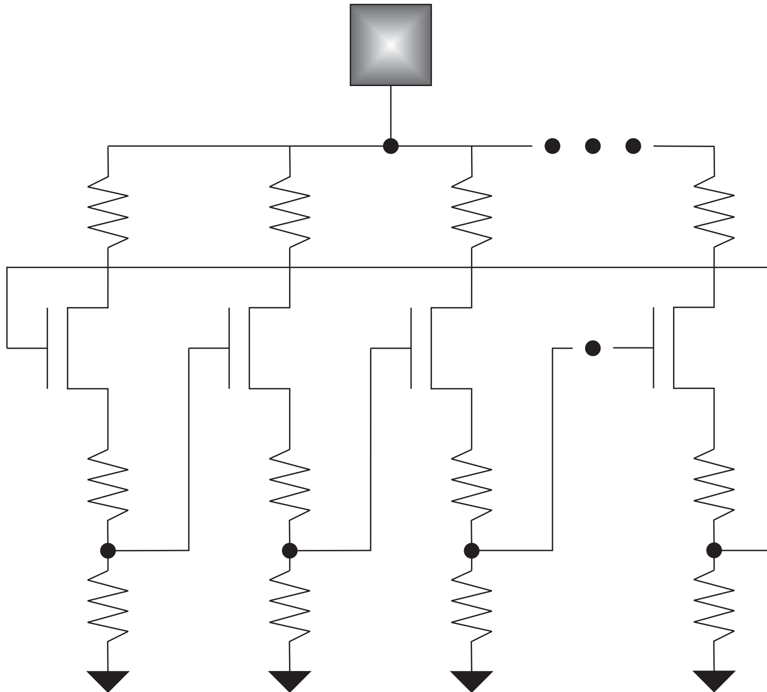

Figure 6.12 Domino source-to-gate coupled resistor-ballasted multi-finger MOSFET

domino-triggering initiation can occur in any MOSFET finger in the structure. As the signal pad increases, the electrical potential of all the MOSFET drain structure increases. As the MOSFET drain potential increases, avalanche multiplication occurs. Eventually, one of the MOSFET fingers undergoes MOSFET snapback. As the electrical conduction occurs in the MOSFET finger, the current flows through the MOSFET source resistor elements. The two resistor elements form a voltage resistor divider. As the voltage increases, the MOSFET gate structure potential increases. As the MOSFET gate potential increases, adjacent MOSFET finger begins to conduct MOSFET source-to-drain current through the MOSFET channel region. As the second MOSFET finger conducts current through its own source, the electrical potential of the MOSFET gate of the third MOSFET finger increases. This continues in this fashion, until the ‘‘*n*th’’ MOSFET finger. As the ‘‘*n*th’’ MOSFET finger undergoes MOSFET conduction, the MOSFET gate of the first MOSFET finger that underwent MOSFET snapback will have its MOSFET gate potential increase, leading to MOSFET channel conduction instead of a MOSFET snapback state.

In this implementation, it was pointed out that the nature of the conduction and response in the ‘‘Domino’’ multi-finger MOSFET is different from other multi-finger MOSFETs, in the following ways:

- The response of the network is current-driven (as opposed to frequency-driven).
- The response is ‘‘static’’ phenomena not ‘‘dynamic.’’
- The time response of the network is associated with the MOSFET gate delay time and the number of MOSFET finger stages.
- The operation time is ‘‘auto-timed’’ and acts only during a fixed time interval, associated with the RC response of the successive stages, the MOSFET gate delay, and the number of successive stages.

In this implementation, the MOSFET current and the models are predictive models, as well as the circuit response. This implementation can also be integrated into a MOSFET gate array environment where the gate electrodes are separated from the pre-drive signal. As discussed in the prior section on gate array implementation, this network can be integrated into the unused MOSFET gate fingers of an OCD network.

6.9 OFF-CHIP DRIVER ESD DESIGN: SUBSTRATE-MODULATED RESISTOR-BALLASTED MOSFET

In a MOSFET OCD network, the injection phenomenon into the substrate can influence the MOSFET substrate potential and the MOSFET gate electrode. The local potential of the MOSFET structure can be modulated by injection phenomenon due to MOSFET drain. Additionally, the MOSFET gate and substrate potential can be modulated by external source elements or circuits. As the potential locally increases under a MOSFET structure, a MOSFET reverse-body effect leads to a lower threshold voltage. The lower threshold voltage leads to an early turn-on of the MOSFET structure. This manifests itself in achieving MOSFET current uniformity in multi-finger structures, a lower turn-on voltage, and an

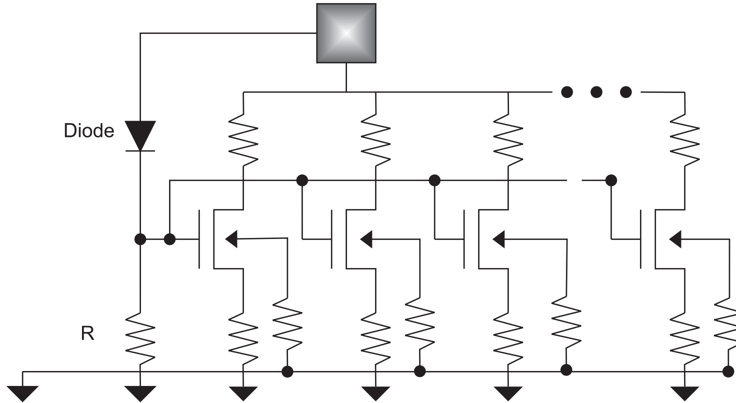

Figure 6.13 *p–n* diode driven resistor-ballasted OCD MOSFET

increase in MOSFET current drive. C. Duvvury demonstrated different techniques to modulate the substrate and the gate electrodes via injection phenomenon or support circuitry. ESD design practices to modulate the turn-on of OCD MOSFET networks can include the following:

- Local substrate potential modulation separated from ''chip'' global substrate potential due to avalanche phenomena of the MOSFET OCD drain.
- Local substrate potential electrical connections separated from the ''chip substrate'' using local guard ring structures connected to ''soft ground.''
- Local substrate potential modulation using guard ring structures and external injection elements in avalanche breakdown (e.g., $n+$ diffusions).
- Local substrate potential modulation using guard ring structures and external injection elements in forward bias (e.g., *p–n* diodes and *p*-channel MOSFET pull-up elements).
- Local substrate potential modulation using guard ring structures and electrical substrate ''pump'' circuitry.

Figure 6.13 shows an example where a *p–n* diode electrically connected to the MOSFET pull-down gate structure can electrically activate the MOSFET pull-down elements. This ''diode'' element can be a defined element or parasitic diode element. This ESD design concept can be introduced in the unused sections of a MOSFET gate-array OCD network.

Figure 6.14 shows a similar concept, where the *p*-channel MOSFET parasitic element is utilized for the gate coupling source. This can be an additional *p*-channel MOSFET or a parasitic element. Figure 6.15 shows an example of a substrate pump network and a local substrate guard ring. C. Duvvury utilized an RC-network, which gate-couples the MOSFET structure. Additionally, a ''soft ground'' is connected to the local substrate regions [45]. The ''soft-ground'' connections are also connected to the substrate through a ''substrate pump'' network that is initiated by the RC-trigger network.

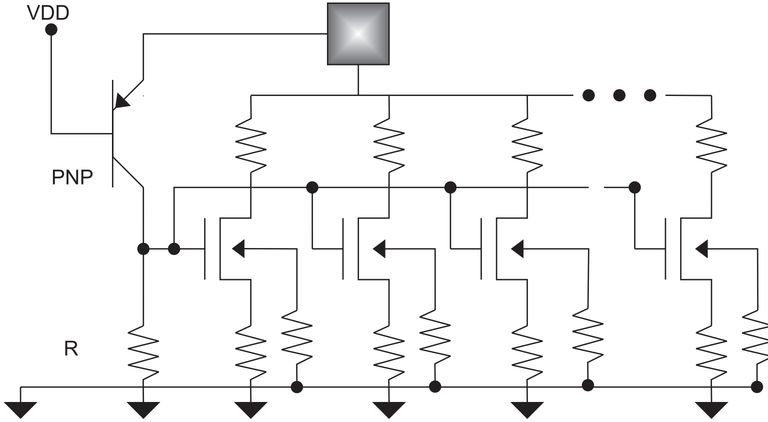

Figure 6.14 *p*-channel MOSFET driven resistor-ballasted OCD MOSFET

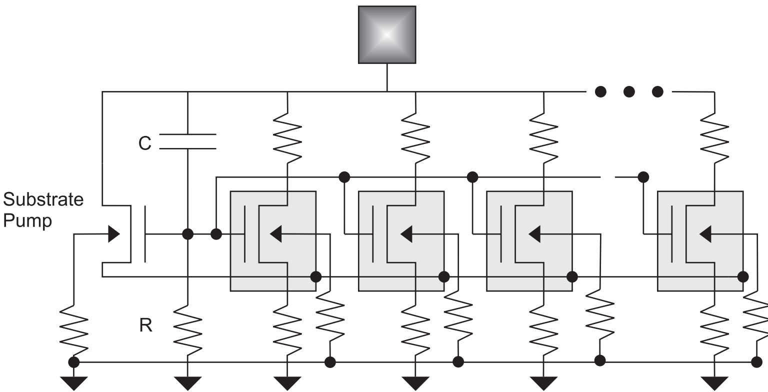

Figure 6.15 Substrate-pumped OCD MOSFET

6.10 SUMMARY AND CLOSING COMMENTS

In this chapter, we introduced both OCDs and ESD issues. MOSFET scaling, performance objectives, and new system environments changed a simple environment with simple circuits into an arena of different OCD circuit topology and issues; this also led to evolution of ESD circuits and solutions such as the Snubber-clamped diode string circuit, the self-bias well ESD circuit, and gate-modulated ESD circuit to multi-finger MOSFET domino concepts. A key point in the chapter is that a number of circuit concepts from mixed-voltage environments have influenced the ESD concepts and vice versa.

In Chapter 7, the design and layout of CMOS and BiCMOS receiver networks are discussed. Receiver networks can be the most sensitive networks in a semiconductor chip in CMOS and RF CMOS applications. As the receiver networks evolve, the ESD solutions and issues vary. The chapter will discuss the receiver evolution as well as the ESD solutions to provide better protection method for receivers. In this chapter, it will be shown that OCD concepts and OCD ESD concepts are added to the ESD receiver solutions to provide better

ESD receiver results. The understanding of receiver circuit topology and the parasitics is critical to achieving good ESD results in bulk CMOS, triple-well CMOS, and BiCMOS Silicon Germanium applications.

PROBLEMS

6.1. Given an OCD with a single *p*-channel MOSFET pull-up and a single *n*-channel MOSFET pull-down where the *p*-channel MOSFET width is twice the *n*-channel MOSFET width. Assume that between each *p*-channel MOSFET pull-up finger, there is a *n*-well contact strip connected to the V_{DD} power supply. Show a representation of the *p*-channel MOSFET pull-up as a *p–n* ideal diode with a series resistor element. Treat the *n*-well as a series resistor, whose width is equal to the width of the *p*-channel MOSFET pull-up, with a length equal to the p^+ diffusion-to-*n*-well contact spacing, and a sheet resistance associated with the *n*-well. Assume all other resistances are negligible. Assume an ESD event occurs at the input signal pad of positive-polarity. Derive the relationship of what the *n*-well sheet resistance and resistor element requirements to prevent MOSFET snapback to occur in the *n*-channel MOSFET pull-down.

6.2. Given the OCD in Problem 6.1, assume it is modified to two *n*-channel MOSFETs placed in series (in a series cascode configuration) for MVI applications. Assume that the *p*-channel MOSFET pull-up width is double the single *n*-channel MOSFET pull-down. Assume that the two *n*-channel MOSFET are of equal MOSFET channel length, and are not designed in a common *p*-well or common area. Assume that the MOSFET snapback is equal to the sum of the two MOSFET snapback values. Derive the relationship of what the resistor requirements are needed to prevent MOSFET snapback to occur in the series cascode MOSFET network.

6.3. Given the MVI OCD in Problem 6.2, assume that the two *n*-channel MOSFET pull-down elements are integrated together into a common design layout. Assume that the MOSFET snapback is equal to

$$(V_{tr1})_{\text{cascode}} = \chi(V_{tr1})$$

where χ is equal to a value between 1 and 2. Derive the relationship for the *p*-channel MOSFET resistance as a function of the integrated MOSFET pull-down network.

6.4. Assume that the relationship for the first trigger voltage in a mixed-voltage interface series cascode MOSFET is a function of the effective base width between the drain of a first MOSFET and the source of the second MOSFET. Show the relationship as a function of the MOSFET channel lengths and MOSFET gate-to-gate spacing. Can one relate the value of χ to the MOSFET channel length and gate-to-gate spacing ? How ? Note the relationship for χ is equal to

$$(V_{tr1})_{\text{cascode}} = \chi(V_{tr1})_{\text{single}}$$

6.5. Given a dual function HSTL/GTL OCD network on a common input pad. The circuit contains a standard *p*-channel MOSFET pull-up and *n*-channel MOSFET pull-down. Additionally, there is a *n*-channel MOSFET pull-up and *n*-channel MOSFET pull-down. The first network is driven by pre-drive circuitry independent of the second network. Show all the possible current paths between OCD signal pad, and the power rails V_{DD} and V_{SS} for positive and negative ESD pulses.

6.6. Given a dual function HSTL/GTL OCD network on a common input pad. The circuit contains a standard *p*-channel MOSFET pull-up and *n*-channel MOSFET pull-down. Additionally, there is a *n*-channel MOSFET pull-up and *n*-channel MOSFET pull-down. Assume the substrate rail V_{SS} is grounded. Given a positive-polarity ESD pulse, the *p*-channel MOSFET pull-up discharges to the V_{DD} power rail. In the case of all *p*-channel MOSFET pull-up networks, the current cannot discharge back to the ground rail through other parallel OCD circuits. In the case of the *n*-channel MOSFET pull-up, current can return through the OCD itself or adjacent I/O or OCD circuits. Show the possible current paths making assumptions of the voltage potential on the power supply rail. At what voltage conditions do these occur ? What is the maximum power supply voltage during an ESD event?

6.7. Assume an off-chip driver uses a resistor element in series with a *n*-channel MOSFET pull-down, and a second resistor element in series with a *p*-channel MOSFET pull-up for OCD symmetry where the *p*-channel MOSFET width is double of the *n*-channel MOSFET width. As a result of the resistor in series with the *p*-channel MOSFET, a separate ESD *p*–*n* diode element is used to provide ESD protection. Calculate the percent extra area required as a function of the design variables of the OCD network to add the extra ESD network, given that the ESD *p*–*n* diode is equal to the *p*-channel MOSFET pull-up width (e.g., ratio of area for the ESD and OCD compared to the self-protecting OCD network).

6.8. PIMP driver networks match the size of the MOSFET pull-up and pull-down elements as a function of an external resistor element. The external resistor initiates an adjustable counter that sizes the output impedance for the network. As a result, the MOSFET channel lengths are equal but the MOSFET finger widths are not equal but vary in physical size. Additionally, resistor-ballasting cannot be added. Where will the PIMP driver network fail? What is the solution to provide an ESD robust PIMP driver network?

6.9. In the mixed voltage interface networks, the *p*-channel MOSFET is used as an *n*-well bias network, first proposed by R. Flaker, where the *p*-channel MOSFET source is connected to the power supply, and its drain is connected to the *n*-well, and the *p*-channel MOSFET gate is electrically connected to the input pad. Experimental results show that this element never fails during HBM, MM, and TLP events. Why? Show the voltage conditions from the pad, the power supply, and the voltage stress conditions of the drain, source, and gate.

6.10. In the *p*-channel MOSFET pull-up stage of a ‘‘floating well’’ mixed voltage interface OCD, there are a number of *p*-channel elements to reduce the voltage stress, as well as establish the voltage potential of the *p*-channel MOSFET *n*-well. Show all the voltage

conditions and operation purposes associated with the network (e.g., Dobberpuhl or Austin-Piro-Stout implementations). Can this network be used as an ESD protection network itself?

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7 Receiver Circuits and ESD

7.1 RECEIVERS AND ESD

Receiver circuits and the ESD protection of receiver circuits are very important in ESD design. Why? Almost all products and applications contain stand-alone receivers, or bidirectional receiver/transmitter circuits. Receiver circuits are typically the most sensitive circuits in a chip application. Receiver performance has a critical role in the semiconductor chip performance. First, receiver circuits are small. Second, the receiver performance requirements limit the ESD loading on the receiver. MOSFET gate area, bipolar emitter area, and electrical interconnect wiring widths impact the receiver performance. Third, receivers are electrically connected to either the MOSFET gate (in a CMOS receiver) or the bipolar base region (in a bipolar receiver); both the MOSFET gate dielectric region and the bipolar transistor base region are the more sensitive region of the structures. Hence, they evolve with MOSFET gate dielectric scaling and bipolar transistor performance objectives. Fourth, receivers require low series resistance. Because of these factors, the receiver is also one of the most interesting network for evaluation of ESD protection. Since receivers are one of the smallest and most sensitive networks, it provides the opportunity to understand the future limitations on ESD protection of future technology generation, potential scaling implications, and lower limits of ESD protection levels achievable.

In this chapter, we will discuss receiver, receiver evolution, ESD receiver problems, receiver ESD integration and solutions, as well as special classes of receiver networks. Receivers with half- and full-transmission gates, zero-threshold voltage transmission gates, Schmitt triggers, and other networks will be used to discuss the issues and problems with receiver networks. The ESD protection sensitivity and solutions will be highlighted in the discussion.

7.1.1 Receivers and Receiver Delay Time

Receiver circuit performance can be quantified by the receiver delay time. A receiver response can be quantified as the intrinsic CMOS receiver gate delay, and the extrinsic

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receiver delay [1–5].

$$T_g = (T_g)_{int} + (T_g)_{ext}$$

The CMOS intrinsic gate delay can be expressed as

$$(T_g)_{int} = R_d(C_d + f_g C_r)$$

The extrinsic delay components of the receiver gate delay include the interconnect delay components of the CMOS gate delay and the ESD networks.

The interconnect delay components of the CMOS gate delay, excluding the intrinsic components, can be expressed as [1–5]

$$(T_g)_{ext} = f_g R_d C_w L_w + 0.4 R_w C_w L_w^2 + 0.7 R_w C_r L_w$$

where $(T_g)_{ext}$ are the interconnect-related delay terms, R_d and C_d are MOSFET output resistance and capacitance (respectively), C_r is the MOSFET receiver switching capacitance, R_w, C_w, and L_w are the resistance, capacitance, and line length of the interconnect, and f_g is the circuit fan-out [1–3]. These interconnect delay terms become a larger percentage of the total CMOS gate delay as the intrinsic delay, $(T_g)_{int} = R_d(C_d + f_g C_r)$, decreases and must be reduced through either interconnect resistance or capacitance reduction. Interconnect RC delay can be reduced by migrating from Al- to Cu-based interconnects, which improves electrical conductivity [4,5].

7.1.2 Receiver Performance and ESD Loading Effect

With the addition of ESD protection, receiver performance objectives must add the influence of the extrinsic loading on the receiver network. The extrinsic delay of the receiver can be represented as the extrinsic interconnect wiring load and the ESD element load

$$(T_g)_{ext} = (T_g)_{wire} + (R_{ESD} C_{ESD})$$

An important ESD design consideration is the relationship of the extrinsic delay terms of the receiver network. As the receiver performance objectives increase, the total extrinsic delay of the receiver must be reduced. Hence, the loading of the interconnects, the ESD element, and any other auxiliary circuitry must be evaluated in the receiver performance. There are two issues. First, the scaling of the interconnects provides for the ability to have a larger percentage of the extrinsic delay term for ESD protection. Second, the scaling of the interconnect can lead to ESD failures [6–12]. The transition from Al to Cu interconnects is important not only for semiconductor chip performance objectives but also for ESD robustness in high-performance chips. Aluminum interconnects was a significant ESD failure mechanism in high-pin-count microprocessor chips for the 250 nm and sub-250 nm technology generations due to the interconnect scaling and system level wire-ability requirements [6,7]. With the migration to a low-k material, the extrinsic delay loading associated with interconnects can be reduced [11,12]. As the interconnect extrinsic delay term is reduced, this will provide some reduced relief on the scaling of the ESD network extrinsic delay factor on receiver networks.

7.2 RECEIVERS AND ESD

Providing ESD protection for receiver networks is a challenge because of the receiver performance requirements and the receiver evolution for each technology generation [10]. A few standard circuit topologies are used for ESD protection of receivers for both HBM and CDM events.

7.2.1 Receivers and HBM

For HBM events, receiver networks used ESD networks include the following:

- Primary stage of a grounded-gate thick oxide MOSFET, a resistor, and a grounded-gate thin oxide MOSFET element.
- Primary stage of a double-diode ESD network.

In early development, grounded-gate ‘‘thick oxide’’ MOSFETs were designed using a parasitic device; the LOCOS isolation served as a thick oxide gate structure, and the LOCOS region defined the source and drain regions. The primary stage of the ESD network would initiate when MOSFET snapback occurred in the ‘‘thick oxide’’ MOSFET. Avalanche breakdown in the primary thick oxide MOSFET would allow conduction to the MOSFET source. Additionally, the standard MOSFET structure served as a secondary stage. With MOSFET avalanche breakdown in the thin oxide MOSFET, the secondary stage would provide conduction to the thin oxide MOSFET source. In conjunction with the resistor element, a resistive divider was formed, allowing a lower voltage on the input node of the MOSFET receiver gate dielectric. In some implementations, the substrate conduction lead to a dynamic threshold effect on the thick oxide MOSFET where the secondary stage influenced the primary stage triggering and conduction process. This topology was favored in NMOS technology where there was no *p*-channel MOSFET to utilize for ESD protection. Additionally, with the introduction of shallow trench isolation (STI), the usage of the primary ‘‘thick oxide’’ MOSFET usage was curtailed because of the high turn-on voltage of the parasitic STI-defined *npn* element (Figure 7.1).

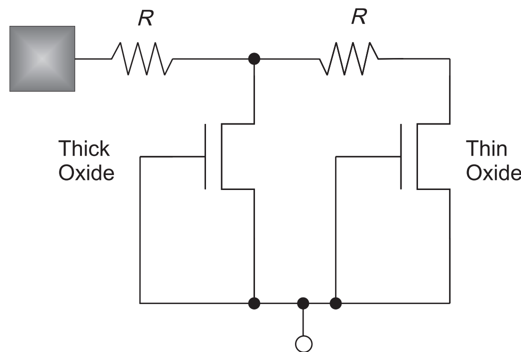

Figure 7.1 Thick oxide/resistor/thin oxide MOSFET ESD network

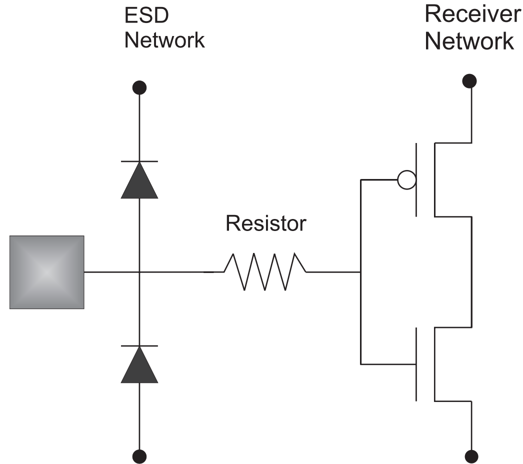

Figure 7.2 Double-diode ESD network

Double-diode ESD networks using two diode elements between the input pad and the two power rails is used in CMOS technology. Diode structures were formed utilizing the *p*-channel and *n*-channel MOSFET source/drain regions as well as the well and tub regions (Figure 7.2).

7.2.2 Receivers and CDM

For CDM events, receiver networks used ESD networks include the following:

- Primary stage of a double-diode ESD network, a resistor, and a secondary stage consisting of a second double-diode ESD network.
- Primary stage of a double-diode ESD network, a series resistor, and a secondary stage of a grounded-gate MOSFET ESD element.

Figure 7.3 shows an example of an ESD network with a primary stage of a double-diode ESD network, a resistor, and a secondary stage consisting of a second double-diode ESD network. Some of the advantages of this network are as follows:

- Scaling.
- Migration.
- Avoidance of dielectric regions.

Figure 7.4 shows a second embodiment of a network that combines both the diode-based and MOSFET-based ESD protection. The advantage of this network is the utilization of the resistor/thin oxide MOSFET provides a resistor divider operation. This improves both the

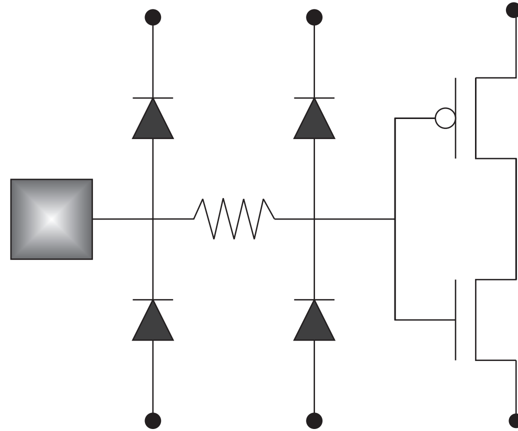

Figure 7.3 Primary stage of a double-diode ESD network, a resistor, and a secondary stage consisting of a second double-diode ESD network

HBM and the CDM ESD results. This CDM network has some of the following advantages:

- Primary and secondary stages both active during HBM events.
- Utilization of MOSFET drain for CDM protection.
- Allowance of a lower series resistor element.

7.3 RECEIVERS AND RECEIVER EVOLUTION

In CMOS, with MOSFET constant electric field scaling theory, the MOSFET dielectric thickness and power supply voltage are scaled to provide improved MOSFET device

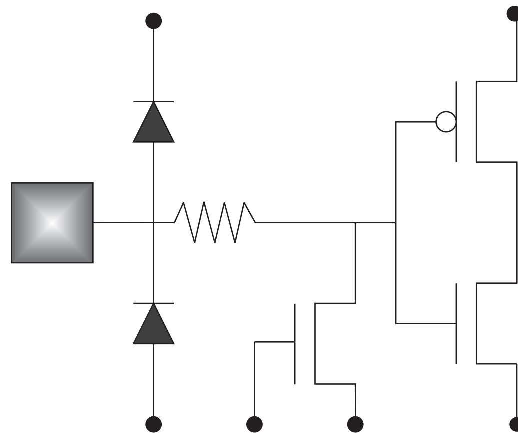

Figure 7.4 Primary stage of a double-diode ESD network, a series resistor, and a secondary stage of a grounded-gate MOSFET ESD element

performance. With MOSFET dielectric scaling, power supply scaling, voltage signal level scaling, and the introduction of mixed-voltage interface applications, receiver architecture, and design continues to become more complex [10,13–32]. In CMOS technology, for 5 and 3.3 V power supply, the dielectric thickness in receiver networks allowed for direct electrical connections to MOSFET gate structures [13,14]. As the power supply was scaled, and with the introduction of mixed-voltage applications, the need to reduce the voltage stress on the dielectric was achieved using a transmission gate (TG) or pass transistor to lower the voltage levels [10]. With decreasing voltage levels, mixed-voltage signals, and dielectric over-voltage condition concerns, a plethora of new receiver circuits evolved with new features: half-pass transmission gates, full-pass transmission gates, pseudo-zero threshold voltage transmission gates, zero threshold voltage threshold voltages, keeper feedback networks, and hysteresis feedback elements. Each of these provided new ESD receiver issues and challenges [10].

7.3.1 Receiver Circuits with Half-Pass Transmission Gate

A common element in a receiver network is a transmission gate network. A half-pass transmission gate, using an n-channel MOSFET element is electrically connected between the ESD element and the MOSFET inverter stage of the receiver network. A TG has an influence on the ESD robustness of a receiver. The TG typically is involved in the ESD failure from HBM, MM, and CDM events. The TG structure is typically connected to the input pad, and the power supply, V_{DD}, making it vulnerable during ESD events.

A TG is a voltage-controlled switch which has a high and low impedance state. In a half-pass TG, the TG is typically a single MOSFET structure whose source and drain are connected in a series fashion between the input pad and the MOSFET receiver gate stage (Figure 7.5). The MOSFET gate controls the logic state. When the n-channel MOSFET gate has a gate voltage equal to the power supply voltage, V_{DD}, the logic transfers a logic "1" from the pad to the receiver.

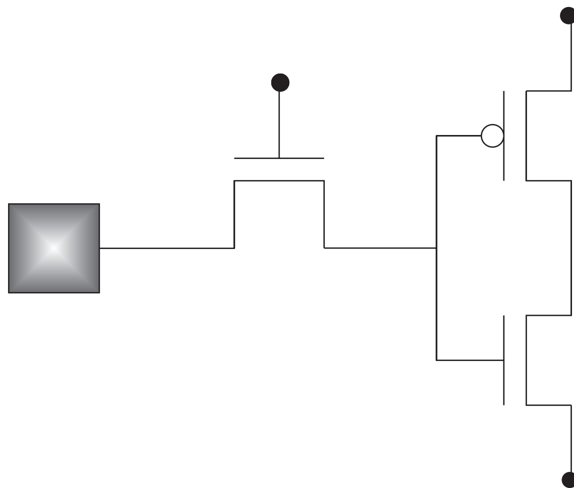

Figure 7.5 MOSFET receiver network with n-channel MOSFET half-pass TG

Assuming the receiver network is initially uncharged, the output capacitance has an initial value. In this state, the voltage that will be observed at the output of the TG, assuming a loading capacitance, C, is [15]

$$V_{\mathrm{out}}(t) = (V_{\mathrm{DD}} - V_{\mathrm{T}n})\left[\frac{(t/\tau_{\mathrm{ch}})}{1 + (t/\tau_{\mathrm{ch}})}\right]$$

with a charging time of

$$\tau_{\mathrm{ch}} = \frac{2C}{\left(\frac{W}{L}\right)(V_{\mathrm{DD}} - V_{\mathrm{T}n})}$$

When the ratio of the time to charging time is long, the output voltage approaches the maximum output voltage, during functional operation of the circuit

$$V_{\mathrm{out}} = V_{\mathrm{DD}} - V_{\mathrm{T}n}$$

From a functional perspective, the highest voltage output value is a threshold voltage lower than the voltage placed on the n-channel MOSFET gate electrode. The MOSFET half-pass transistor TG also has a characteristic resistance. The resistance can be expressed as

$$R_n = \frac{1}{\left(\frac{W}{L}\right)(V_{\mathrm{DD}} - V_{\mathrm{T}n})}$$

The resistance of the MOSFET half-pass transistor plays a role in the ESD event in that it current-limits the amount of current that can flow from the signal pad to the MOSFET receiver network. In conjunction with other circuit elements, and additional ESD elements, it serves as a resistor divider. During ESD events, after the MOSFET snapback voltage, the resistance of interest is the MOSFET dynamic on-resistance.

During ESD operation, there are two points that influence the operation of the n-channel MOSFET half-pass transistor. First, the output voltage will be dependent on the MOSFET gate voltage state. Second, the MOSFET snapback voltage has a role in the voltage drop, and the conduction process through the half-pass transistor.

In the case of the voltage on the MOSFET gate electrode, assuming the gate is floating, the state of the gate electrode is a function of the half-pass transistor input-to-gate capacitance and the other electrode capacitances that form a capacitor divider network. As the input voltage increases, the capacitance coupling between the MOSFET half-pass transistor input-to-gate capacitor causes the MOSFET gate to rise.

At the same time, as the input voltage on the MOSFET pass-transistor increases, and the half-pass transistor drain-to-source voltage increases, the MOSFET snapback voltage is reached leading to MOSFET snapback. In order for MOSFET snapback to occur, the impedance in series with the MOSFET half-pass transistor must allow current conduction. In the case that there are no circuit elements except the MOSFET receiver inverter stage, the current conduction leads to a charging of the MOSFET gates. As the current flows through the half-pass transistor, the MOSFET gates of the inverter stage increases until the current through the MOSFET half-pass transistor fails, or MOSFET gate dielectric breakdown occurs.

In the case of additional other elements in the receiver network between the MOSFET half-pass transistor and the MOSFET receiver inverter stage, a current path can be established leading to current flowing through the MOSFET half-pass transistor, and the additional elements. The presence of the other elements can lead to MOSFET second breakdown of the MOSFET half-pass TG structure.

The introduction of the MOSFET half-pass transistor establishes a voltage margin allowing the operation of the ESD networks to discharge current away from the receiver network and through the ESD network current loop. For ESD events that occur at the input signal pads, the ESD elements should be placed between the signal pad and the MOSFET half-pass transistor (e.g., HBM, MM, and TLP events).

For charged device model (CDM) events, the ESD current flows from the substrate to the signal pad. In the case of a p^- substrate which is charged positively, when the signal pad is placed at a ground potential, current will flow from the chip substrate to the signal pad. When there is a n-channel MOSFET half-pass transistor TG, current will flow in a few different current paths.

- First, current will flow from the substrate to the n-diffusion (e.g., p^- substrate-to-n-channel MOSFET diffusion metallurgical junction) input side of the MOSFET half-pass TG.
- A second current path is through the MOSFET receiver inverter stage n-channel MOSFET gate and continued through the MOSFET half-pass transistor channel region (e.g., source-to-drain).
- When there are more circuit elements present between the MOSFET half-pass transmission gate and the MOSFET inverter stage, current will flow through those circuit elements and through the n-channel MOSFET half-pass transmission gate.

In the case that the current is flowing from the output side of the MOSFET half-pass TG, there is a delay time that occurs to allow the current to flow to the signal pad from the interior of the chip. If we assume the MOSFET inverter stage, a capacitance, C, and the voltage rise to a maximum voltage condition, we can estimate the MOSFET half-pass transistor delay time by assuming the signal pad is at a ground potential [15]

$$V_{\text{out}}(t) = (V^* - V_{\text{T}n})\left[\frac{2\exp(-t/\tau_{\text{d}})}{1+\exp(-t/\tau_{\text{d}})}\right]$$

and discharge time [15]

$$\tau_{\text{d}} = \frac{2C}{\left(\dfrac{W}{L}\right)(V^* - V_{\text{T}n})}$$

During functional operation, the voltage $V^* = V_{\text{DD}}$. During ESD events, the MOSFET half-pass TG voltage is a function of the capacitive divider formed between the gate-to-source, and gate-to-drain capacitances.

From an ESD design perspective, the key issues associated with MOSFET half-pass transistor transmission gates are the following:

- Half-pass MOSFET TG elements are to be placed between HBM ESD networks and MOSFET receiver inverter stages.
- Half-pass MOSFET TG elements are vulnerable to ESD events due to the electrical placement in series with the MOSFET receiver inverter stage and the input signal pad.
- Half-pass MOSFET TG element are vulnerable to ESD events due to the electrical placement in series with the signal pad and the power rails (e.g., V_{SS} and V_{DD}).
- Half-pass MOSFET TG elements must be integrated with the HBM ESD networks, CDM networks, and additional receiver network functions to provide good ESD results in receiver signal pads.
- MOSFET-based receiver network ESD failures typically involve failure of the MOSFET half-pass TG element.
- MOSFET half-pass TG ESD failure during HBM events are typically MOSFET source-to-drain failures.
- MOSFET half-pass TG ESD failure during CDM events can be MOSFET substrate-to-input diffusion contact and junction failure, MOSFET source-to-drain, and MOSFET gate-to-input diffusion failure mechanisms.

7.3.2 Receiver with Full-Pass Transmission Gate

A common element in a receiver network is a TG. TGs are in the form of full- and half-pass TGs. A full-pass TG, uses a *p*-channel MOSFET and an *n*-channel MOSFET element. The logic states of the full-pass transistor for the *p*-channel and *n*-channel half-pass elements are complementary. A TG is a voltage-controlled switch which has a high and low impedance state. In a full-pass TG, the TG has both the *p*-channel and *n*-channel MOSFET structure sources and drains connected in a series between the input pad and the MOSFET receiver gate stage [13]. The MOSFET gate controls the logic state. When the *n*-channel MOSFET gate has a gate voltage equal to the power supply voltage V_{DD}, the logic transfers a logic "1" from the pad to the receiver. When the *p*-channel MOSFET gate has a gate voltage equal to the power supply voltage V_{SS} , the logic transfers a logic "1" from the pad to the receiver. Figure 7.6 shows the full-pass TG electrically connected between the ESD element and the MOSFET inverter stage of the receiver network.

A full-pass TG has an influence on both the ESD robustness of a MOSFET receiver network [13]. During a positive-polarity ESD HBM event, a positive pulse occurs on input pad. When the potential of the p^+/n-well diode element reaches forward bias, current flows through the diode element to the V_{DD} power supply. As this occurs, the voltage potential on the input of the full-pass transistor begins to increase. In the case of an *n*-channel half-pass transistor, the voltage differential across the *n*-channel device would increase until MOSFET snapback would occur; if gate-coupling occurs, the half-pass may under MOSFET turn-on during ESD pulse events. In the case of the full-pass TG, as the voltage drop increases, the *p*-channel pass transistor p^+/n-well node will forward bias; this leads to forward-active operation of the lateral and/or vertical parasitic *pnp* bipolar transistor. In the case of the lateral parasitic *pnp* element, this will lead to a decrease in the voltage-differential across the full-pass TG. In some sense, the *p*-channel half-pass TG transistor prevents failure

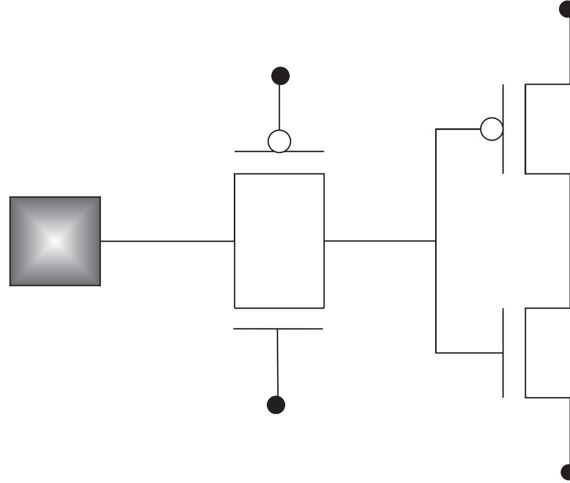

Figure 7.6 Full-pass TG integrated between the ESD network and the MOSFET receiver

of the *n*-channel half-pass TG transistor. In the case of a negative-polarity event, the half-pass transistor will discharge to the semiconductor substrate, in parallel with the *n*-well/*p*-substrate diode ESD element.

Figure 7.7 shows the experimental results of a MOSFET receiver network as a function of *n*-well sheet resistance for a positive HBM pulse event (with the substrate grounded). Experimental results show that the highest HBM ESD results occur with the full-pass

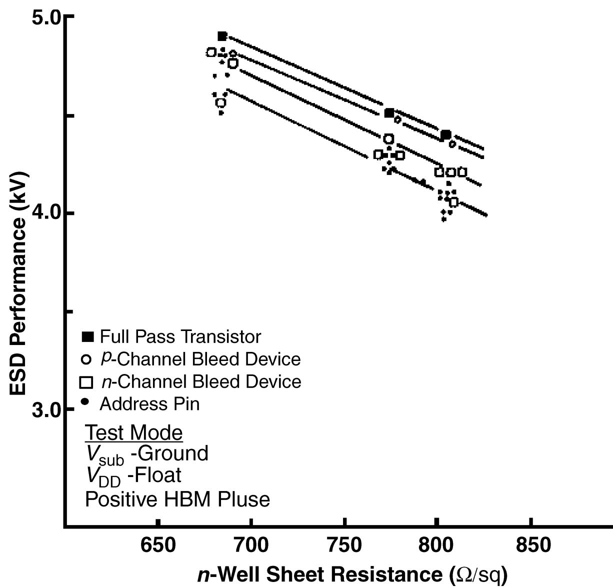

Figure 7.7 ESD HBM results as a function of *n*-well sheet resistance of receiver networks with and without full-pass transistor elements (with the grounded reference V_{SS})

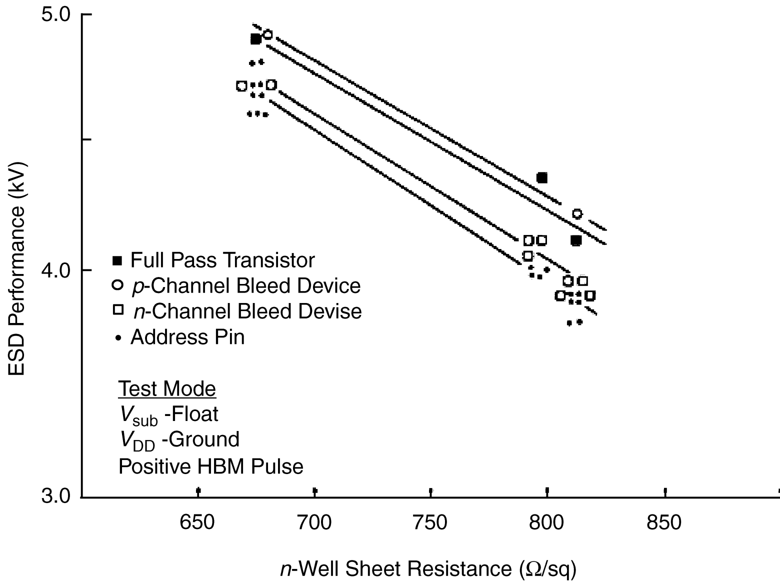

Figure 7.8 ESD HBM results as a function of *n*-well sheet resistance of receiver networks with and without full-pass transistor elements (with the grounded reference V_{DD})

transistor. Figure 7.8 shows the experimental results of a MOSFET receiver network as a function of *n*-well sheet resistance for a positive HBM pulse event (with the V_{DD} power rail grounded). A key point in the results is that the presence of the full-pass TG does not degrade the ESD protection results in the receiver. The experimental results show that the highest results occur with the presence of a *p*-type element on the input node, which improves the receiver network results. Independent of the *n*-well sheet resistance or reference polarity, for a positive pulse event, the highest address pin results occur with the full-pass TG.

7.3.3 Receiver, Half-Pass Transmission Gate, and Keeper Network

With the introduction of the MOSFET half-pass TG in receiver networks, the quality of the CMOS logic levels is hampered in CMOS receiver networks. The half-pass TG, using an *n*-channel MOSFET element is electrically connected between the ESD element and the MOSFET inverter stage of the receiver network [10]. A half-pass TG is a voltage-controlled switch which has a high and low impedance state. In a half-pass TG, the TG is typically a single *n*-channel MOSFET structure whose source and drain are connected in a series fashion between the input pad and the MOSFET receiver gate stage. The MOSFET gate controls the logic state. When the *n*-channel MOSFET gate has a gate voltage equal to the power supply voltage V_{DD}, the logic transfers a logic “1” from the pad to the receiver.

The output voltage of the half-pass transistor can be expressed as [15]

$$V_{\text{out}}(t) = (V_{\text{DD}} - V_{\text{T}n})\left[\frac{(t/\tau_{\text{ch}})}{1 + (t/\tau_{\text{ch}})}\right]$$

with a charging time of [15]

$$\tau_{\text{ch}} = \frac{2C}{\left(\frac{W}{L}\right)(V_{\text{DD}} - V_{\text{T}n})}$$

The output voltage then asymptotically approaches a maximum condition of

$$V_{\text{out}} = V_{\text{DD}} - V_{\text{T}n}$$

When the power supply voltage of a technology is large compared to the MOSFET threshold voltage, the output voltage is within the receiver level to distinguish a logic "1" level from intermediate transition levels and logic "0" levels. The MOSFET threshold drop that incurs with a half-pass TG impacts the margin of a logic "1" level. The output level of the half-pass transistor, which is below the full power supply voltage, is also referred to as a logic weak "1" state. When the weak "1" is present at the input of the MOSFET receiver inverter stage, the ability to have the MOSFET receiver inverter transition to a logic "0" is compromised. As technology is scaled, the power supply decreased from 5 to 2.5 V and the weak "1" logic level became a larger issue.

To address the impact of the half-pass MOSFET TG network on the receiver state, a "half-latch," also known as a MOSFET keeper network, is placed on the output of the MOSFET inverter stage. Figure 7.9 shows the MOSFET receiver network with the half-pass MOSFET TG and the MOSFET keeper network. In the network, a *p*-channel MOSFET keeper network source and drain is electrically connected to the input side of the MOSFET receiver inverter stage. The gate of the *p*-channel MOSFET keeper network is connected to the output stage of the MOSFET receiver inverter stage. In this fashion, the MOSFET keeper network serves as a feedback element between the output and the input of the MOSFET

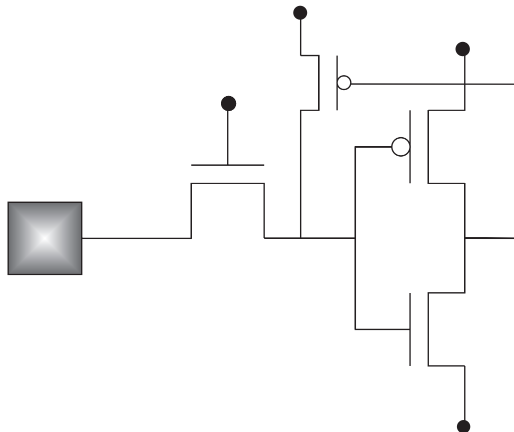

Figure 7.9 MOSFET receiver network with the half-pass MOSFET TG and the MOSFET keeper network

receiver inverter stage. Fundamentally, it is acting as a feedback latch, as is present in a latch network (e.g., this is present in latches, SRAM cells, and other applications).

In this network, when a logic "1" level is on the signal pad, the output of the MOSFET TG is a logic "weak 1" level. This is inverted by the MOSFET inverter stage to a weak logic "0." The *p*-channel MOSFET keeper gate voltage is driven to a weak logic "0" state. When the *p*-channel MOSFET keeper voltage reaches the *p*-channel MOSFET keeper level, the keeper element conducts current between the V_{DD} power supply and the MOSFET receiver inverter input stage. The *p*-channel MOSFET keeper charges the input of the MOSFET receiver inverter stage to the V_{DD} power supply, leading to a good logic "1" state; this condition then outputs a good logic "0" state on the output of the MOSFET inverter stage [15].

The introduction of the *p*-channel MOSFET keeper network (e.g., half-latch feedback element), although it served significant value for logic functionality, introduces a new ESD failure mechanism in receiver networks [10]. During an ESD event, where a positive polarity current pulse is applied to the signal pad, and the power supply V_{DD} serves as a reference ground, the presence of the MOSFET half-latch circuit constrains the voltage potential of the half-pass MOSFET TG element. The reason is that the *p*-channel MOSFET *n*-well is electrically connected to a power supply V_{DD}. When V_{DD} is grounded, the metallurgical junction formed between the *p*-channel drain and the *n*-well region "pins" the electrical potential of the *p*-channel MOSFET keeper drain at the forward-bias diode voltage, V_{be}. The parasitic diode formed between the *n*-well and the *p*-channel MOSFET keeper forces the half-pass MOSFET TG voltage to be constrained to within a forward bias voltage drop relative to the ground reference. In this fashion, the voltage from the signal pad minus the forward-bias diode voltage is there across the TG. During ESD testing, this leads to MOSFET second breakdown of the half-pass MOSFET TG. The physical damage is evident from the MOSFET source-to-drain junction, and within the *p*-channel MOSFET keeper drain (e.g., the *p*-channel MOSFET drain contacts to diffusion region). In the case that no *p*-channel MOSFET keeper is present, the output of the half-pass MOSFET TG rises until MOSFET gate dielectric breakdown of the MOSFET inverter stage. With the pinning of the half-pass MOSFET TG, the voltage-to-failure of the MOSFET receiver network is equal to the sum of the MOSFET second breakdown voltage, the forward-bias voltage of the *p*-channel MOSFET to *n*-well voltage, and corresponding series resistances in the *n*-well (Figure 7.10).

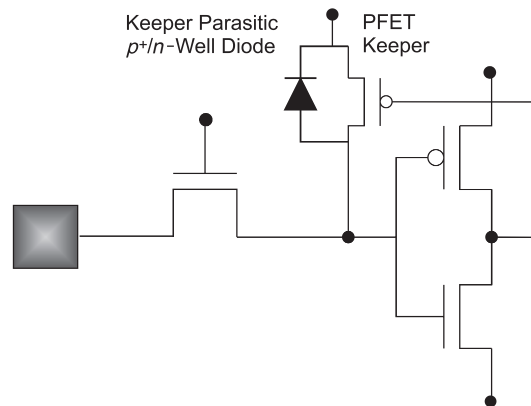

Figure 7.10 MOSFET receiver network with the half-pass MOSFET TG and the MOSFET keeper network, highlighting the parasitic diode electrically connected to the V_{DD} power supply voltage

The ESD degradation of the addition of the *p*-channel MOSFET keeper network was apparent in the evolution of the MOSFET receiver networks. In the evolutionary transition from 5 to 2.5 V power supplies with the CMOS scaling, these elements were introduced with a rapid decrease in the HBM ESD protection levels of receiver networks. J. Zimmerman and S. Voldman showed that in an integrated design with a signal pad, a diode-based ESD network, and a MOSFET receiver signal pad with a half-pass TG, an inverter, and a *p*-channel MOSFET keeper element lead the network achieved 2.5 kV HBM levels. It was shown that by removal of the *p*-channel MOSFET keeper element, the HBM ESD protection levels increased from 2.5 to 7.5 kV. This demonstrated that the impact of the protection levels were significantly impaired by the *p*-channel MOSFET keeper feedback element. An ESD design concept demonstrates that the presence of feedback element and the electrical connections of physical elements associated with the grounded references can impair ESD protection levels of receiver networks. The addition of small physical elements coupled to the power supply references can introduce significant reduction of protection results in some test modes.

To avoid ESD protection concerns with the MOSFET receiver network with the half-pass TG, inverter stage, and the MOSFET keeper feedback network, the following ESD design solutions can be implemented:

- Add resistance in series with elements that do not impact circuit performance.
- Eliminate the ‘‘pinning’’ of the output node of the half-pass TG.
- Decouple the element from the grounded V_{DD} reference.

To improve the ESD robustness of the receiver network, the following solutions can consist of the following:

- Add resistance in series with the *p*-channel MOSFET keeper network between the MOSFET inverter stage input node and the *p*-channel MOSFET keeper drain node.
- Add a resistor between the V_{DD} and the *n*-well resistance of the *p*-channel MOSFET keeper network in series with the forward-bias metallurgical junction formed between the *p*-channel MOSFET drain and the *n*-well.
- Add a resistor after the half-pass MOSFET TG node and before the *p*-channel MOSFET keeper drain node.

7.3.4 Receiver, Half-Pass Transmission Gate, and the Modified Keeper Network

The introduction of the *p*-channel MOSFET keeper network (e.g., half-latch feedback element), although it served significant value for logic functionality, introduces a new ESD failure mechanism in receiver networks. During an ESD event, where a positive polarity current pulse is applied to the signal pad and the power supply V_{DD} serves as a reference ground, the presence of the MOSFET half-latch circuit constrains the voltage potential of the half-pass MOSFET TG element. To avoid the ‘‘pinning’’ of the half-pass transistor MOSFET TG output voltage, the decoupling of the electrical node from the grounded reference power supply is needed [10]. In the prior section, the means of decoupling

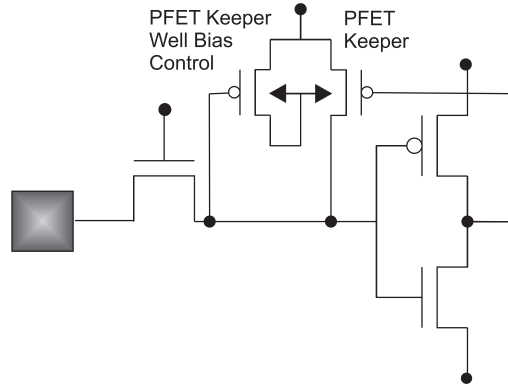

Figure 7.11 MOSFET receiver network with half-pass MOSFET TG, an inverter stage, and a modified MOSFET keeper half-latch network

recommended introduction of resistor elements in three different locations within the current path that initiates the "pinning" of the node by the *p*-channel MOSFET keeper network.

The electrical decoupling of the *p*-channel MOSFET keeper *n*-well node can be achieved by introduction of a network that allows the *n*-well to "float" when the V_{DD} power supply is ground reference [19]. Figure 7.11 shows the introduction of a modified MOSFET keeper network. Voldman first introduced and applied the concept of the *n*-well bias control network to the half-pass MOSFET keeper network to avoid ESD concerns in receivers [19]. The receiver network consists of a half-pass MOSFET TG followed by the MOSFET *p*-channel keeper element, and the MOSFET receiver inverter stage. An additional *p*-channel MOSFET is added whose source is electrically connected to the V_{DD} power supply rail, and drain is connected to the *n*-well of the MOSFET *p*-channel keeper element. The *p*-channel MOSFET drain is also electrically connected to its own *n*-well. The gate of the new element is connected to output side of the half-pass MOSFET TG. Note that R. Flaker first introduced this concept for mixed voltage interface (MVI) off-chip driver (OCD) networks for decoupling of the *p*-channel MOSFET driver pull-up from the power supply [23,24]. In this implementation, the concept of Flaker's "*n*-well bias control network" is applied to a receiver network feedback element and serves the ESD function to decouple the MOSFET feedback element node from the V_{DD} power supply during ESD testing [23,24]. In this implementation, there exist different networks to achieve the same objective [25–31].

In the operation of the network, when a positive polarity ESD pulse occurs on the signal pad, the input of the half-pass MOSFET TG begins to rise. Through capacitive coupling of the gate node, and the current flow through the half-pass transistor, the voltage increases on the output of the half-pass MOSFET transistor. As the half-pass transistor output rises, the first *p*-channel MOSFET gate rises, turning the *p*-channel MOSFET "off." The *p*-channel MOSFET decouples the *n*-well node of the *p*-channel MOSFET keeper feedback element from the V_{DD} power supply. In this fashion, as the voltage continues to increase, the metallurgical junction formed between the *p*-channel drain and the *n*-well region forward biases and charges up its local *n*-well, which "floats" but does not "pin" the voltage potential. The parasitic diode formed between the *n*-well and the *p*-channel MOSFET keeper no longer forces the half-pass MOSFET TG voltage to be constrained to within a forward-bias voltage drop relative to the ground reference. With the modified keeper network, the

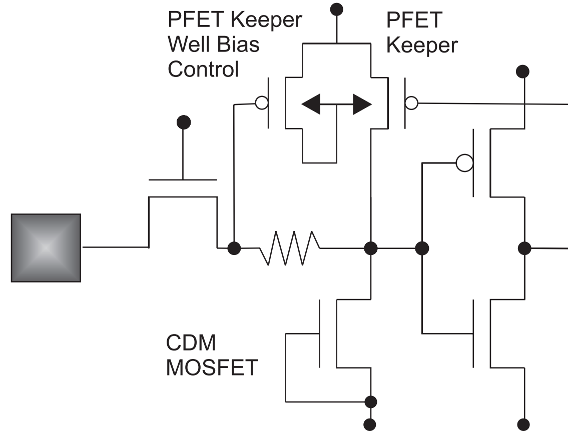

Figure 7.12 Receiver network with the half-pass MOSFET TG, the modified keeper network, and a charged device model (CDM) grounded-gate MOSFET

output of the half-pass MOSFET TG rises until MOSFET gate dielectric breakdown of the MOSFET inverter stage.

As an ESD design practice, to avoid ESD protection concerns with the MOSFET receiver network with the half-pass TG, inverter stage, and the MOSFET keeper feedback network, the following ESD design solutions can be implemented:

- Eliminate the ‘‘pinning’’ of the output node of the half-pass TG.
- Decouple the element from the grounded V_{DD} reference by introduction of logic circuitry.
- Decouple the element from the grounded V_{DD} reference by introduction of *n*-well or *p*-well bias control networks.

This network can be further extended by the introduction of charged device model (CDM) protection elements. A grounded-gate *n*-channel MOSFET can be added after the half-pass MOSFET TG network (Figure 7.12).

7.4 RECEIVER CIRCUITS WITH PSEUDO-ZERO V_T HALF-PASS TRANSMISSION GATES

With the introduction of the half-pass MOSFET TG, the threshold voltage impacts the quality of the logic level. One method to avoid the loss of the threshold drop is to provide a MOSFET with a zero threshold voltage (also known as a ‘‘Zero V_T’’ MOSFET) [17,18]. Another technique is to set the half-pass MOSFET TG voltage at a gate voltage so that the effective logic level is maintained [20].

In a standard half-pass MOSFET TG, the output voltage is equal to

$$V_{out}(t) = (V_{DD} - V_{Tn})\left[\frac{(t/\tau_{ch})}{1 + (t/\tau_{ch})}\right]$$

with a charging time of

$$\tau_{ch} = \frac{2C}{\left(\frac{W}{L}\right)(V_{DD} - V_{Tn})}$$

Assuming a reference voltage setting which is equal to

$$V_{REF} - V_{Tn} = V_{DD}$$

then a reference voltage value equal to

$$V_{REF} = V_{Tn} + V_{DD}$$

exists where

$$V_{out}(t) = (V_{REF} - V_{Tn})\left[\frac{(t/\tau_{ch})}{1 + (t/\tau_{ch})}\right]$$

or

$$V_{out}(t) = (V_{DD})\left[\frac{(t/\tau_{ch})}{1 + (t/\tau_{ch})}\right]$$

To establish a reference voltage, a voltage reference network can be constructed where the reference voltage is above the power supply voltage by the n-channel MOSFET half-pass TG threshold voltage.

Figure 7.13 shows an example of a voltage reference network for a half-pass pseudo-zero V_T TG. M. Johnson utilized two p-channel MOSFET devices to form the gate reference

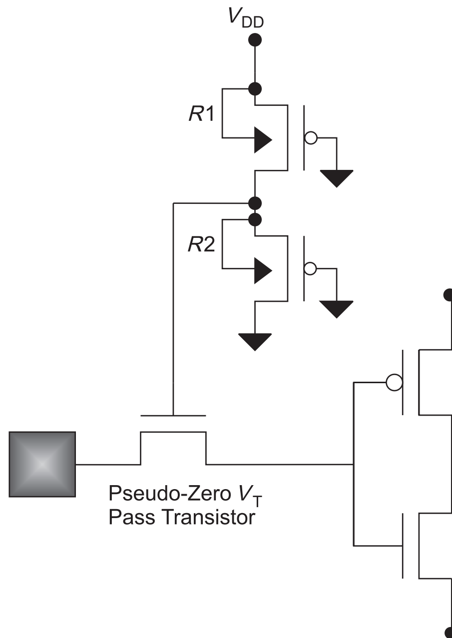

Figure 7.13 Half-pass pseudo-zero V_T TG

voltage; two *p*-channel MOSFET transistors are used as a resistive voltage divider between a higher power supply rail and the ground rail. The gate of the *p*-channel transistors are established, so the MOSFETs are in a normally on-state during chip operation.

One issue with the receiver network is the potential of the electrical ''pinning'' of the half-pass transistor MOSFET gate electrode during ESD testing relative to the V_{CC} and V_{SS} power rails. When the V_{CC} power rail is a grounded reference during ESD testing or events, the *p*-channel MOSFET of the reference network will pin the half-pass transistor MOSFET gate to within one forward-bias diode voltage. The metallurgical junction formed between the *p*-channel drain and the *n*-well will ''pin'' the half-pass transistor gate voltage. As the pad voltage rises, the half-pass MOSFET TG input-to-gate voltage will increase. This can lead to MOSFET dielectric breakdown in the input-to-gate region.

An ESD design practice can be instituted that prevents ESD failure as follows:

- Add resistance in series with the half-pass transistor MOSFET gate electrode.
- Add an isolating ''switch'' that decouples the half-pass transistor gate from the reference controller.
- Decouple the voltage reference well nodes from the power supplies using *n*-well control bias networks.

Figure 7.14 shows an example of a pseudo-Zero V_T half-pass voltage reference network with *n*-well decoupling networks [20]. As the half-pass transistor MOSFET TG input-to-gate voltage increases, the gate node rises. As the TG MOSFET gate electrode rises, the *n*-well of

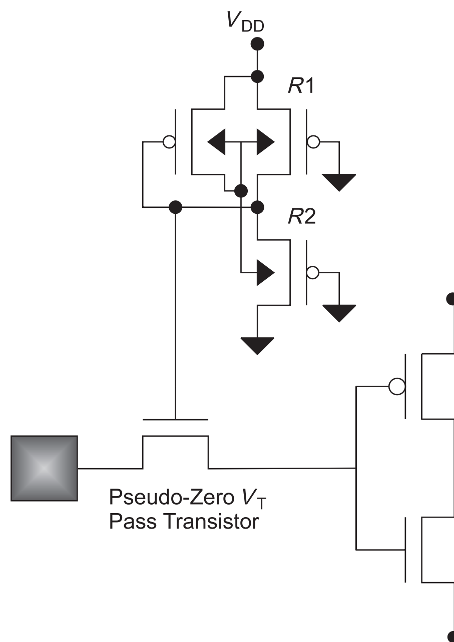

Figure 7.14 Pseudo-zero V_T half-pass voltage reference network with *n*-well decoupling elements

the voltage reference networks decouple from the V_{CC} power supply electrodes. This allows the half-pass TG MOSFET gate electrode "float" and avoid electrical overstress.

7.5 RECEIVER WITH ZERO TRANSMISSION GATE

Receiver networks that utilize a TG (or pass transistor) have the issue of voltage level reduction at the output side of the TG when the threshold voltage is non-zero. Using a MOSFET with a zero threshold voltage (e.g., also referred to as a "zero V_T" device), the threshold voltage drop across the TG in receiver networks can be avoided [17]. Zero V_T MOSFET devices are formed by constructing the MOSFET device as a standard MOSFET, but avoid the MOSFET threshold voltage implant and the *p*-well implant under the MOSFET gate structure. For example, a zero V_T *n*-channel MOSFET is formed in the *p*-substrate wafer, or p^- epitaxial region in a region without the *p*-well implant (Figure 7.15). The *p*-channel MOSFET threshold adjust implant is also blocked to avoid the increase in the MOSFET threshold voltage.

Zero V_T devices are typically utilized in high-performance receiver applications [17,18]. Adams, Braceras, Connor, and Evans introduced a receiver network to achieve the following objectives:

- Provide an input signal of the native voltage level to the gate dielectric (without the TG voltage drop).
- Prevent overshoot voltage conditions that lead to dielectric over-voltage of the pass transistor or the MOSFET gate dielectric.
- Prevent undershoot voltage conditions that lead to dielectric over-voltage of the pass transistor or the MOSFET gate dielectric.
- Provide receiver which does not use multiple power supply voltages or burn dc power.

In the aforementioned circuit network, a zero-V_T (ZVT) transistor is used as the pass transistor. Additionally, an *n*-channel MOSFET source is connected to the output of the TG transistor and its drain is connected to the MOSFET gate of the TG. The MOSFET gate of this element is electrically tied to ground. The gate of the MOSFET ZVT TG is not connected directly to the power supply, but is connected through an "on" *p*-channel MOSFET whose gate is grounded.

The MOSFET (ZVT) TG, also known as the "ZPASS" network prevents positive overshoot or mixed-voltage conditions to apply an over-voltage condition to the receiver gate structure. In this fashion, positive overshoots are limited to the voltage condition on the gate of the MOSFET (ZVT) device.

For a negative undershoot, current flows through the MOSFET (ZVT) TG, the *n*-channel transistor and the *p*-channel device. The *p*-channel and *n*-channel transistor serves as a resistor divider network whose center node voltage divides the condition on the MOSFET (ZVT) device gate structure. This prevents dielectric overstress of the TG dielectric, and also clamps the voltage condition on the MOSFET receiver gate dielectric.

Whereas this receiver network provides a good solution to minimize the overshoot and undershoot conditions on the MOSFET gate dielectric, the addition of the resistor–divider

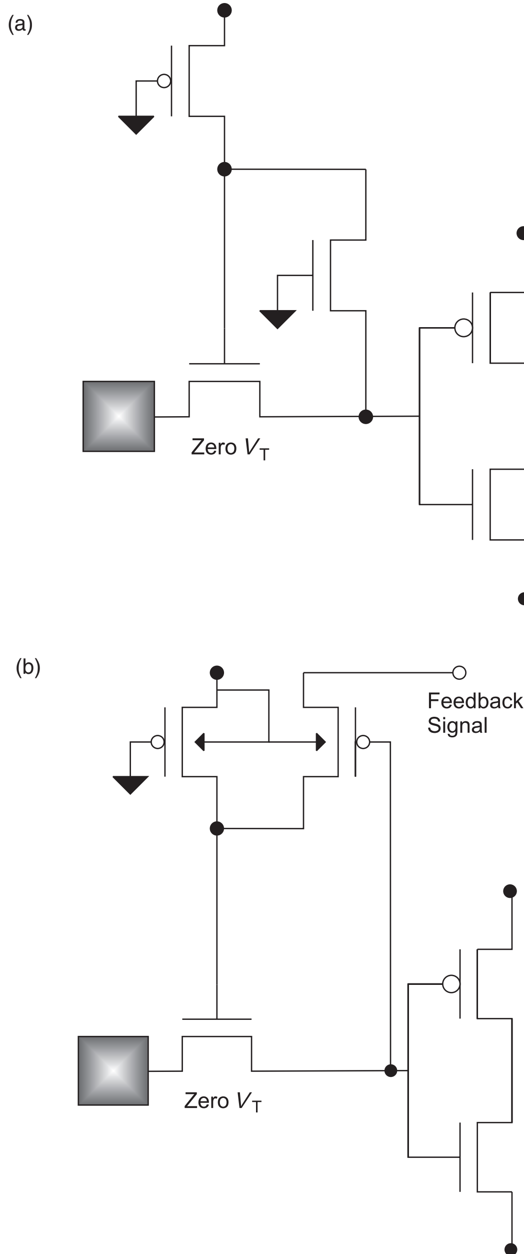

Figure 7.15 (a,b) Receiver network with zero V_T TG and dielectric over-voltage network

network introduces a current path for failure during ESD events. During ESD events, for the case that the power supply V_{DD} is grounded, the MOSFET (ZVT) device, the *n*-channel, and *p*-channel elements provide a current path to the referenced V_{DD} power supply. Experimental observations of the ESD testing results demonstrated MOSFET second breakdown of the ZVT, and the *n*-channel transistor, as well as damage in the *p*-channel MOSFET. Whereas

the resistive–divider network served as a good solution to minimize electrical over-voltage during functional operation from mixed voltage interfaces, overshoot, and undershoot, the presence of the resistor-divider solution lead to the ‘‘pinning’’ of the output of the MOSFET ZVT transistor, leading to failure of the ZPASS network. ESD protection can be improved by good ESD protection prior to the ZPASS network, or additional resistance in the ZPASS resistor–divider network to prevent the ‘‘pinning’’ during ESD test conditions.

7.6 RECEIVER CIRCUITS WITH BLEED TRANSISTORS

In receiver networks, noise and charge build-up on signal pads can initiate an undesired initial condition on an input pad or switching of the inverter circuit [13,14]. To avoid charge build-up, half- and full-pass TGs are used to reduce the charge sensitivity. MOSFET transistors which are normally ‘‘on’’ can be used as resistors to maintain the low logic ‘‘0’’ state when no intentional signal is applied. Minimum-width long-channel transistors can provide a low width-to-length ratio suitable as a resistance element. Typical width-to-length ratios can be 1:50 and 1:100 providing very high resistance and low current drive. Receiver networks can use a narrow-width long-channel *n*-channel or *p*-channel MOSFET whose gate is either electrically connected to the input node or the power supply rails (Figures 7.16 and 7.17). In the case of the narrow-width long-channel *p*-channel MOSFET structure, the MOSFET gate is electrically connected to the ground potential to be normally ‘‘on.’’ In the case of the narrow-width long-channel *n*-channel MOSFET structure, the MOSFET gate is electrically connected to the power supply voltage to be normally ‘‘on.’’ In either case, the electrical connections of these normally ‘‘on’’ elements can lead to ESD failures which involve the gate-to-diffusion electrical overstress; these elements will not undergo MOSFET second breakdown due to the long channels. For example, given an narrow-width long-channel *n*-type MOSFET whose gate is connected to the V_{DD} power supply, electrical overstress can occur between the MOSFET drain and the gate region.

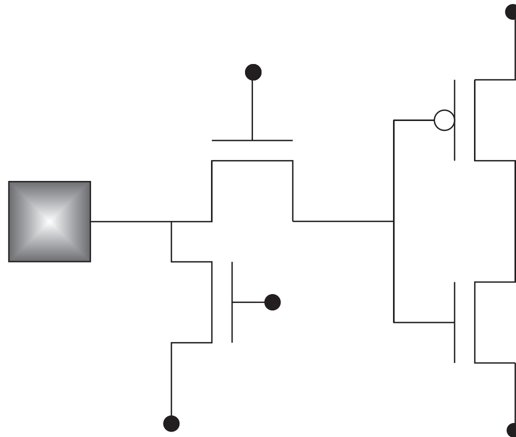

Figure 7.16 Receiver network with *n*-channel bleed transistors

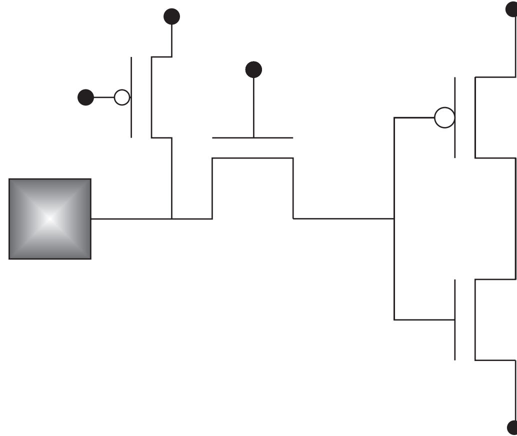

Figure 7.17 Receiver with *p*-channel bleed transistors

7.7 RECEIVER CIRCUITS WITH TEST FUNCTIONS

For functional testing, receiver networks are modified to allow the states of the receivers to be placed in various states. Test function are added by placing elements in a parallel with the signal path to avoid impacts to receiver performance. To avoid performance impacts, the elements are typically small, and hence vulnerable to ESD failure.

Figure 7.18 is an example of a test function network that is placed on an input signal node of a receiver. Two MOSFETs are placed in a series cascode between the input signal and the V_{SS} ground node. This network is placed in parallel to the half-pass MOSFET TG network. A first MOSFET has its gate electrically connected to the V_{DD} power supply voltage. The second MOSFET gate is connected to test functions. The test function is the closest network to the

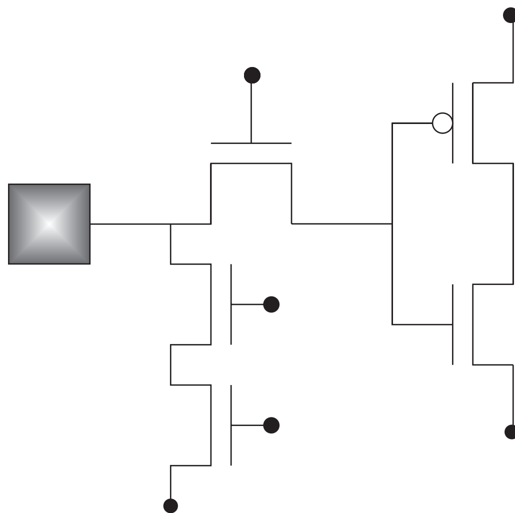

Figure 7.18 Receiver network with test functions

signal pad. During CDM testing, a failure mechanism was evident between the first MOSFET gate electrode and the MOSFET drain. When the V_{DD} is charged, and the input signal pad node is at a ground potential, the first MOSFET gate-to-drain overlap region leads to ESD failure.

In the ESD design of receiver networks, the following solutions can be applied to eliminate the failure of MOSFET test functions in receiver networks:

- Test functions should be placed after the half-pass MOSFET TG to avoid both HBM and CDM failures.
- Test functions connected to the power rails should introduce decoupling by placement of resistance elements in series with the MOSFET gate and source.
- Test functions can place resistive elements in series with the MOSFET drain to avoid electrical overstress in receiver networks.

7.8 RECEIVER WITH SCHMITT TRIGGER FEEDBACK NETWORKS

Receiver networks can introduce feedback elements which provide higher tolerance to noise. Schmitt trigger receiver networks introduce feedback elements to make receivers more tolerant to small input changes. A Schmitt trigger network introduces a hysteresis voltage where the forward and reverse voltage characteristics do not follow the same voltage transfer characteristic path. For the input characteristic, a higher input switching value is needed to switch the circuit when the input value is increasing. This state is referred to as a value of V^+. For the input characteristic, a lower input switching value is needed to switch the circuit when the input value is decreasing. This state is referred to as a value of V^-. The difference between the two states is defined as the hysteresis voltage

$$V_H = V^+ + V^-$$

Figure 7.19 shows an example of a receiver network with the Schmitt trigger feedback [15]. In the receiver network, the *p*-channel MOSFET pull-up and the *n*-channel MOSFET pull-down elements are split into a series cascode MOSFET structure. Two elements provide the MOSFET feedback. In the case of an *n*-channel pull-down stage, an additional Schmitt trigger feedback *n*-channel MOSFET circuit element is placed; an *n*-channel MOSFET source is connected between the two *n*-channel pull-down MOSFETs and its drain is electrically connected to the local V_{DD} power supply (e.g., or analog V_{DD}). The gate of the Schmitt trigger feedback element is connected to the output of the MOSFET receiver output stage. In the case of a *p*-channel pull-up stage, an additional Schmitt trigger feedback *p*-channel MOSFET circuit element is placed; a *p*-channel MOSFET source is connected between the two *p*-channel pull-up MOSFETs and its drain is electrically connected to the local V_{SS} power supply (e.g., or analog V_{SS}). The gate of the *p*-channel Schmitt trigger feedback element is connected to the output of the MOSFET receiver output stage.

For the receiver network, the two switching conditions can be expressed as [15]

$$V^+ = \frac{V_{DD} + V_{Tn}\sqrt{\dfrac{(W/L)_{n1}}{(W/L)_{nf}}}}{1 + \sqrt{\dfrac{(W/L)_{n1}}{(W/L)_{nf}}}}$$

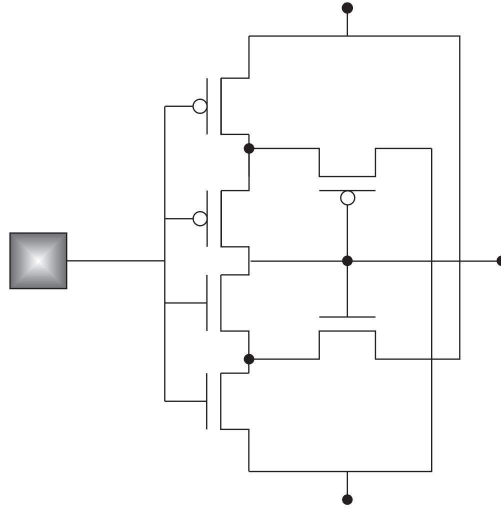

Figure 7.19 Symmetric receiver network with Schmitt trigger feedback elements

where the first width-to-length ratio $(W/L)_{n1}$ is the lowest receiver *n*-channel pull-down element, and the second width-to-length ratio $(W/L)_{nf}$ is the *n*-channel Schmitt trigger feedback element. The reverse trigger voltage is expressed as a function of the *p*-channel pull-up elements and the *p*-channel Schmitt trigger feedback element [15]

$$V^{-} = \frac{(V_{DD} - V_{Tn})\sqrt{\frac{(W/L)_{p1}}{(W/L)_{pf}}}}{1 + \sqrt{\frac{(W/L)_{p1}}{(W/L)_{pf}}}}$$

where the first width-to-length ratio $(W/L)_{p1}$ is the lowest receiver *p*-channel pull-up element, and the second width-to-length ratio $(W/L)_{pf}$ is the *p*-channel Schmitt trigger feedback element. A symmetric trigger voltage can be established using this receiver network where

$$V^{+} = \frac{1}{2}V_{DD} + \Delta V$$
$$V^{-} = \frac{1}{2}V_{DD} - \Delta V$$

where the hysteresis is given by

$$V_{H} = 2(\Delta V)$$

Given that the ratio of the MOSFET receiver stage to the Schmitt trigger feedback for the *n*-channel and the *p*-channel elements are the same, and assuming a threshold voltage for the *n*-channel and *p*-channel are equal in magnitude, it can be expressed as [15]

$$\Delta V = \frac{V_{DD}\left(1 - \sqrt{\frac{(W/L)}{(W/L)_{f}}}\right) + 2V_{T}\left(1 - \sqrt{\frac{(W/L)}{(W/L)_{f}}}\right)}{2\left(1 + \sqrt{\frac{(W/L)}{(W/L)_{f}}}\right)}$$

and

$$\sqrt{\frac{(W/L)}{(W/L)_{\mathrm{f}}}} = \frac{V_{\mathrm{DD}} - 2(\Delta V)}{V_{\mathrm{DD}} + 2(\Delta V) - 2V_{\mathrm{T}}}$$

The MOSFET receiver network is vulnerable from ESD events due to the Schmitt trigger feedback element in the case where the ESD networks are connected to the V_{DD} power rail. Additionally, where this receiver network is placed on an independent power rail, such as analog V_{DD} (e.g., AV_{DD}). ESD failure of Schmitt trigger networks and erratic switching behavior on ESD test systems were first noted. During HBM testing, an ESD diode network can discharge the current to the AV_{DD} power rail. As the ESD current flows to the AV_{DD} power rail, the AV_{DD} power rail voltage increases. As the voltage increases, MOSFET snapback occurs through the Schmitt trigger *n*-channel MOSFET feedback element and the *n*-channel MOSFET pull-down element. When the AV_{DD} power rail voltage reaches the voltage condition where the Schmitt trigger and the pull-down MOSFET undergo MOSFET second breakdown, the circuit output failure occurs. From the tester, failure may not be observed since there is no rupture of the MOSFET receiver gate insulator, but the operation of the MOSFET receiver network will not have the same hysteresis character and switching points.

As an ESD practice, feedback elements can lead to early ESD failure of networks. An ESD design practice to prevent failure can be as follows:

- *Buffering of feedback elements*: Buffer the feedback elements with series resistance to delay the turn-on.
- *Decoupling of feedback elements*: Decouple feedback elements from the power rails.
- *Alternate current paths to avoid feedback elements*: Establish alternative current paths for the ESD current.

ESD solutions exist which prevent the failure of the MOSFET receiver with the Schmitt trigger feedback elements during ESD events:

- Current-limit the flow of the ESD current to the Schmitt trigger MOSFET along the power bus or series impedance element.
- Provide the MOSFET width and lengths of the MOSFET Schmitt trigger element and pull-down element to allow for a high MOSFET second breakdown current magnitude.
- Provide ESD power clamps on the power rails which trigger prior to the turn-on of the Schmitt trigger MOSFET feedback and the MOSFET pull-down element.
- Provide a current path to alternate power rails when placed on an independent analog power rail.

In this implementation, the sizing of the MOSFET width-to-length ratio, and the relative size of the MOSFET Schmitt trigger elements and the MOSFET pull-up and pull-down elements all influence the hysteresis condition and the triggering point. As a result, co-synthesis of the trigger points, hysteresis condition, and the ESD protection levels are

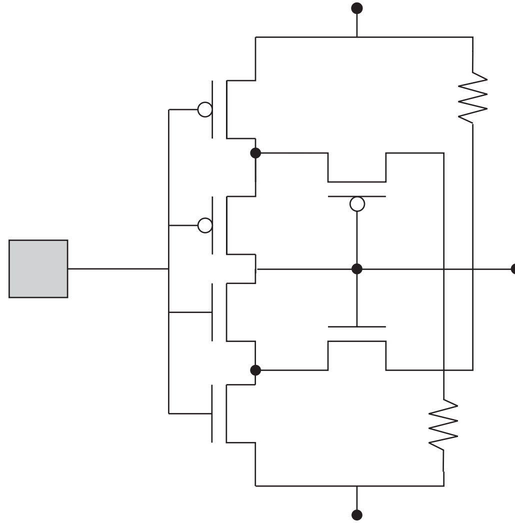

Figure 7.20 Modified Schmitt trigger network for ESD improvement

possible by evaluating the size of the MOSFET elements needed in the circuit implementation. Figure 7.20 highlights an ESD improvement in the Schmitt trigger network.

7.9 BIPOLAR TRANSISTOR RECEIVERS

7.9.1 Bipolar Single Ended Receiver Circuits

Receiver circuits are a common ESD sensitive circuit in Bipolar and BiCMOS technology. Bipolar receiver circuits typically consist of *npn* bipolar transistor configured in a common emitter configuration (Figure 7.21). For bipolar receivers, the input pad is electrically connected to the base contact of the *npn* transistor, with the collector connected to V_{CC} either directly or through additional circuitry. The *npn* bipolar transistor emitter is electrically connected to V_{SS}, or through a emitter resistor element, or additional circuitry.

In bipolar receiver networks, for a positive-polarity HBM ESD events, as the base voltage increases, the base-to-emitter voltage increases leading to forward biasing of the base–emitter junction. The base–emitter junction becomes forward active, leading to current flowing from the base to the emitter region. Typically in bipolar receiver networks, the physical size of the emitter regions are small. When the ESD current exceeds the safe operation area (SOA), degradation effects occur in the bipolar transistor. The bipolar device degradation is observed as a change in the transconductance of the bipolar transistor. From the electrical parametrics, the unity current gain cutoff frequency, f_T, decreases with increased ESD current levels. From a f_T–I_C plot, the f_T magnitude decreases with ESD pulse events, leading to a decrease in the peak f_T.

For a negative pulse event, the base–emitter region is reverse biased. As the voltage on the signal pad decreases, the base–emitter reverse-bias voltage across the base–emitter metallurgical junction increases. Avalanche breakdown occurs in the emitter–base metallurgical

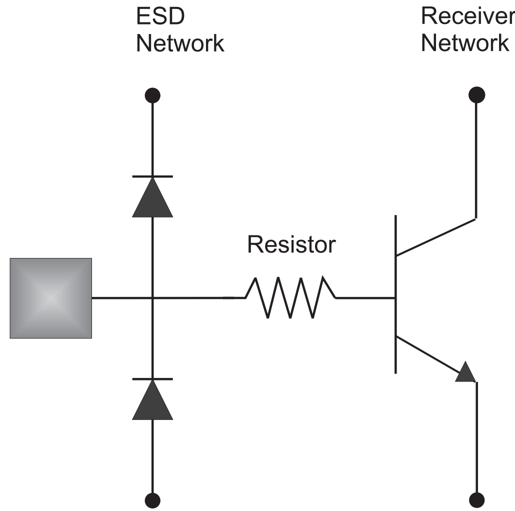

Figure 7.21 Bipolar receiver network

junction, leading to an increase in the current flowing through the emitter and base regions; this leads to thermal runaway and bipolar second breakdown in the bipolar transistor. The experimental results show that the negative-polarity failure level has a lower magnitude compared to the positive-polarity failure level.

One common ESD design solution used to provide improved ESD results in a single-ended bipolar receiver network is to place a *p–n* diode element in parallel with the *npn* bipolar transistor emitter–base junction (Figure 7.22). Using a parallel element, the *p–n* junction is placed such that the anode is electrically connected to the *npn* emitter, and the cathode is electrically connected to the *npn* base region; this ESD element serves as a bypass

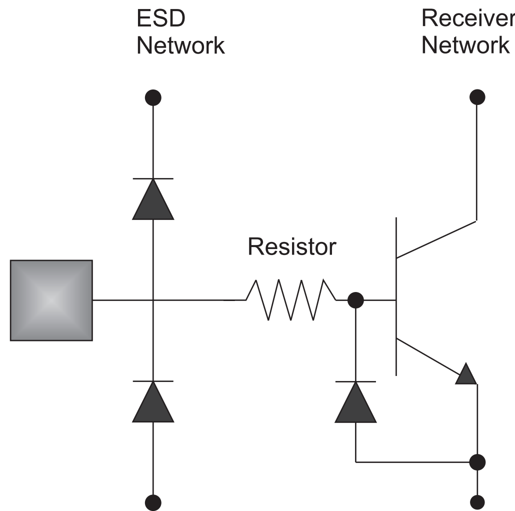

Figure 7.22 Bipolar receiver network with ESD diode

element avoiding avalanche breakdown of the *npn* base–emitter junction. The diode element is placed local to the *npn* transistor element to avoid substrate resistance from preventing early turn-on of the ESD diode element. Note that this element is analogous to the CDM solution used in CMOS receiver networks. For a bipolar transistor, it is serving for events from both the signal pad and potential events from the emitter electrode.

In radio frequency (RF) bipolar receivers, metal-insulator-metal (MIM) capacitors are used between the signal pad and the base electrode. For positive- or negative-mode polarity events, the MIM capacitor can fail due to dielectric degradation. Without ESD protection on the receiver network, the ESD failure levels of the receiver network will be limited by the MIM capacitor element. An ESD solution to prevent ESD failure in these RF bipolar receivers is to use a *p–n* diode element in parallel with the MIM capacitor element. The *p–n* diode element can be in a reverse configuration so that it serves as a parallel capacitor element, and does not allow a dc voltage to be transmitted between the signal pad and the bipolar receiver base element. The functional disadvantage of the *p–n* element is the impact of the effective quality factor "*Q*" of the capacitor element.

7.9.2 Bipolar Differential Receiver Circuits

Differential receiver networks are used to improve the signal-to-noise ratio in bipolar networks. Differential receiver networks use a differential pair of identical *npn* bipolar transistors in a common-emitter mode. For differential bipolar receivers, two input pads are electrically connected to the base contacts of the identical *npn* transistors, and the two emitters are connected together. Below the emitter connection, additional circuitry, a current source or a resistor element is commonly used (Figure 7.23).

One of the unique problems with differential receiver networks is pin-to-pin ESD failure mechanism. In ESD testing, we can apply an ESD pulse event to one of the two differential signal pads, using the second differential signal pad as the ground reference. In differential pair bipolar receiver networks, for a positive-polarity HBM ESD events, as the base voltage increases the base-to-emitter voltage of the first transistor leading to forward biasing of the base–emitter junction. The base–emitter junction becomes forward active, leading to current flowing from the base to the emitter region. For the second *npn* bipolar transistor, the base–emitter region is reverse biased. As the voltage on the first signal pad increases, the base–emitter reverse-bias voltage across the second transistor base–emitter metallurgical junction increases. Avalanche breakdown occurs in the emitter–base metallurgical junction, leading to an increase in the current flowing through the emitter and base regions; this leads to

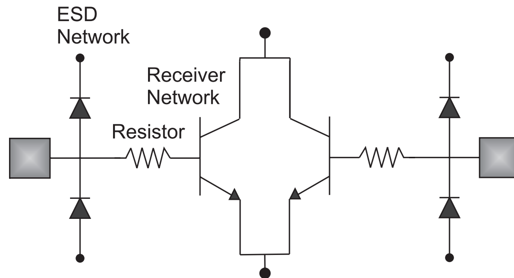

Figure 7.23 Bipolar differential pair receiver network

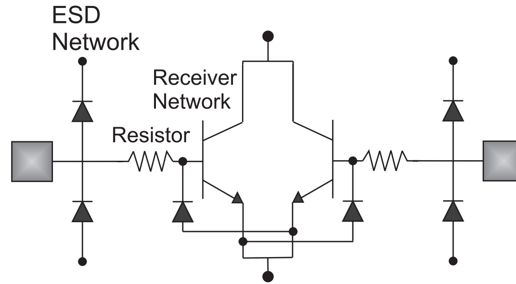

Figure 7.24 Bipolar differential pair with ESD protection to avoid pin-to-pin ESD failures

thermal runaway and bipolar second breakdown in the grounded second bipolar transistor of the differential pair. Note that the degradation of the second transistor prior to the first transistor can also lead to a differential offset hampering the matching of the two sides of the differential pair. It is possible that the failure criteria is associated with a *npn* mismatch prior to the ESD failure of either *npn* device.

An ESD design solution used to provide improved ESD results in a differential pair bipolar receiver network is to place a *p–n* diode element in parallel with the *npn* bipolar transistor emitter–base junction (Figure 7.24). Using a parallel element, the *p–n* junction is placed such that the anode is electrically connected to the *npn* emitter and the cathode to the base region. In this fashion, an alternate forward-bias current path is established between both sides of the differential pair. Second, another method is to introduce a back-to-back diode string between both sides of the differential pair. This has the advantage of allowing a higher current between both sides of the differential pair, but the disadvantage of asymmetry matching and capacitance loading performance degradation. Additionally, a dual-emitter structure can be utilized where the first emitter is for functionality and the second emitter is for ESD protection [34].

7.10 SUMMARY AND CLOSING COMMENTS

In this chapter, Chapter 7, receiver networks and ESD issues were discussed in fundamental CMOS and bipolar technology. The discussion focused on ESD implications of receivers as receiver networks evolved with technology generations and technology scaling. MOSFET scaling leads to an increase in complexity in receiver networks to address power supply scaling, threshold voltage scaling, MOSFET dielectric scaling and noise, as well as mixed signal interface environments. The transitions of the receiver networks lead to new ESD issues almost every technology generation. Additionally, feedback networks and pin-to-pin ESD issues were discussed in networks with hysteresis, feedback elements, and differential inputs became necessary. The focus of the chapter addressed how to build a better receiver network with an increased ESD robustness by modification of the non-performance impacted circuit elements. The concepts and design practices are transferable to both bidirectional networks and other similar receiver circuits.

Chapter 8, will address issues with SOI circuitry and ESD. Chapter 8, *SOI ESD Circuits*, addresses SOI circuits utilized in mainstream SOI application. The focus of the chapter will be on integration of the SOI ESD networks in SOI microprocessors. In the chapter, the

evolution of the SOI ESD networks with the power supply scaling will be self-evident; as the power supply was reduced, technology innovation and scaling improved the ESD robustness of the SOI ESD structure. ESD learning led to more scaled and aggressive designs and architectural tricks, and ESD fault recognition led to improved SOI product results. Applying ESD design practices, such as gate decoupling for the SOI-gated diode structures, and the addition of decoupling from the power supply, additional improvements continued. The concepts are useful in the understanding of bulk CMOS receiver networks as well.

PROBLEMS

7.1. Assume a receiver network consisting of a pad, an *n*-channel half-pass transistor, and an inverter circuit. Assume that the *n*-channel half-pass transistor breakdown voltage to substrate is lower than the gate oxide breakdown voltage. Given that the *n*-channel half-pass transistor has a MOSFET width *W*, and conductance to substrate of value *G* per unit micron, show the voltage response of the circuit.

7.2. Assume a receiver network consisting of a pad, an *n*-channel half-pass transistor, and an inverter circuit. Assume that the *n*-channel half-pass transistor breakdown voltage, V_{BR}, to substrate is higher than the gate oxide breakdown voltage, V_{OX}. Assume the MOSFET snapback voltage V_{t1} is less than the oxide breakdown voltage. What is the circuit response as a function of voltage?

7.3. Assume a receiver network consisting of a pad, an *n*-channel half-pass transistor, and an inverter circuit. Assume that the *n*-channel half-pass transistor breakdown voltage, V_{BR}, to substrate is higher than the gate oxide breakdown voltage, V_{OX}. Assume the MOSFET snapback voltage V_{t1} is greater than the oxide breakdown voltage. What is the circuit response as a function of voltage?

7.4. Assume a receiver network consisting of a pad, a full-pass transmission gate (*p*-channel and *n*-channel MOSFET of equal width), and an inverter network. As a positive ESD pulse is applied, derive the current as a function of voltage across the full-pass transmission gate assuming current flows through the receiver dielectric according to $C\mathrm{d}V/\mathrm{d}t$. Does the *n*-channel MOSFET undergo MOSFET snapback? What size should the *p*-channel MOSFET be in order to prevent *n*-channel MOSFET snapback in the full pass transistor network? Take into account the *p*-channel MOSFET as a diode-resistor element or *pnp* transistor.

7.5. Assuming a receiver network consisting of a pad, an *n*-channel MOSFET transmission gate, an inverter, and a *p*-channel MOSFET keeper feedback element of width *W*. Show the circuit schematic highlighting the parasitic diode formed between the *p*-channel MOSFET keeper drain and its corresponding *n*-well. Assuming an *n*-well resistance value associated with the width *W*, and *n*-well sheet resistance, and modeling the keeper network as an ideal diode and well series resistor, derive the current and voltage relations across the *n*-channel MOSFET transmission gate when the V_{DD} is grounded. What well-resistor value is needed to avoid the failure of the *n*-channel MOSFET half-pass transistor? Given that an additional resistor is placed

between the *p*-channel MOSFET keeper drain and the *n*-channel MOSFET half-pass node, what resistor value will prevent the MOSFET half-pass transistor from failing?

7.6. Given a receiver network consisting of a pad, an *n*-channel MOSFET transmisson gate, and a receiver network, list all the possible failure mechanisms and current paths to failure from HBM, MM, and CDM events.

7.7. Given an SOI receiver network consisting of a pad, an *n*-channel SOI MOSFET transmission gate, and a SOI receiver network, list all the possible failure mechanisms and current paths to failure from HBM, MM, and CDM events. Evaluate positive and negative polarity to both V_{DD} and V_{SS} . How does this differ from the bulk implementation? Which is more robust? How does the charge get back to the input pad for CDM mechanisms?

7.8. Given an SOI ESD network and an SOI receiver network, consisting of a pad, a SOI double-diode network (whose gate is connected to their respective cathode nodes), a SOI *n*-channel pass transistor and a SOI receiver network. Evaluate positive and negative polarity to both V_{DD} and V_{SS}. List all possible failure mechanisms, and current paths to failure from HBM, MM, and CDM events.

7.9. In SOI technology, the substrate region below the buried oxide is electrically disconnected from the thin silicon film above the buried oxide region. Does providing an electrical contact between the substrate and the substrate power rail make CDM mechanisms better or worse? How will the failure mechanisms change?

7.10. Assume a receiver network with a *n*-channel zero-threshold voltage transmission gate between the pad and the inverter. What is better for ESD—a zero V_T device or a non-zero V_T device?

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8 SOI ESD Circuits and Design Integration

8.1 SOI ESD DESIGN INTEGRATION

In this chapter, we will focus on ESD protection in silicon-on-insulator (SOI) technology. The focus will be on demonstrated SOI implementations, as well as the future SOI ESD solutions.

SOI technology remained outside the mainstream semiconductor chip applications for many years, with the majority of interest in military, space, and radio frequency (RF) applications [1]. In the 1990s, SOI entered the mainstream arena as an evolutionary extension of mainstream CMOS technology [1–11]. After 10 years of research and development in IBM, the first microprocessor was implemented into a mainstream product. In that period, from 1993 to 2000, the focus was to provide ESD solutions to mainstream SOI technology. In that time frame, approximately seven SOI CPU chips were used as prototypes to mainstream SOI CPU chips, where the ESD protection devices, circuits, and architectures were developed [18–28,33–38,42–45]. During that period, there were parallel efforts in measurement of ESD robustness of SOI devices and structures [12–17]; these publications focused on device response, but did not address the ESD design integration issues and the focus on protection of SOI receiver and off-chip driver (OCD) circuits. Since that time, SOI has an increasing role in mainstream technology used for microprocessor and logic applications, with new announcements of efforts annually.

As technologies scale below 0.1-μm technology generation, MOSFET issues, such as short channel effects (SCE) control, gate resistance, channel profiling, hot electrons, and negative bias temperature instability (NBTI) continue to challenge device engineers designing in bulk CMOS technology. Additionally, CMOS latchup and ESD continue to be an issue in bulk CMOS applications. In bulk CMOS applications, CMOS latchup issues are increasing from cable discharge events (CDE) and system-on-chip (SOC) integration issues. SOI technology provides low leakage current, low-capacitance MOSFETs and resistor elements, good sub-threshold *I–V* characteristics, good noise isolation, and does

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not have bulk CMOS latchup issues. With partially depleted (PD) SOI technology with body contacts, floating body effects and ESD concerns have been addressed.

In this chapter, the focus will be on ESD SOI design and design integration. ESD structures and circuits will be shown, with an emphasis on ESD design architecture and synthesis with the power architecture of mainstream SOI CPU implementations.

8.1.1 SOI Versus Bulk CMOS ESD Design Advantages

SOI provides advantages for ESD design compared to bulk CMOS technology. The lack of a vertical diode structure was perceived as an ESD design disadvantage, but many of the ESD design advantages implementing an actual design in SOI technology were not understood [12]. These advantages can best be understood by implementing a bulk CMOS ESD design into SOI technology, and evaluating the design rule and design rule checking advantages. SOI has many layout design advantages for ESD design [11,19–24]. The following list comprise some of the ESD design advantages when designing in SOI technology:

- No p^+ substrate contact guard rings are required.
- No *n*-well guard rings are required.
- *n*-well-to-*n*-well space not required.
- No triple well edge isolation region.
- Diode areas can be of minimum width, and perimeter-to-area ratio can be higher than equivalent bulk implementations.
- MOSFET source and drain area can be of minimum width.
- No silicide-to-isolation edge requirements.
- No contact-to-isolation edge requirement.
- No salicide junction penetration issues in MOSFET source and drain, or diode structures.
- No parasitic vertical *pnp* formed between the *p*-channel MOSFET, *n*-well, and p^- substrate.
- No parasitic vertical or lateral *npn* formed between the *n*-channel MOSFET, *p*-well, and *n*-well.
- No *p*-channel MOSFET-to-*n*-channel MOSFET space rules.
- No latchup p^+/n^+ space rules required.
- No parasitic interaction between successive circuit elements or stages in the ESD design.
- SOI MOSFET body regions are electrically decoupled from the power supply rail.
- SOI MOSFET body region are electrically decoupled from the ground power rail.
- SOI MOSFET gate is electrically isolated from the semiconductor substrate by the buried oxide (BOX), leading to reduced charged device model (CDM) failures due to SOI MOSFET gate oxide pin-holes.
- SOI MOSFET decoupled MOSFET body regions allow for dynamic threshold design.

- SOI MOSFETs *n*-channel MOSFET and *p*-channel MOSFET provide circuit design symmetry (e.g., which is not possible in a dual-well CMOS design due to asymmetry relative to the ground substrate).
- SOI ESD structures can be constructed in the thin silicon region, or below the SOI BOX region.

8.1.2 SOI Versus Bulk CMOS ESD Design Layout Disadvantages

There are some ESD design disadvantages in SOI design, which are as follows:

- SOI thin film scaling can lead to wider structures.
- SOI structures can lead to higher self-heating and a lower power-to-failure.
- SOI fully depleted ESD design will have limited ability to discharge ESD current.
- SOI structures typically have a SOI MOSFET gate structure increasing capacitance and leading to dielectric failure mechanisms.
- SOI buried resistor (BR) ballast elements have no negative discharge capability to the substrate.
- ESD currents flow through limited electrical connections leading to earlier metallization failures (e.g., the majority of the SOI semiconductor chip is isolated to the substrate).

8.1.3 SOI Design Layout: T-Shaped Layout Style

To address the ‘‘floating body’’ condition of a SOI MOSFET, a MOSFET body-contact can be placed to control the electric potential of the SOI MOSFET body. The SOI MOSFET body contact adds an additional contact to the MOSFET structure (e.g., one additional contact beyond the bulk-MOSFET device). The concern of the SOI MOSFET body contact is twofold: first, the addition of the MOSFET body contact impacts chip area; and second, it impacts remapping of bulk-CMOS to SOI technology. SOI MOSFET body contact can be formed by defining a T-shape region of silicon on the SOI BOX region [1]. The MOSFET source and drain are formed by using a dielectric and polysilicon gate structure. The SOI MOSFET polysilicon gate structure is contacted on one side that extends from beyond the SOI MOSFET source and drain, where an electrical MOSFET gate contact is placed on the gate structure. On the opposite side, the SOI polysilicon MOSFET gate structure extends past the SOI MOSFET source and drain definition edge, but only partially to the end of the T-shaped silicon region to allow for formation of the SOI MOSFET body-contact. A SOI MOSFET body contact region is formed by a dopant implant in the silicon region, followed by an electrical contact. The region under the contact is doped with the same dopant polarity as the channel region, but of a higher doping concentration. The construction of the MOSFET gate, source, drain, and body forms an ‘‘H-shaped’’ structure (e.g., a T-shaped silicon region domain) (Figure 8.1).

To provide ESD protection in SOI technology, one of the concerns was the lack of a vertical diode structure for electrical discharge [12]. The introduction of the MOSFET body

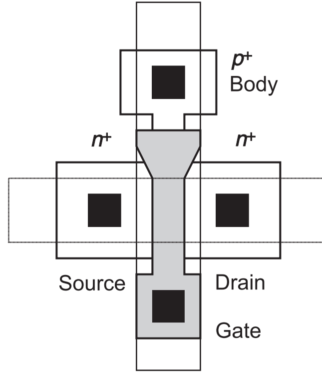

Figure 8.1 H-shaped SOI MOSFET with SOI MOSFET body contact

contact, although it was a functional and layout design area and remapping concern, is an advantage for ESD protection. The introduction of the SOI MOSFET body allows for the ability to provide a lateral *p–n* diode structure [20].

Using the T-shaped silicon domains, a SOI lateral diode structure can be formed [20]. For example, using a *p*-channel SOI MOSFET device, the SOI MOSFET source and drain region can serve as the anode, and the SOI MOSFET *n*-type channel and body can serve as the cathode. Using an *n*-channel SOI MOSFET device, the SOI MOSFET source and drain region can serve as a diode cathode, and the SOI *p*-channel MOSFET can serve as the anode. Since both the *p*- and *n*-channel SOI MOSFET bodies are disconnected from the well regions and the substrate, the electrodes can be changed and connected to input pads, power rails, or ground connections to form diode structures. In these cases, the SOI MOSFET gate structures are connected in fashion to avoid dielectric failure during ESD testing.

Figure 8.2 shows an example of the SOI MOSFET design layout for a SOI double-diode circuit that utilizes H-shaped (or T-shaped) SOI MOSFETs in a diode form [20]. Using both a *p*- and an *n*-channel SOI MOSFET, the *p*-channel SOI MOSFET can serve as a ‘‘SOI diode’’ to the power supply rail, and the *n*-channel SOI MOSFET can serve as a ‘‘SOI diode’’ to the ground power rail. The SOI MOSFET layout can be wired across both the

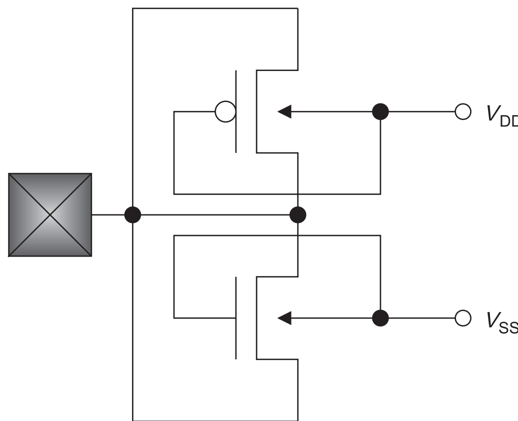

Figure 8.2 SOI double-diode ESD network using CMOS T-shaped SOI MOSFETs with body contacts

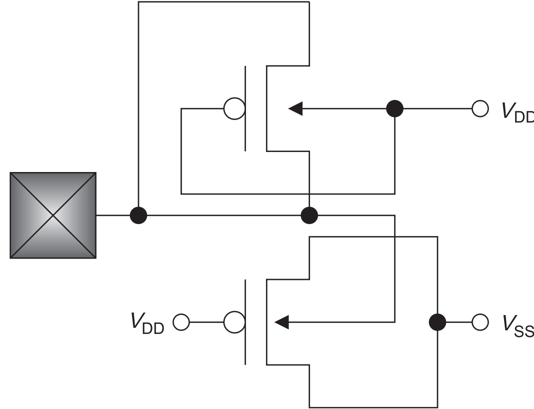

Figure 8.3 PMOS-defined SOI double-diode ESD network using T-shaped body-contacted SOI transistors

SOI *n*- and *p*-channel MOSFETs electrically connecting the MOSFET source and drain regions. The body and gate contacts can be electrically connected to the respective power supply rails.

An SOI ESD double-diode network can be formed using only SOI *p*-channel MOSFET body-contacted devices. A PMOS implementation can use an SOI *p*-channel MOSFET source and drain as the anode of the SOI MOSFET to the power supply voltage, and a second SOI *p*-channel MOSFET whose SOI MOSFET body contact serves as the anode for the diode to the substrate power rail [20] (Figure 8.3).

An SOI ESD double-diode network can be formed using only SOI *n*-channel MOSFET body-contacted devices. An NMOS implementation can use an SOI *n*-channel MOSFET *p*-type body that serves as the anode to the power supply voltage, and a second SOI *n*-channel MOSFET whose SOI MOSFET source and drain serves as the cathode for the diode to the substrate power rail (Figure 8.4).

ESD design considerations utilizing the T-shaped SOI MOSFETs with local body contacts are as follows:

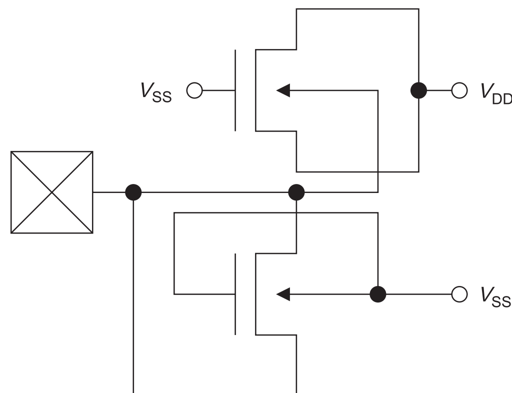

Figure 8.4 NMOS-defined SOI double-diode ESD network using T-shaped body-contacted SOI transistors

- A local SOI MOSFET body contact is needed to avoid lateral resistance effects along the SOI MOSFET channel.
- The SOI MOSFET length should be of the order of the SOI MOSFET width for each unit.

These ESD design considerations limit the effectiveness to use these structures for large SOI ESD diode structures. It is also found that the ability to produce area-compact ESD designs with the T-shaped local body contact structures [20].

8.1.4 SOI Design Layout: Mixed-Voltage Interface (MVI) T-Shaped Layout Style

In SOI ESD design, mixed-voltage interface (MVI) circuits can be constructed using the SOI MOSFET with the body contact [20]. With the SOI MOSFET body contact structure, the SOI MOSFET can be used in a diode configuration for SOI protection networks. The SOI MOSFET body contact can be formed by defining a T-shaped region of silicon on the SOI BOX region. The MOSFET source and drain are formed by using a dielectric and polysilicon gate structure. The SOI MOSFET polysilicon gate structure is contacted on one side that extends from beyond the SOI MOSFET source and drain, where an electrical MOSFET gate contact is placed on the gate structure. On the opposite side, the SOI polysilicon MOSFET gate structure extends past the SOI MOSFET source and drain definition edge, but only partially to the end of the T-shaped silicon region to allow for formation of the SOI MOSFET body-contact. A SOI MOSFET body contact region is formed by a dopant implant in the silicon region, followed by an electrical contact. The region under the contact is doped with the same dopant polarity as the channel region, but of a higher doping concentration. The construction of the MOSFET gate, source, drain, and body forms an ‘‘H-shaped’’ structure (e.g., a T-shaped silicon region domain).

Figure 8.5 shows a mixed-voltage SOI diode string using SOI MOSFETs with body contacts [20]. Using a *p*-channel SOI MOSFET structure, the *n*-type SOI MOSFET body can

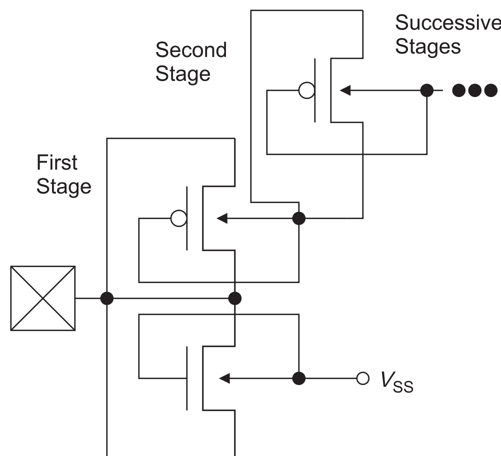

Figure 8.5 SOI ESD diode string network using a SOI MOSFET with body contact

serve as the SOI "diode" cathode structure. For negative-polarity ESD discharge events, an *n*-channel body-contacted SOI MOSFET can be placed in a diode configuration, where the SOI MOSFET body serves as the cathode. For positive polarity ESD discharge events, body-contacted *p*-channel SOI MOSFET can be formed in a "diode configuration" between the input pad and the power supply.

Mixed-voltage SOI ESD diode strings formed using T-shaped body-contacted SOI MOSFET have advantages and disadvantages comparing to bulk CMOS implementations:

- SOI ESD diode strings do not have parasitic leakage amplification issues (e.g., bulk CMOS vertical *pnp* elements form a common collector leakage amplification).
- SOI ESD diode strings do not have a vertical *pnp* current discharge path to the substrate.
- SOI ESD diode strings are not involved in latchup events.
- SOI ESD diode strings using T-shaped body-contacted SOI MOSFETs in diode configuration have poor layout design efficiency.
- SOI ESD diode strings using T-shaped body-contacted SOI MOSFETs in diode configuration have high-series resistance.

In SOI ESD design, there is a lack of a vertical *pnp* element and the decoupling of the successive stages from the semiconductor substrate. First, without the vertical *pnp* parasitic element, Darlington common collector leakage amplification does not occur. Second, there is no current injection to the substrate and hence the current must flow through the complete series diode string (e.g., which is not true in bulk CMOS implementation). Third, without the vertical current injection, there are no concerns of CMOS latchup associated with the series diode string network. Unfortunately, this SOI design style can lead to a high SOI ESD diode series resistance. Figures 8.6 and 8.7 show the *I–V* characteristics of the ESD diode string

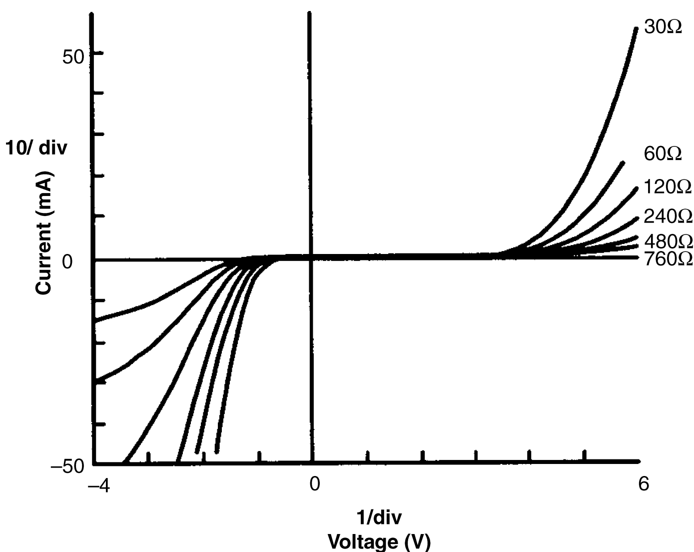

Figure 8.6 SOI ESD diode string *I–V* characteristic

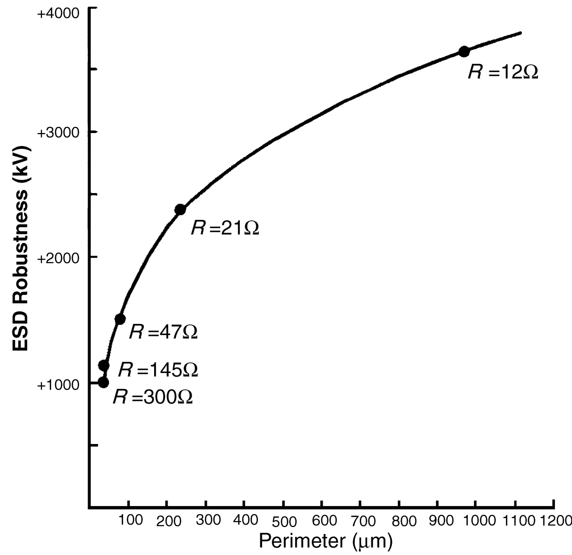

Figure 8.7 ESD HBM results of a SOI body-contacted T-shaped device diode string network as a function of the total design width

and the ESD HBM results, respectively. Figure 8.6 shows that high diode series resistance occurs with the series elements. Figure 8.7 also shows that as the perimeter is increased toward 1000 microns, the ESD results improve in the structure. Unfortunately, the size of the element and the physical area are not desirable.

Using the body-contacted SOI MOSFET structures, ESD diode strings were formed using five elements in series for a 5–2.5 V mixed-voltage interface in a 0.25-μm MOSFET channel length SOI CMOS technology [20]. With the perimeter of 30 μm, the resistance was 500 Ω; HBM ESD results only achieved 1.0 kV prior to structure failure. With a 960 μm perimeter, the resistance was reduced to 24 Ω, and a 3.5 kV HBM level was achieved.

Experimental results in this technology generation demonstrate that the physical area and the series resistance magnitude are too high for suitable ESD structures. Hence, it is advised not to use the T-shaped SOI-body-contacted elements when using in a series configuration unless a high perimeter can be utilized. Whereas this design layout and structure may be limited for input node circuitry, such circuits can be utilized between ground power rails, between V_{DD} power rails, V_{DD}-to-V_{SS} power rails, and other ESD embodiments.

Table 8.1 SOI ESD diode string implementation design and ESD robustness

Perimeter	Resistance (Ω)	ESD HBM level (kV)
30	500	1.0
60	272	1.1
120	90	1.5
240	80	2.3
480	48	3.0
960	24	3.5

8.2 SOI ESD DESIGN: DIODE DESIGN

Another method of forming a SOI diode structure for ESD design is constructing a lateral polysilicon gated diode structure [18–19,21–24]. Using the source and drain implants from a *p*-channel MOSFET and an *n*-channel MOSFET, as well as the MOSFET gate dielectric and gate stack structure, a lateral SOI gated diode structure is constructed. The layout and design was discussed in the prior chapter on SOI ESD structures (Chapter 5). In partially depleted SOI (PD-SOI), the source/drain features are defined using shallow trench isolation (STI), which abuts the silicon dioxide (SiO_2) BOX. A salicide film is formed on the source/drain junctions. In the formation of the lateral SOI diode structure, the width of the mask must allow the ability to align and be placed on the SOI MOSFET polysilicon gate structure to allow for the formation of the two sides of the lateral SOI gated diode structure. Figure 8.8 shows an example of the SOI lateral gated diode structure.

In an SOI lateral gated diode ESD network, because of the decoupling from the substrate potential, the same diode structure can be used for the two ESD diodes [11,21–23]. The same physical structure can be used for the ESD diode between the input and the V_{DD} power supply, and between the input pad and the V_{SS} power supply rail. Figure 8.9 shows the SOI ESD double-diode network. The first observation is the distinction between the bulk CMOS and this network, which is the presence of the SOI MOSFET gate structure. In the SOI double-diode ESD gate structure, as shown, the gate structure is electrically connected to the n^+ cathode region of the lateral $p^+/n^-/n^+$ diode structure.

Because of the symmetry, the identical ESD SOI lateral diode design element can be used to address both the positive and the negative HBM ESD events. In the design, this is achieved by electrical connection of the anode for one diode and the cathode for the second diode; these elements are then electrically connected to the corresponding power rails. This provides the following ESD design practice advantages:

- Optimization of a single element: Only one diode element is required for ESD design optimization and modeling.
- Symmetry of layout and design: The use of a single element allows for good layout and design symmetry spatially, which provides layout advantages.
- Utilization for positive and negative polarity events: The ESD results for both positive and negative polarity are similar due to the use of a single element type and the natural symmetry in the CMOS circuitry itself.

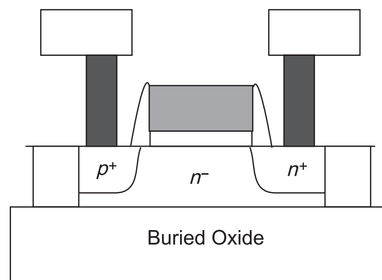

Figure 8.8 SOI lateral gated diode structure

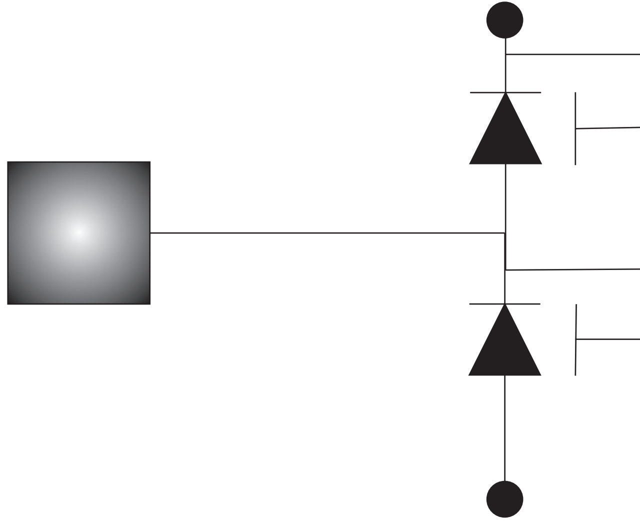

Figure 8.9 ESD double-diode input circuit for SOI technology

In the ESD design optimization, only one diode element is required for optimization, whereas in bulk CMOS, the asymmetry in dual-well CMOS leads to an asymmetry in the ESD diode solutions. For example, in single- and dual-well CMOS, a p^+/n-well diode is used for positive polarity events, and an n-well diode is used for negative polarity events; this requires optimization of both structures as well as two models.

In SOI, the ability of using one element type also leads to a symmetrical design layout as well. The use of a single element allows the changing of the metallization-to-contact configuration. The same element can be utilized by changing which node is electrically connected. Hence, no unique SOI ESD feature issues will occur.

In SOI, the ability to use a single element provides an equal ESD robustness of the physical element. Experimental results show that when the electrodes are interchanged and the ESD pulse polarity is switched, the identical result occurs. As a result, for human body model (HBM) positive and negative polarity events, the ESD robustness will be equivalent if the failure limitation is the ESD structure. Second, for machine model (MM) events, as a result of the positive and negative oscillation, this implementation will allow an equivalent response to both polarities.

When mapping ESD networks from bulk STI-bound diodes to SOI ESD networks, the STI is eliminated between the p^+ anode and the n^+ cathode, and a polysilicon gate structure is used to define the anode and cathode regions. The bulk implementation designs typically consisted of a high-perimeter diode structure. The mask to define the p^+ and n^+ implants must be placed over the polysilicon gate structure. In this fashion, the polysilicon-bound diode structure has a polysilicon film with two different dopant types and work functions along the device channel length [18,19,21–23]. With the placement of this structure on a BOX, the STI abuts the BOX film, isolating the polysilicon diode structure from adjacent structures.

In the remapping of a bulk CMOS diode design into a SOI technology, the SOI design optimization can be achieved by the following ESD design remapping design changes:

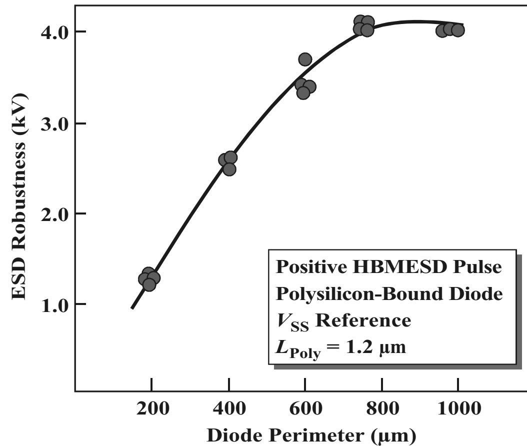

Figure 8.10 ESD results of a ESD polysilicon gated diode structure as a function of polysilicon gate perimeter ($L_{poly} = 1.2$ μm)

- *n*-well guard rings and related guard ring space ground rules are eliminated.
- p^+ substrate contact rules and guard rings are eliminated.
- *n*-well -to-substrate diode elements are to be eliminated.
- *n*-well to *n*-well ground rules are eliminated.
- n^+ to substrate diode elements are eliminated.
- n^+ ground rules are eliminated.
- $p^+/n^-/n^+$ diode element: p^+ anode diffusion width can be reduced to minimum contacted width.
- $p^+/n^-/n^+$ diode element: n^+ cathode diffusion width can be reduced to minimum contacted width.
- $p^+/n^-/n^+$ diode element: MOSFET halo is eliminated.
- $p^+/n^-/n^+$ diode element: STI shape between p^+ and n^+ is eliminated and replaced with gate structure.
- $p^+/n^-/n^+$ diode element perimeter increased for both positive and negative diode structures.

In a 0.25-μm SOI technology, the lateral polysilicon diode structure was studied as a function of the SOI diode perimeter and the polysilicon channel length [20]. Figure 8.10 shows the ESD robustness of a polysilicon-bound gated diode structure as a function of polysilicon perimeter. HBM results shows that the ESD results improve linearly with increasing diode perimeter with a design L_{poly} of 1.2 μm. Figure 8.11 shows the HBM ESD results as a function of polysilicon length for an 800-μm perimeter diode structure.

In a high-pin-count high-performance SOI chip, the SOI ESD network size is modified to evaluate the ESD robustness as a function of perimeter size [21–24]. This was completed by

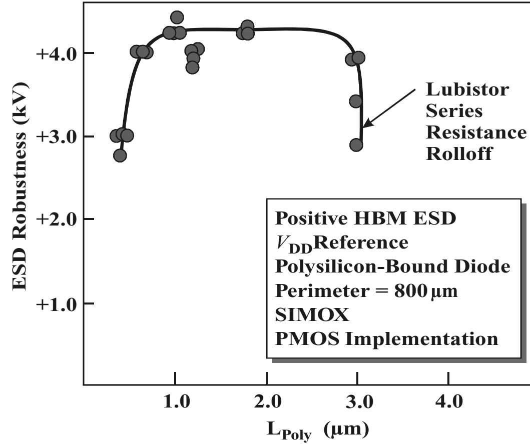

Figure 8.11 ESD results of a ESD polysilicon gated diode structure as a function of polysilicon gate length for a 800-μm perimeter diode structure

using a multi-finger SOI diode structure. The structure consisted of a two-, four-, and seven-finger diode structure, where each finger has a perimeter of 68 µm. Figure 8.12 shows a cross-section of the seven-finger SOI diode structure. The SOI ESD network has local *W M*0 bar interconnects placed along the complete length of the p^+ and n^+ contact regions. This provides low electrical and thermal resistance on the diffusion areas. The local *M*0 *W* interconnect is contacted with *W* contacts and connected to the first-level *M*1 Ti/Al/Ti metallurgy. The *M*1 interconnects are then connected to the *M*2 copper interconnects. Figure 8.13 shows an enlargement of the SOI ESD structure. Since there is no ESD advantage for the vertical p^+ anode and n^+ cathode areas, the structure was designed to minimum ground-rule spacings between the *W M*0 interconnect, gate dimensions, and overlay tolerances. This allows for high-perimeter diode designs in a small physical silicon area. The polysilicon ring forms the gate structure with the gate contact landing over the STI isolation, as can be seen in Figure 8.14.

Figure 8.15 shows the ESD results of peripheral circuits as a function of ESD perimeter. The OCD circuitry consists of a single *n*-channel MOSFET pull-down and single *p*-channel MOSFET pull-up transistor. The circuitry is resistor-ballasted using BR elements. The series

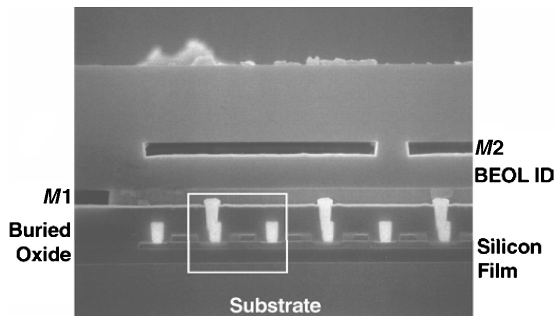

Figure 8.12 Cross-section of an SOI ESD diode structure

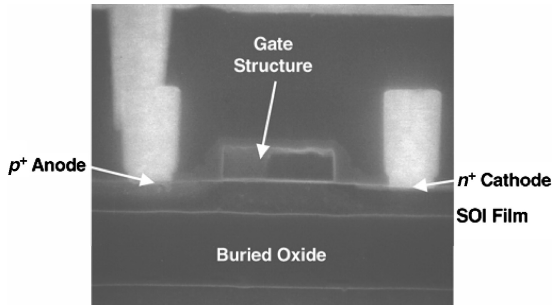

Figure 8.13 Cross-section of a lateral polysilicon-gated-SOI ESD diode structure

BR elements are adjusted in resistance value dependent on the interconnect length and resistance for I/O cell impedance matching. HBM ESD results of 4 kV are achieved with the 169 µm two-finger diode structure. ESD results increased with increasing p^+ anode perimeter for both the 338- and 591-µm structures. ESD results higher than 8 kV were achieved using the 591-µm diode structure [23,24].

Figure 8.15 also shows the ESD results into receiver networks. The test receiver consisted of a NFET pull-down test mode network in parallel with the receiver gate. ESD measurement results increased with the structure size for both the positive and negative test modes. The ESD results indicate that neither the SOI receiver network nor the BR resistor-ballasted driver circuitry limited the ESD robustness of the SOI technology. Failure analysis demonstrated in all three ESD cases that the ESD failure mechanism occurred in the ESD network between the p^+ anode and cathode. From this work, an equivalency of 23.8 V/µm diode is achieved with the smallest two-finger ESD design, and the seven-finger structure shows an equivalency of 14.2 V/µm (the actual scaling slope shows 11 V/µm scaling) in a high-pin-count high-performance chip. Our work shows that the scaling to the 0.12-µm L_{eff} technology has demonstrated significant improvement over the prior generations [23,24].

Figure 8.16 shows the ESD distribution for the three different-size ESD designs. The I/O design was optimized to tradeoff ESD robustness versus capacitive loading effect of the ESD network, where it was chosen to use the four-finger SOI structure, which provided minimal capacitance loading effects yet maintained ESD robustness well over 4 kV [23,24].

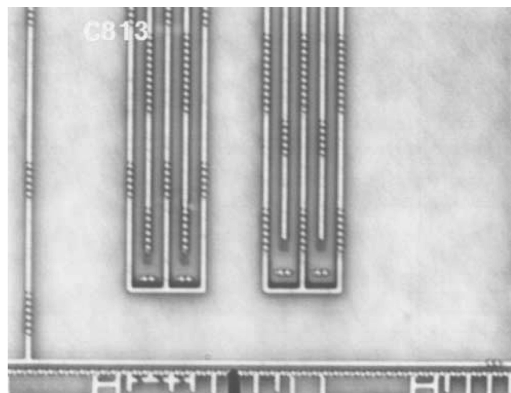

Figure 8.14 Top view of the SOI ESD network

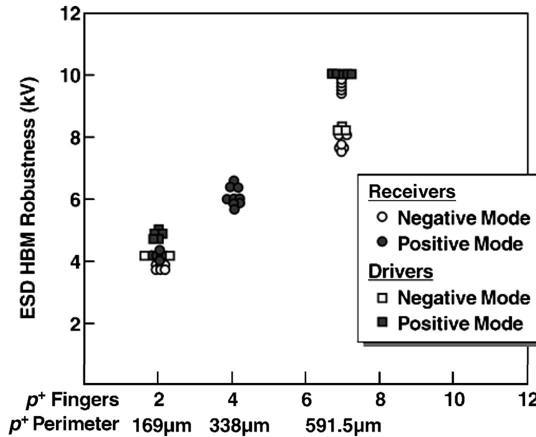

Figure 8.15 ESD results of SOI ESD network with OCD and receivers in a 1000-pin high-performance chip, where the different ESD design perimeters were tested

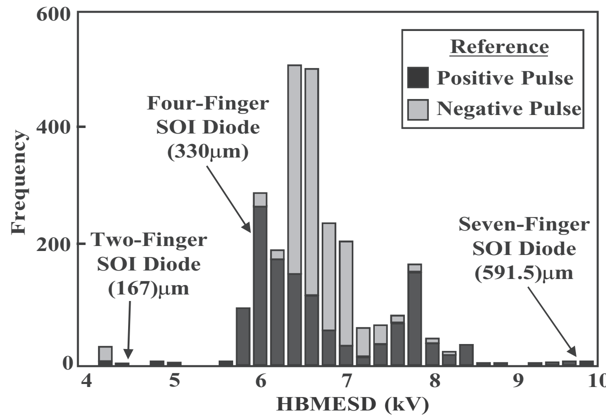

Figure 8.16 Distribution of ESD results for three different perimeter SOI ESD designs

8.3 SOI ESD DIODE DESIGN: MIXED VOLTAGE INTERFACE (MVI) ENVIRONMENTS

SOI ESD design must address MVI applications, when the SOI CPU must interface with higher power supply voltages of older technologies. SOI semiconductor chips allow the introduction of multiple power pins where the external I/O power rail exceeds the native power supply voltage. The implementation is dependent on whether the SOI chip must receive and transmit the higher voltage, or just receive the higher voltage state on the peripheral I/O [21–24].

SOI ESD design practices for mixed-voltage applications can be as follows:

- Single power rail architecture: SOI diode string from input to V_{DD}.
- Dual power supply rail architecture: SOI double-diode to V_{CC}, and a SOI bidirectional diode string between V_{CC} and V_{DD}.

In the first case, the second power supply is not utilized and the network has a series of diodes between the input pad to the native power supply voltage.

In the second case, the higher power rail is contained on-chip, and the ESD network is connected to the higher power pin. Additionally, a series of diode elements are placed between the V_{CC} and V_{DD} power rails, as well as a return diode element. In this SOI chip architecture, the ESD network can discharge to both the power rails, as well as provide ESD protection between the two power rails.

As an example, a first application for a 5.0 V/2.5 V interface SOI chip used a SOI double-diode element between the input pad, and placed seven SOI diodes between the two power supply. In this fashion, ESD protection was verified between the 5.0- and 2.5-V power supplies, and between the input pins to all power rails.

As a second example, ESD protection networks were constructed in a 2.5-V power supply 0.20-μm CMOS technology generation chip. In the 0.20-μm L_{eff} technology, deep extension implants were added to the shallow high doped drain implants to maintain V_T roll-off characteristics. In SOI technology, extension implants reduce the emitter and collector area for the lateral bipolar device; this reduces the bipolar current gain and improves short channel effects. The source/drain junctions use a $TiSi_2$ salicide film to reduce the diffusion sheet resistance. The technology supports a 5.0-nm oxide thickness. Figure 8.17 shows the SOI lateral gated diode with abrupt and extension implant drain structures. In this 0.20-μm technology, lateral polysilicon-gated SOI diodes demonstrated an ESD (HBM) robustness level of 8.0 V/μm, which was superior to the ESD robustness of the equivalent structure in the 0.25-μm L_{eff} technology that used abrupt junctions. The extension implant dose was significantly higher than that used in the abrupt 0.25-μm L_{eff} technology [23,24].

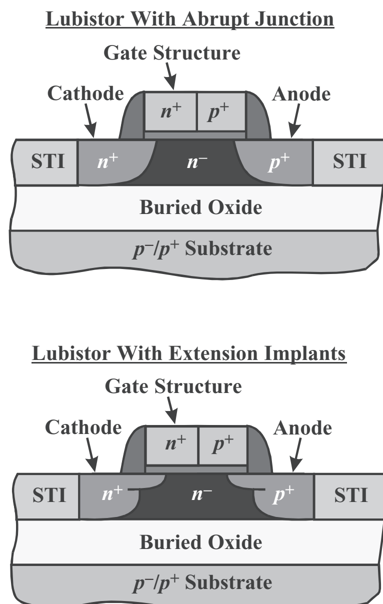

Figure 8.17 Cross-section of an SOI lateral gated diode with abrupt and extension implant drain structures

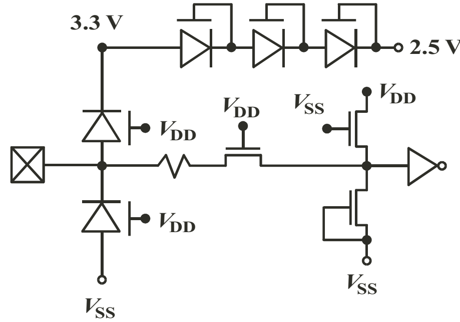

Figure 8.18 SOI ESD circuitry and receiver network

A 250-MHz RISC-based microprocessor was designed in bulk CMOS technology in a 16 × 16 ball-grid-array package. The mixed-voltage application required 3.3 V tolerant I/O networks with a 2.5-V core voltage. In this design, the OCD networks were placed inside the center of the microprocessor chip, limiting the area allowed for the I/O network and ESD device. The C4 solder balls were connected to the receiver and OCD banks via aluminum (Al) interconnects. In the bulk implementation, the OCD circuitry ESD results were limited by the Al interconnects. For the receiver networks, the ESD robustness of the receivers was limited by failure of the *n*-channel transmission gate (TG) and clamp networks. ESD results in the receiver networks were 4.3 kV (HBM) (Figure 8.18). The ESD STI-bound diode networks were modified to polysilicon-gated-SOI lateral diode structures with identical area for the bulk and SOI ESD areas. The SOI ESD design area was divided so that the diode perimeter for the SOI diode to V_{DD} was the same as the one to the V_{SS} power rail. No additional area or masks were utilized for ESD protection. The OCD circuit consisted of a self-biased well *p*-channel pull-up network and a cascoded series *n*-channel pull-down network. Resistor ballasting was employed in series with the *n*-channel pull-down network, using four SOI 40-Ω BR elements. The receiver networks comprised an *n*-channel pass transistor, an *n*-channel grounded gate, *n*-channel clamp device, and a *p*-channel MOSFET keeper element [23,24].

In the ESD network, three SOI diodes were placed between the 3.3- and 2.5-V power supplies. The first diode element was electrically connected to the 3.3-V power supply. Note that the four SOI diode elements were placed local to the I/O cell. In this fashion, all the SOI diode elements between the 3.3- and the 2.5-V power rails are in parallel (Figure 8.18).

Experimental results of the bulk and SOI implementations are shown in Figure 8.19. No ESD failures were evident below 6.5 kV (HBM), whereas the bulk CMOS receiver failures occurred at 4.3 kV. In the SOI implementation, the *n*-channel pass transistor and the *n*-channel over-voltage clamp networks did not use body contacts. It is believed that the "floating body" introduced body coupling and a lower trigger voltage of the *n*-channel elements, preventing early failure to the receiver networks.

8.4 SOI ESD NETWORKS IN SOI CPU WITH ALUMINUM (Al) INTERCONNECTS

Another implementation of an advanced 330-MHz 1.8V RISC-based microprocessor was mapped from bulk CMOS to SOI technology. The technology supported a 0.15-μm L_{eff}

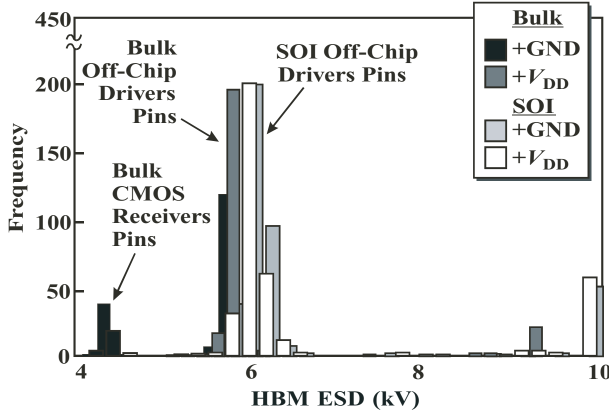

Figure 8.19 ESD HBM results of a 250-MHz RISC-based microprocessor in bulk CMOS and SOI technology

n-channel MOSFET and a 0.17-μm L_{eff} *p*-channel MOSFET device. The MOSFET drain used extension implants, halos, and cobalt salicide ($CoSi_2$) junctions. The source/drain extensions provided good V_T rolloff characteristics, and the $CoSi_2$ allowed the ability to maintain low-salicided polysilicon gate structure sheet resistance. The peripheral circuitry was placed on the outside edge of the microprocessor. The receiver network comprised a zero-V_T TG pass transistor and the receiver gate structure. The resistor was placed in series with the OCD for functional impedance-matching considerations [23,24].

In the bulk implementation, the ESD network comprised a single diode to V_{DD} and a single *n*-well diode element to V_{SS}. The ESD testing was completed in positive and negative polarities relative to V_{DD}, I/O V_{DD}, and V_{SS}. ESD results in bulk silicon showed no fails below 10-kV HBM levels (I/O V_{DD} is the external I/O power rail). In the SOI implementation, a 700-μm perimeter SOI polysilicon-gated diode network was connected to V_{DD} and to V_{SS}. The ESD area was allocated equally for the ESD diode to V_{DD} and V_{SS}. Worst-case ESD failures first occurred at 9.4 kV relative to the V_{SS} power rail for positive polarity. HBM testing relative to the V_{DD} power rail showed no failures below 10-kV HBM levels for the positive polarity. For negative pulse testing, no ESD failures occurred below −10 kV relative to the V_{SS} ground rail. Worst-case negative pulse failures occurred at −7.0 kV relative to V_{DD} power rail and −7.2 kV relative to I/O V_{DD} (Figure 8.20).

SOI failure analysis was completed on the worst-case failure mechanisms. Failure analysis results show that the aluminum interconnects in the power bus was the ESD-limiting failure mechanism in this design (Figure 8.21). Mapping a 330-MHz CPU design from bulk CMOS to SOI, the ESD results 7.2-kV HBM were achieved; the results were achieved in the SOI technology without additional masks, extra implants, or additional area [23].

ESD results were the test case of positive polarity to V_{DD} and negative polarity to V_{SS}, where a specific ESD solution was provided in the design. All other test modes saw some form of degradation in comparison to the bulk CMOS implementation. For positive polarity relative to V_{SS}, the lower SOI chip capacitance and potential current paths back to the V_{SS} ground plane were postulated for the 9.4-kV result. For the negative mode failures relative to V_{DD} and I/O V_{DD}, the power-bus rail failure was the limiting failure mechanism. There are three possible reasons: first, the implementation in SOI does not have a unique ESD element

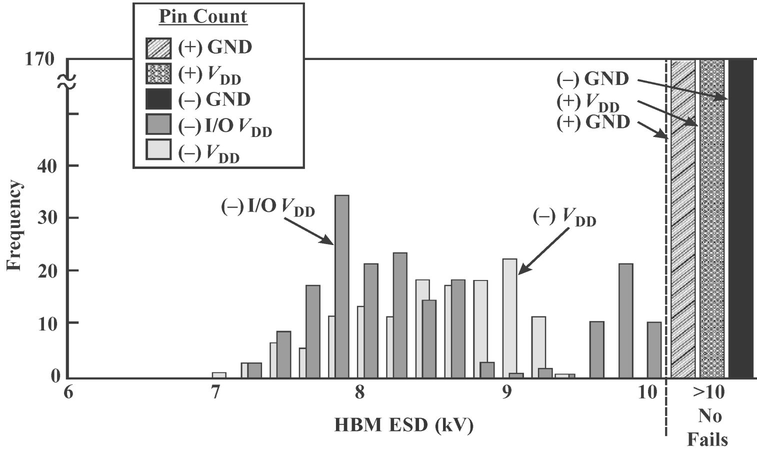

Figure 8.20 ESD HBM results of a 330-MHz 1.8-V RISC-based SOI microprocessor in a 0.15-μm L_{eff} technology

that provides a direct current path between pad and V_{DD} in a forward active element as is provided in the bulk implementation; second, in SOI, there are fewer current paths back to a given reference pin (V_{DD} or I/O V_{DD}); and third, the ESD robustness of the interconnects in SOI will be lower because of the increased dynamic thermal resistance from the BOX film. From this design remap, the learning demonstrated that additional design and architecture adjustments can be made to achieve the same results in the SOI implementation as was achieved in the bulk implementations. A key point in this work is that the silicon-based failure mechanisms were not the worst-case ESD limitation; the limitation of achieving only 7.2-kV HBM levels was related to the interconnects. By widening the aluminum interconnects or using fat wire upper-level metallization levels, ESD results in this technology could have achieved over 9.0-kV HBM in SOI technology.

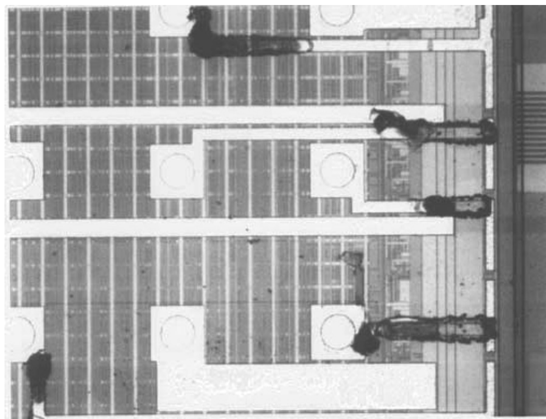

Figure 8.21 Failure analysis of SOI microprocessor with aluminum interconnects

8.5 SOI ESD DESIGN IN COPPER (Cu) INTERCONNECTS

Copper interconnects were introduced into CMOS technology for increased performance, but with the introduction of copper interconnects, the ESD robustness of microprocessors was interconnect-limited [21–24].

In the 0.12-μm L_{eff} technology generation, Cu interconnects with SiO_2 inter-level dielectrics are introduced to provide reduced interconnect RC delay. In this technology generation, the ESD robustness of the Cu interconnects are superior to the Al interconnect used in the prior technology generation. It has been shown that Cu interconnects achieve a 2× improvement in the critical current density to failure, J_{crit}. In this technology, there are six levels of Cu interconnects, a 0.12-μm L_{eff} *n*-channel MOSFET, and a 0.15-μm L_{eff} *p*-channel MOSFET (wher e both transistors have extension implants, $CoSi_2$, and a 3.5-nm dielectric thickness).

A 480-MHz 1.8V-power-supply microprocessor was designed in this 0.12-μm L_{eff} technology. Mixed-voltage interface circuits were used with the I/O circuits at 3.3-V power supply voltage and an internal core at 2.5-V power supply voltage. The bulk CMOS ESD architecture consisted of a diode string where the first element had a significantly larger perimeter. This first diode was connected to the exterior 3.3-V power rail. A string of diodes was then used locally to the cell with significantly less diode perimeter. The string of elements was shared across I/O books to achieve cross-pin parallelism and allow for reduction of the diode perimeter in the diode string of a given pad. The OCD circuitry consisted of BR-ballasted driver circuitry for both impedance control and for ESD protection. ESD protection results demonstrated worst-case HBM results of +7.8-kV HBM and −7.6-kV HBM. ESD testing was completed relative to V_{DD}, V_{SS}, AV_{DD}, $L2AV_{DD}$, and OV_{DD} power rails. The remapped design achieved 580 MHz in SOI [5]. In the SOI implementation, the STI-bounded diode structures were converted to SOI lateral polysilicon-bound gated diode elements. The perimeter of the diode-to-ground was increased in area and equal to the diode between pad and OV_{DD}. One hundred strings of SOI diodes were in a parallel configuration between the two power rails. For the SOI implementation, additional V_{DD}-to-V_{SS} ESD diode strings were added in the "white space" area of the design. ESD results are shown in Figure 8.22.

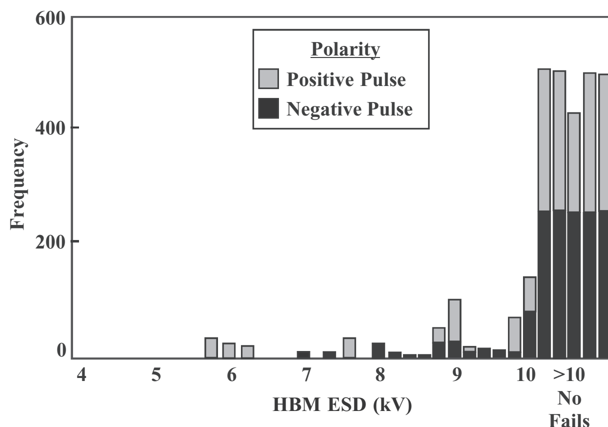

Figure 8.22 ESD HBM results of a 480-MHz 1.8-V RISC-based SOI microprocessor in a 0.12-μm L_{eff} technology

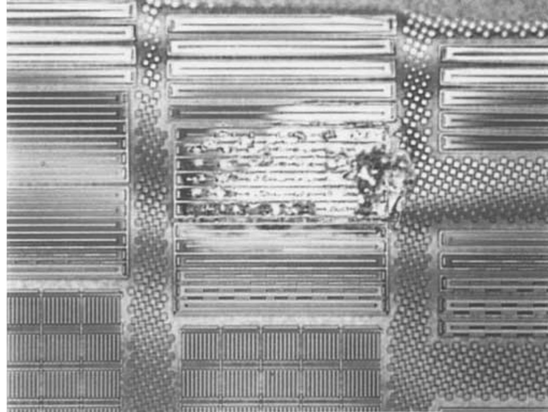

Figure 8.23 Failure analysis of the SOI ESD network in a 480-MHz 1.8-V microprocessor

In the SOI implementation, the worst-case ESD test mode for positive HBM tests was 8.0 kV (HBM). All pins exceeded 10-kV HBM levels relative to V_{SS}, V_{DD}, L2AV_{DD}, and OV_{DD} and exceeded 9.4 kV relative to L2AV_{DD} and OV_{DD}. Pin-to-pin tests all exceeded 10-kV HBM ESD test conditions. For negative mode tests, all pins passed to −10-kV ESD test levels with respect to V_{SS}. ESD test results of −7.4 kV were achieved with respect to the core V_{DD}. Additional failures occurred on specific pins associated with secondary and tertiary power rails (L2AV_{DD}, OV_{DD}, and L2 OV_{DD}). The worst-case failure was −5.8 kV in this first-pass SOI implementation. The failure mechanism at the ESD magnitude of −7.4 kV was failure of the polysilicon gated diode structure (Figure 8.23).

At this same failure point, the BR resistor structures also showed silicon damage. This implementation demonstrated the ability to achieve over 4-kV ESD protection in a mixed-voltage interface network at frequencies up to 600 MHz in PD SOI technology. It was also evident from these results that, with improved negative-mode ESD solutions, achieving ESD protection levels above 8 kV is possible.

8.6 SOI ESD DESIGN WITH GATE CIRCUITRY

SOI ESD design using SOI structures on the SOI thin film surface contains gate dielectric structures. As a result, these SOI ESD structures are sensitive to gate over-voltage conditions. SOI ESD structures vulnerable to MOSFET dielectric over-voltage include the following:

- SOI MOSFETs.
- SOI BR elements.
- SOI lateral gated-diode elements.

In mixed-voltage applications, and overshoot and undershoot conditions, the MOSFET gate dielectric can become over-stressed.

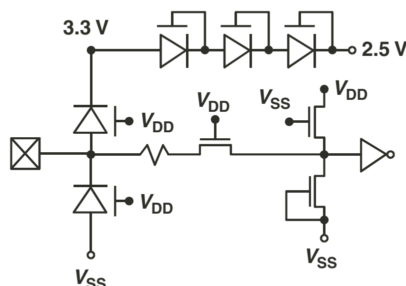

Figure 8.24 SOI ESD circuitry and receiver network

In the case of the MOSFET, using an RC-triggered SOI MOSFET or a grounded-gate SOI MOSFET ESD application, as the pad node reaches the MOSFET dielectric breakdown condition, dielectric failure or degradation can occur.

In a mixed-voltage interface condition, where a SOI polysilicon gated diode structure is used, the SOI gate dielectric can become overstressed in some functional and ESD modes of operation. For example, a mixed-voltage application required 3.3-V tolerant I/O networks with a 2.5-V core voltage (Figure 8.24). In this implementation, if the SOI diode structure gate of the "up-diode" was electrically connected to the 3.3-V power supply, and the SOI diode structure gate of the "down-diode" was connected to the input pad node, voltage states exist where electrical over-voltage can occur. In the case of the pad voltage increasing to 3.3 V, the gate-to-anode voltage (e.g., $V_{pad} - V_{SS}$) of the "down-diode" would be 3.3 V. In the case that the pad voltage was 0 V, the gate-to-anode voltage (e.g., $V_{CC} - V_{pad}$) of the "up-diode" would be 3.3 V; in both these cases, the SOI diode dielectric voltage would be overstressed. Additionally, SOI failure mechanisms can occur in the SOI gated diode during CDM events, when the gate structure is connected to the input pad. To avoid electrical overstress, the following solutions can be established:

- Decouple the SOI lateral gated-diode gate structure from the anode or cathode.
- Decouple the SOI lateral gate-diode structure from the power supply rails.

The first ESD design practice prevents the over-voltage of the SOI device dielectric by electrically connecting the SOI polysilicon gate to the anode or cathode and forcing an electrical connection to the pad voltage, or to one of the power rails. As shown, the maximum differential voltage state on the gate is $V_{CC} - V_{DD}$ or $V_{DD} - V_{SS}$.

From the second ESD design practice, the gate can be set at a power supply voltage, but not electrically coupled to the power supply rails. This can be achieved using a "dummy inverter" circuit whose input is set at a low state. In this fashion, the dummy inverter output sets the voltage at the power supply voltage, but is not electrically connected, to avoid adverse ESD conditions. Experimental results using this implementation achieved 5000-V HBM, 800-V MM, and 1000-V CDM levels (Figure 8.25).

Additional process and device solutions exist to address the issue of the lateral gated diode dielectric gate failure and operation. Methods to address the SOI lateral gated diode dielectric failure are as follows:

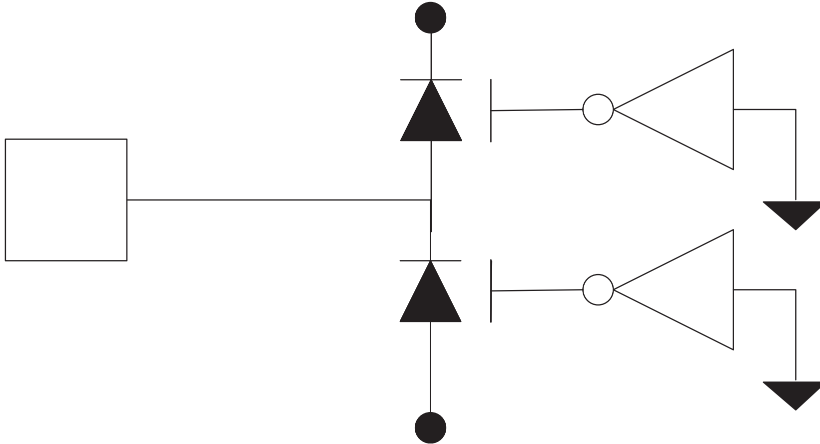

Figure 8.25 SOI diode with dummy inverter gate circuitry

- Removal of halo implant [26].
- Polysilicon gate depletion (e.g., lower polysilicon gate doping concentration) [27].
- Removal of SOI lateral gated diode gate dielectric structure [20,29,31].

N. Zamdner noted that the existence of the ‘‘bad halo’’ leads to higher series resistance [26]. Removal of the bad halo leads to reduction of the series resistance. S. Voldman and J. Brown proposed allowing polysilicon gate depletion to reduce the gate dielectric overstress [27]; this solution lowers the gate dielectric over-voltage. M. D. Ker and T. H. Tang removed the SOI lateral gate dielectric structure, completely removing the issue of gate dielectric overstress [29–31]; this solution requires an additional mask step and etch for the gate removal.

8.7 SOI AND DYNAMIC THRESHOLD ESD NETWORKS

SOI technology does not have the MOSFET body electrically connected to the substrate. This allows for the opportunity of construction of SOI body-coupled ESD structures. Dynamic threshold MOSFETs lend themselves to achieving a near ideal sub-threshold characteristics, a high on-current to off-current ratio (I_{ON}/I_{OFF}), and higher MOSFET current drive [32].

SOI dynamic threshold ESD networks allows for the following:

- Low-trigger voltage: DTMOS allows for a low-trigger condition allowing for early turn-on during ESD events [33–39].
- Body coupling: Body coupling allows for uniform control of substrate potential during ESD events [33–39].
- Gate coupling: Gate coupling in ESD structures provides uniform control of gate electrode potential and turn-on of all MOSFET fingers [33–39].

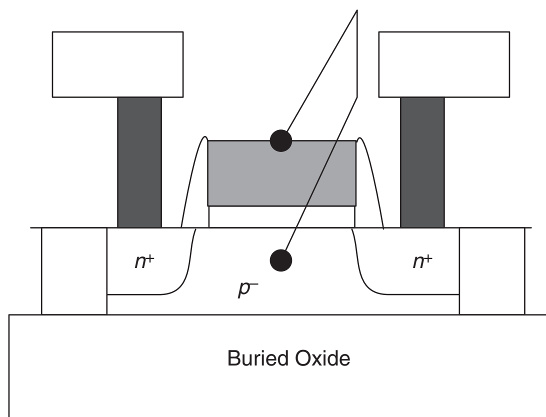

Figure 8.26 DTMOS body- and gate-coupled SOI ESD device

- Symmetry of circuits: *n*- and *p*-channel dynamic threshold MOSFETs can be used for positive and negative ESD discharges [33–39].

SOI DTMOS ESD structures allow for ideal features to provide good ESD protection in SOI networks. Figure 8.26 shows an example of a DTMOS body- and gate-coupled SOI ESD device. In the circuit, the body and gate electrode are electrically connected to the input pad node. In this case, the network forms an inherent double-diode network between the SOI MOSFET body and the MOSFET source/drain junction regions. Note that in the SOI *n*-channel MOSFET, the *p*-body serves as the anode, and the *n*-diffusion serves as the cathode; in the SOI *p*-channel MOSFET, the *n*-body serves as the cathode and the *p*-diffusion serves as the anode. Additionally, note that the *n*-channel SOI MOSFET is electrically connected to the V_{DD} power supply, and the *p*-channel SOI MOSFET is electrically connected to the V_{SS} power supply [35,36]. Note that this configuration is identical to the topology of an active clamp network [36–38].

8.8 SOI TECHNOLOGY AND MISCELLANEOUS ESD ISSUES

SOI technology must address additional issues associated with ESD, which manifest themselves differently in bulk CMOS. The issues include the following:

- Substrate contacts.
- Fuse networks.

In SOI, when charging occurs on the substrate, the insulating BOX prevents the electrical charge to pass to the SOI semiconductor devices. Given no electrical connection to the power grid or to the devices, the BOX will undergo dielectric failure, or an surface discharge will occur at the edge of the semiconductor chip [43,44]. As a result, an electrical current must find a path to discharge to the surface, the devices, the power grid, or the chip package. S. Geissler demonstrated that improper electrical contacts can lead to changes in the logic states on functional testers, after touching an SOI wafer. S. Geissler and S. Voldman

proposed different structures and methods of preventing the back-side charging [43,44]. This can be achieved by an edge spark gap structure, electrical interconnects through the BOX structure, or ESD protection devices [43,44]. A key advantage of the SOI technology is that the charge accumulated in the substrate does not reach the SOI receiver networks since the MOSFET body are floating; as a result, while on one hand, the need to ground the back side is fundamental, on the other hand, it is desirable to not allow the rapid discharge from the back of the wafer to reenter the circuitry.

In the implementation of fuses, fuse control networks are required to determine if a fuse is ‘‘open.’’ Fuse networks that are electrically connected to external pins must provide ESD protection. In the implementation of SOI ESD networks to protect the fuse network, it is also fundamental that the ESD failure of the SOI ESD devices leads to misreading of the fuse state [42]. As a result, care must be taken in the implementation of the choice of ESD network to avoid HBM, MM, or CDM events leading to SOI ESD network failure and misinterpretation of the fuse states.

8.9 SUMMARY AND CLOSING COMMENTS

In this chapter, Chapter 8, SOI ESD circuits utilized in mainstream SOI applications were discussed. The focus of the chapter was on integration of the SOI ESD networks in SOI microprocessors. Both native power supply and mixed-voltage interface applications were reviewed. The evolution of the ESD networks with the power supply scaling is evident; as the power supply was reduced, technology innovation and scaling improved the ESD robustness of the SOI ESD structures. In time, ESD learning leads to more scaled and aggressive designs and architectural tricks, and ESD fault recognition leads to improved SOI product results. Applying ESD design practices, such as gate decoupling for the SOI gated diode structures and the addition of decoupling from the power supply, additional improvements continued.

In Chapter 9, the design and layout of ESD power clamps is discussed for CMOS and BiCMOS technologies. ESD power clamps are fundamental to an ESD protection strategy and design implementation. In this chapter, we will discuss both CMOS and BiCMOS ESD power clamp netwoks for CMOS, BiCMOS silicon germanium, and gallium arsenide networks.

PROBLEMS

8.1. SOI ESD networks consist of SOI gated-diode elements with a p^+ anode and a cathode comprising an n-well and an n^+ implant. The SOI MOSFET gate structure is electrically connected to the cathode. Forming an SOI double-diode network, this element is placed between the input signal pad and the V_{DD} and V_{SS} power rails. Show all cases of the voltage stress between the input signal pad and the power rails, and the conditions across the ESD element.

8.2. SOI ESD networks consist of SOI gated-diode elements with a p^+ anode and a cathode comprising an n-well and an n^+ implant. The SOI MOSFET gate structure is electrically connected to the cathode. Forming an SOI double-diode network, this element is placed

between the input signal pad and the V_{DD} and V_{SS} power rails. Assume the input signal exceeds the power supply voltage, (e.g., V_{CC}) show all possible voltage state conditions where failure will occur.

8.3. To avoid electrical overstress of the gate structures, the SOI ESD element gates were separated from the power supply connections and electrically connected to the output of an SOI inverter circuit. The input of the dummy inverter circuit was electrically connected to V_{SS}. Evaluate the voltage conditions for an input level of V_{CC} and V_{SS} (e.g., high "1" and low "0" conditions). Assume long-channel MOSFETs in the inverter circuit. Calculate the resistance magnitude in series with the SOI ESD gate structures assuming the SOI MOSFET "on" resistance.

8.4. SOI diode string networks can exist where the anode and cathode elements are placed in a series configuration. In this case, the gates are connected to the cathode. Show the voltage condition for N SOI diodes, when N SOI diodes are placed in a series configuration between V_{DD} and V_{SS}. What is the maximum voltage stress across the gate structures?

8.5. Fuse networks are designed to read the state of the fuse to determine whether a fuse is "blown" open or intact. Fuse circuit networks must correctly read the state of the fuse, without the network itself leading to a false reading. Additionally, ESD events can cause failure of fuse elements. As a result, ESD networks are needed to prevent ESD failures of the fuse. But, the ESD networks cannot introduce "false fuse readings." Show that using an SOI ESD double-diode network (with gate coupled to cathodes) can lead to false fuse reading when used following the fuse element but prior to the "read" circuitry.

8.6. SOI ESD fuse networks must protect the fuse elements, and not introduce false readings. What possible SOI ESD networks will avoid false reading of the fuse networks?

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9 ESD Power Clamps

9.1 ESD POWER CLAMP DESIGN PRACTICES

An electrostatic discharge (ESD) design practice is the integration of ESD power clamps between the power supply rails. ESD power clamps popularity occurred in the 1990s to achieve better ESD results in semiconductor chips [1–6]. By mid 1990s, diode string [3–17], MOSFET-based [1,3,20–27], and bipolar ESD power clamps [43–49], and silicon-controlled rectifiers [50–60] became part of the ESD design methodology and practice. From 1995 to 2005, the focus on the MOSFET ESD power clamps have been on producing a better ESD power clamp, design integration, physical placement [33–36], and low leakage [38]. In the other technologies, the focus has been extending the concepts to triple-well CMOS [11,12], BiCMOS, silicon germanium [10,13–15,45–47], gallium arsenide [48,49], and silicon-on-insulator (SOI) technologies [17–19]. ESD power clamps achieve both functional and ESD advantages. ESD power clamps achieve ESD robustness and electrical overstress (EOS) robustness by enhancing the ESD design practice as follows:

- Establishment of ESD Current Loops: The addition of power clamps provides an alternative current loop for the ESD current.
- Bidirectional Current Paths: Bidirectional current flow allows the flow of the ESD current through the loop in both directions.
- Segmented Chip Current Path: ESD power clamps can be placed between independent and disconnected chip segments allowing electrical connectivity.
- Rail-to-Rail ESD Protection: Rail-to-rail ESD protection between the two power rails is achieved using the power clamp placed between the two power rails.
- Pin-to-Pin ESD Protection: Pin-to-Pin ESD protection is achieved by establishing bidirectional current paths from the first pin, through the power clamp and to the second pin.

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- Impedance Reduction: With the introduction of the ESD power clamp, the impedance through the current loop can be reduced.
- Chip-Impedance Independence: With an ESD power clamp, the current loop is a not a function of the natural impedance (capacitance) of the semiconductor chip.
- Segmentation Independence: With an ESD power clamp, the influence of segmentation is reduced.
- Power Bus Resistance Independence: With the introduction of the ESD power clamps, the periodicity and placement can reduce the impact of the bus resistance in the ESD current loop.
- Voltage Clamping: Using voltage-triggered ESD power clamps, the voltage limitation can be placed on the power supply rail; this limits overvoltage states, electrical overstress, undershoot, and overshoot phenomena. Additionally, the ESD power clamp defines a voltage level where the ESD power clamp begins conduction of the current and prevents electrical overstress of the semiconductor chip circuitry.
- Latchup Prevention: Placement of power clamps can reduce the initiation of parasitic *pnpn* elements within a semiconductor chip.

The ESD power clamp establishes additional current loops within the semiconductor chip to establish alternative current loops for the ESD current flow. This allows the current to flow from the ESD element through the chip power rails and ground planes.

The establishment of bidirectional current flow allows for both rail-to-rail ESD protection and pin-to-pin. Using ESD power clamps that have bidirectional features allows for improved bidirectional rail-to-rail protection. Additionally, the bidirectionality allows for pin-to-pin protection since a forward bias current path can be established when the pins are reversed or the polarity of the pulse is reversed.

In mixed signal (MS), mixed-voltage interface (MVI), and system-on-chip (SOC), chip segments are naturally isolated through the power bus architecture, but remain in a common substrate. This leads to the requirement of testing relative to any pin to all power rails. In a segmented chip design, natural forward bias current paths may not exist. ESD power clamps can reestablish the electrical connectivity; without the electrical connectivity and forward bias path, input pin ESD results relative to different power rails will be significantly variable.

With the introduction of the ESD power clamp, the impedance through the current loop can be reduced. This provides both improved rail-to-rail ESD protection results, as well as improved pin-to-rail ESD results. With an ESD power clamp, the current loop is a not a function of the natural impedance (capacitance) of the semiconductor chip. When no ESD power clamp exists, the ESD protection levels are a function of the chip capacitance and how the current distributes in space and time through the semiconductor chip. The total chip capacitance is a function of the chip size, and the effective chip capacitance is a function of how the current distributes. With the ESD power clamps, current "sinks" or conductance paths can be integrated into the chip architecture allowing independence from the chip natural capacitance.

As a semiconductor chip is segmented into the different chip sectors, cores, or voltage islands, the use of power clamps reduces the impact of the segmentation. With the segmentation, the separate region has a lower capacitance within the power grid of the

segment. With the addition of ESD power clamps, the electrical connectivity allows for a lower impedance within the sector, or a new current path to the core, where larger capacitance elements exist (e.g., core capacitance).

With the introduction of the ESD power clamps, the periodicity and placement can reduce the impact of the bus resistance in the ESD current loop. The placement and periodicity of the ESD power clamps allow for less dependence on the bus architecture (e.g., metal resistance and metal bus width). As a result, improvements occur in the variation of identical pins (e.g., ESD pin failure distribution).

Using voltage-triggered ESD power clamps, the voltage limitation can be placed on the power supply rail. This limits over-voltage states, electrical overstress, undershoot, and overshoot phenomena. Additionally, the ESD power clamp defines a voltage level where the ESD power clamp begins conduction of the current and prevents electrical overstress of the semiconductor chip circuitry.

With the creation of a voltage clamp on the power rail, CMOS latchup robustness can be improved (e.g., for some latchup conditions). CMOS latchup can be initiated by over-voltage conditions between the V_{DD} and V_{SS} power supply. ESD power clamps establish a maximum voltage across the two power rails; this indirectly prevents dc or transient CMOS latchup. Indirectly, this can also lower the voltage drop for input pin over-voltage conditions as well, by lowering the input voltage state during an input pin over-voltage condition. Hence, the voltage limiting advantage can reduce the total voltage state of the power rails and establish an alternative current path which is not prone to CMOS latchup.

A significant number of new ESD power clamp circuits and inventions occur in the literature. In this chapter, some basic classes of ESD power clamps will be discussed associated with CMOS, triple-well CMOS, BiCMOS, BiCMOS SiGe, and SOI technologies. Power clamps for native power supplies and mixed voltage conditions will be discussed. The classes of the ESD power clamps are as follows:

- Diode string ESD power clamps.
- Frequency-triggered MOSFET ESD power clamps.
- Voltage-triggered MOSFET ESD power clamps.
- Bipolar voltage-triggered ESD power clamps.
- Silicon controlled rectifier (SCR) ESD power clamps.

9.2 ESD POWER CLAMPS: DIODE-BASED

9.2.1 ESD Power Clamps: Series Diode Strings as Core Clamps

ESD power clamps between the power supply and ground potential consist of a series of diode elements. Series diode elements are most common on signal pins for mixed-voltage interface (MVI) applications. Series diode elements are also used between two power rails, or two ground rails. In the case of two power rails, it is common to use diode elements between separate V_{DD} power domains, such as analog V_{DD} and digital V_{DD}. Series diode

elements can also be used between a power rail, such as digital V_{DD}, and the ground rail, digital V_{SS}.

In the use of series diodes as core clamps between V_{DD} and V_{SS}, turn-on voltage, resistance, and leakage are important issues in the semiconductor chip design. The turn-on voltage is a function of the number of diodes in series, the forward voltage of each diode, the area parameter, and vertical bipolar current gain. Assuming equal areas of each diode, this can be expressed as

$$V_T = mV_f - V_o \frac{m(m-1)}{2} \ln(\beta + 1)$$

Explicitly expressing the temperature dependence,

$$V_T(T) = mV_f - \left(\frac{kT}{q}\right) \frac{m(m-1)}{2} \ln(\beta(T) + 1)$$

where T is the temperature.

Using series diode elements as a ESD core clamp between the V_{DD} and the V_{SS}, the turn-on voltage of the series diode string must exceed the power supply voltage differential (Figure 9.1)

$$V_T(T) = mV_f - \left(\frac{kT}{q}\right) \frac{m(m-1)}{2} \ln(\beta(T) + 1) \geq V_{DD} - V_{SS}$$

With power supply voltage variations, the core clamp turn-on voltage must exceed the statistical variations of the power supply voltage. Hence, to address the statistical variation

Figure 9.1 Diode string core clamp

of the power supply, the condition for the core clamp can be expressed as

$$V_{\mathrm{T}}(T) = mV_{\mathrm{f}} - \left(\frac{kT}{q}\right)\frac{m(m-1)}{2}\ln(\beta(T)+1) \geq (V_{\mathrm{DD}} + \Delta V_{\mathrm{DD}}) - V_{\mathrm{SS}}$$

The presence of the parasitic *pnp* bipolar current gain term reduces the effectiveness of every successive diode in the diode string. Because of the parasitic *pnp* current gain term, additional diodes will be required to achieve to satisfy the inequality. As a result, the non-linearity term leads to semiconductor chip area and additional elements in the design. For example, given a diode string of $m + 1$ diodes, the representation can be shown as

$$V_{\mathrm{T}(m+1)} = (m+1)V_{\mathrm{f}} - V_{\mathrm{o}}\frac{(m+1)(m+1-1)}{2}\ln(\beta+1)$$

The change in the turn-on voltage can then be represented as

$$V_{\mathrm{T}(m+1)} - V_{\mathrm{T}(m)} = [(m+1) - m]V_{\mathrm{f}} - V_{\mathrm{o}}\left[\frac{(m+1)(m)}{2} - \frac{m(m-1)}{2}\right]\ln(\beta+1)$$

which can be expressed as

$$V_{\mathrm{T}(m+1)} - V_{\mathrm{T}(m)} = V_{\mathrm{f}} - mV_{\mathrm{o}}\ln(\beta+1)$$

As the number of diodes increase, the net forward voltage with the addition of more elements is less effective with each additional element since the second term decreases the net gain in the turn-on voltage.

In the diode clamp formulation, the solution for the number of diodes is a quadratic equation. We can solve for the number of diodes by first equating the sides of the inequality and then putting the expression in quadratic form

$$-\left[\left(\frac{2}{V_{\mathrm{o}}\ln(\beta+1)}\right)\left\{mV_{\mathrm{f}} - (V_{\mathrm{o}})\frac{m(m-1)}{2}\ln(\beta+1)\right\}\right] = -\left(\frac{2}{V_{\mathrm{o}}\ln(\beta+1)}\right)[(V_{\mathrm{DD}} + \Delta V_{\mathrm{DD}}) - V_{\mathrm{SS}}]$$

Rearranging the terms

$$m^2 - \left(1 + \frac{2}{\ln(\beta+1)}\left[\frac{V_{\mathrm{f}}}{V_{\mathrm{o}}}\right]\right)m + \left(\frac{2}{\ln(\beta+1)}\left[\frac{V_{\mathrm{DD}} + \Delta V_{\mathrm{DD}} - V_{\mathrm{SS}}}{V_{\mathrm{o}}}\right]\right) = 0$$

From this form, the solution of the number of diodes can be solved, applying the quadratic formula

$$m = \frac{1}{2}\left(1 + \frac{2}{\ln(\beta+1)}\left[\frac{V_{\mathrm{f}}}{V_{\mathrm{o}}}\right]\right) \pm \frac{1}{2}\sqrt{\left(1 + \frac{2}{\ln(\beta+1)}\left[\frac{V_{\mathrm{f}}}{V_{\mathrm{o}}}\right]\right)^2 - 4\left(\frac{2}{\ln(\beta+1)}\left[\frac{V_{\mathrm{DD}} + \Delta V_{\mathrm{DD}} - V_{\mathrm{SS}}}{V_{\mathrm{o}}}\right]\right)}$$

From this expression the number of diodes can be calculated. Note in this expression, the number of diodes are related to the ratio of the voltages. In the limit that the *pnp* bipolar current gain is much smaller than unity, the expression should reduce to the power supply voltage term over the forward voltage of the diodes.

For high-voltage power supplies, the use of diode strings is not efficient when the parasitic bipolar term is significant in magnitude. As the power supply is scaled to lower voltages, the use of series diode elements becomes more practical. Assume a power supply voltage V'_{DD} according to MOSFET constant electric field scaling

$$V'_T(T) = mV_{\mathrm{f}} - \left(\frac{kT}{q}\right)\frac{m(m-1)}{2}\ln(\beta(T)+1) \geq V'_{\mathrm{DD}} + \Delta V'_{\mathrm{DD}}$$

$$V'_{\mathrm{DD}} = \frac{V_{\mathrm{DD}}}{\alpha}$$

and

$$\Delta V'_{\mathrm{DD}} = \frac{\Delta V_{\mathrm{DD}}}{\alpha}$$

As the power supply voltage is scaled, the number of elements to satisfy the inequality will be reduced.

9.2.2 ESD Power Clamps: Series Diode Strings as Core Clamps—Cladded Design Concept

In the earlier section, it was noted that three primary considerations are necessary in the design of ESD diode string power clamps. The ESD design considerations include the voltage turn-on condition, the resistance, and the leakage amplification issue. The leakage amplification was discussed by S. Dabral and T. J. Maloney [4–6], and G. Gerosa and S. Voldman [7,8]. In the implementation by Gerosa and Voldman, a simple diode was implemented across a number of successive stage to limit the forward bias diode turn-on [7,8].

Maloney addressed the question of non-uniform current flow in the diode string to maximize the ESD design efficiency. It was noted that the parasitic *pnp* bipolar current gain is a function of the collector current magnitude due to bipolar effects such as the Webster effect [5]. Maloney noted the paradox that the high bipolar current gain reduces the turn-on voltage of the power clamp; at the same time, the high bipolar current gain leads to the ability to discharge a higher ESD current. The condition for achieving the optimum ESD protection device has the following ESD design practice:

- Discharge the highest current and distribute current through the ESD diode string.
- Maximization of turn-on voltage.

Maloney noted that the total current can be represented as [5]

$$I_{\mathrm{tot}} = I_1\left(1 - \frac{1}{\beta+1}\right) + I_2\left(1 - \frac{1}{\beta+1}\right) + \cdots + I_{n-1}\left(1 - \frac{1}{\beta+1}\right) + I_n$$

To maximize the total voltage condition under the constraint of a constant total current, a constraint function was established where

$$g(V_1, V_2, \ldots, V_n) = \left\{ \frac{\beta + 1}{\beta} I_n + \sum_{j=1}^{j=n-1} I_j \right\} - C_o = 0$$

where

$$I_k = A_k \exp\left\{ \frac{V_k}{V_o} \right\}$$

Using the method of Lagrangian multipliers, Maloney showed given a function *H*, where *H* is a function of the forward voltages and the constraint variable [5]

$$H(V_1, V_2, \ldots, V_n, \lambda) = V_T - \lambda_g(V_1, V_2, \ldots, V_n)$$
$$\frac{\partial H}{\partial V_j} = 1 - \frac{\lambda A_j}{V_o} \exp\left(\frac{V_j}{V_o} \right) = 0$$

for all successive stages, and for the last stage

$$\frac{\partial H}{\partial V_n} = 1 - \frac{\lambda A_n}{V_o} \frac{\beta + 1}{\beta} \exp\left(\frac{V_n}{V_o} \right) = 0$$

Maloney showed that for the case of bipolar current gain significantly greater than unity, the optimum condition is equal to currents in all diode stages. For the case of *any pnp* bipolar current gain, the optimum condition is

$$I_1 = I_2 = I_{n-1} = \frac{I_{tot}(\beta + 1)}{n\beta}$$

and

$$I_n = \frac{I_{tot}}{n}$$

where the diode currents are the currents in the successive stages of the network. Mathematically, it was shown that the optimum ESD design practice is when the currents are equalized through the successive stages.

To achieve equalization of the successive currents, the bias network of variable resistor values compensates for the bipolar current gain factor. Using resistor elements as a parallel bias network, the optimum condition for "*n*" stages would be resistor values of the following sequence [5]

$$\frac{R}{n-1} \; \frac{R}{n-2} \; \frac{R}{n-3} \; \cdots \; \frac{R}{3} \, \frac{R}{2} \, R$$

Figure 9.2 shows an example of the "cladded bias network" that addresses the uniformity of current using resistor elements. In practice, the "resistors" are *p*-channel MOSFET elements.

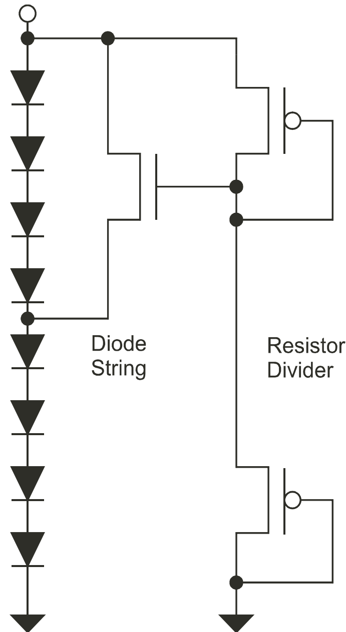

Figure 9.2 ESD diode string with cladded bias network

9.2.3 ESD Power Clamps: Series Diode Strings as Core Clamps—Boosted Design Concept

In a second method, Maloney proposed the concept of ‘‘boosting’’ the successive diode stages (Figure 9.3) [5]. Conceptually, the successive diode stages are placed in parallel with a control network; the control network is a buffered voltage divider network (using resistor elements). The buffered voltage divider network is electrically connected in a position within the diode string. The voltage divider sets a state to supply extra current to the center stage of the voltage divider. In the implementation by Maloney, it was noted that *p*-channel MOSFETs can be used as the resistor element. The use of the *p*-channel element will also allow integration with the p^+/n-well diodes of the diode string.

9.2.4 ESD Power Clamps: Series Diode Strings as Core Clamps—Cantilever Design Concept

To avoid the leakage current of the ESD diode string during functional operation, the diode string can be decoupled from the lower power rail preventing leakage current and unnecessary standby power loss [5]. In a microprocessor, with the addition of the ESD elements and the high temperatures, it is an advantage to prevent the ESD structures from causing leakage current. Hence, a circuit that decouples from the power sources during functional chip operation is advantageous. Figure 9.4 shows a ‘‘Cantilever ESD power clamp’’ which electrically decouples the diode string during chip operation. By synthesizing

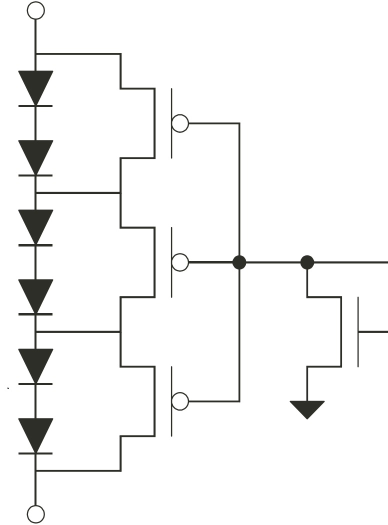

Figure 9.3 ESD diode string with a boosted center stage

the diode string with an RC-coupled *p*-channel MOSFET network, a circuit can achieve the following advantages:

- DC Disablement: Diode String disablement during chip functional operation.
- Off-State Leakage Reduction: Darlington current disablement during chip operation desensitizing temperature dependence.

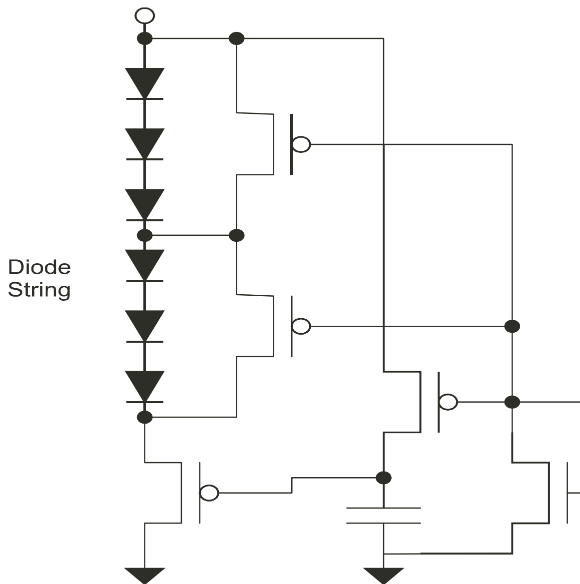

Figure 9.4 Cantilever ESD diode string

- Frequency-Triggered ESD Initiation: Initiation during an ESD event whose RC-trigger is responsive to an ESD pulse.

In the circuit, transistor elements are used to equalize the current in the successive stages during ESD operation. Additionally, the *p*-channel MOSFET is initiated during ESD events to allow current to flow between the power rails.

9.2.5 ESD Power Clamps: Triple-Well Series Diodes as Core Clamps

In triple-well technology, ESD power clamps can be constructed between the power supply and the ground potential, which can address the leakage concerns which occur in the single- and dual-well CMOS structures [10–15]. In single- and dual-well CMOS series diode ESD power clamps, the p^+/n-well elements, the parasitic bipolar element exists between the p^+ diffusion, the *n*-well, and the substrate region. The successive diode stages are in a *pnp* common-collector configuration. As was shown for mixed voltage interface (MVI) dual-well CMOS diode strings, the leakage is amplified by each successive stage [5–9].

Triple-well CMOS and BiCMOS technologies allows for a buried *n*-type layer to be placed in a fashion to isolate the *p*-epitaxial region or *p*-well region [10]. Utilizing the *n*-type buried layer, triple-well technology allows for the ability to reduce the parasitic leakage current in ESD power clamp networks [10–15]. In a triple-well technology, the shallow trench isolation (STI) defined p^+ diffusion can be placed in a *n*-well region, or a *p*-well region. The *n*-buried layer can be placed under the *n*-well or *p*-well region [10].

A triple-well ESD power clamp can be formed using a p^+ anode in a *n*-well, with an underlying buried layer implant. Isolated epitaxial regions can be formed using an implant layer or sub-collector implants from bipolar transistor elements. The "edge" structure, to isolate the epitaxial region, can be a diffused region (e.g., *n*-well) or a trench isolation structure. In BiCMOS and BiCMOS Silicon Germanium technology, the sub-collector implant can be placed under a *p*-well region to isolate the epitaxial region. In the case of an *n*-type buried layer under the *n*-well region, the vertical *pnp* bipolar current gain can be significantly reduced as a result of the increase in the parasitic *pnp* base width, and higher doping concentration. The vertical *pnp* bipolar current gain can be further reduced using a sub-collector implant and trench isolation, as demonstrated by Voldman and Gebreselasie [10]. Using an *n*-buried layer, a sub-collector and deep trench (DT) isolation, the *pnp* vertical bipolar gain is sufficiently reduced such that the leakage amplification is not a significant issue [10]. Figure 9.5 shows an example of a DT defined triple-well technology ESD diode string network.

In triple-well CMOS technology, or a BiCMOS technology, the diode structure can be placed in a *p*-well region which is isolated by a lower *n*-type structure and a sidewall edge structure [12–14]. Forming a triple-well diode structure, the STI-defined p^+ diffusion can be placed in a *p*-well region. The STI-defined cathode is contained within the *p*-well. The triple-well isolating region can be used in two fashions:

- Electrically connected to the successive ESD power clamp stages serving as a second *p–n* junction for improved discharge capability.

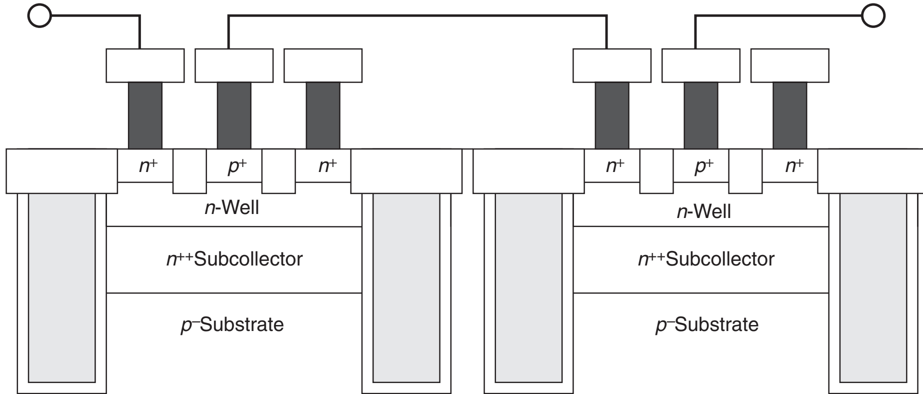

Figure 9.5 Deep trench defined ESD power clamp

- Electrically "floating" in the *p*-substrate region.
- Electrically biased to a separate bias potential.

In the first case, the *n*-band isolation region can be electrically connected and serve as a second cathode structure for the ESD power clamp, as proposed by Sloan, Pequignot, Stout, and Voldman [11] (Figure 9.6). In this fashion, the separate band region increases the total diode area forming two parallel metallurgical junctions and two parallel current paths which converge for each successive stage. An advantage of this implementation is the ability to utilize the deep buried layer region as well as the STI-defined n^+ cathode. But, in this process, the isolation is compromised for improved current discharge capability. Additionally, in this fashion, a parasitic *pnp* is formed between the *p*-well, the *n*-band region, and the *p*-substrate. Although there is a vertical parasitic *npn* transistor formed between the *n*-band, the *p*-well region, and the STI-defined *n*-cathode element because they are electrically connected, this eliminates any parasitic *npn* interaction. An additional ESD design layout disadvantage is that each successive stage cannot merge the triple-well region together (e.g., note that the spacing between the adjacent wells and buried layers can be a significant).

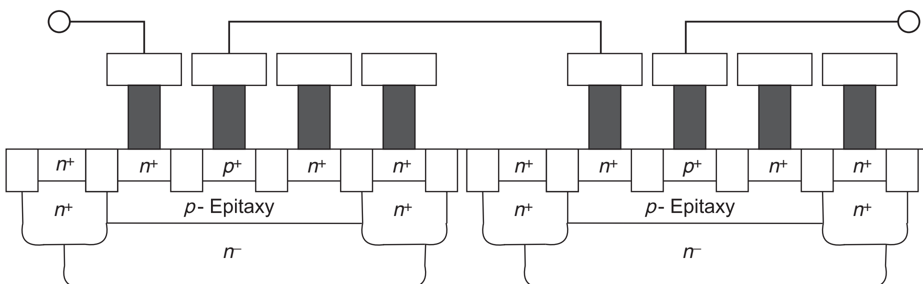

Figure 9.6 Triple-well ESD power clamp with p^+ diffusion in an isolated *p*-well and *n*-band second cathode

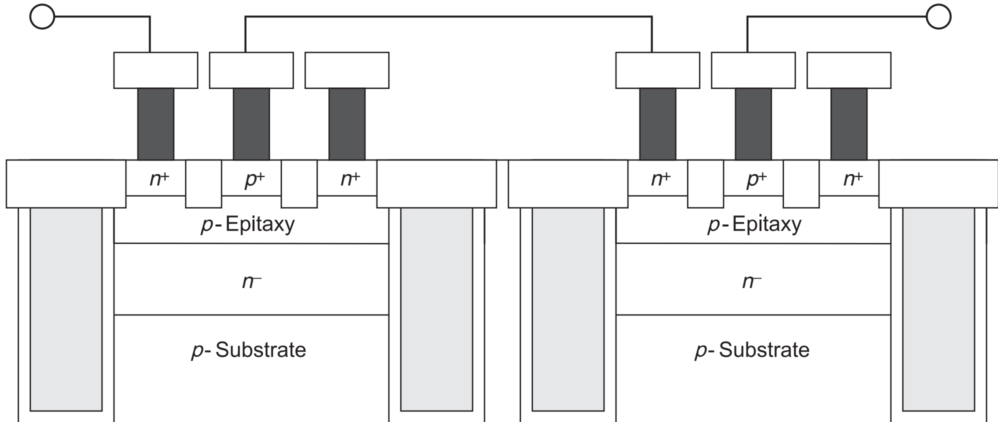

Figure 9.7 Triple-well ESD power clamp with p^+ diffusion in an isolated *p*-well, floating *n*-subcollector, and deep trench (DT) isolation

In the second case, the *n*-band region can remain floating in the substrate region, as proposed by Sloan, Pequignot, Stout, and Voldman [11] (Figure 9.7). A parasitic *pnp* is formed between the *p*-well, the *n*-band region, and the *p*-substrate. Additionally, there is a vertical parasitic *npn* transistor formed between the *n*-band, the *p*-well region, and the STI-defined *n*-cathode element. S. S. Chen *et al*. [12–14] used a sub-collector region and a DT sidewall to isolate the *p*-well region from the substrate. Using the sub-collector region and the DT sidewall isolation, the leakage current is reduced (e.g., compared to the single- and dual-well series diode CMOS ESD power clamps). S. S. Chen showed that the Darlington leakage amplification effect can be significantly reduced using triple-well diode string ESD power clamps [12–14]. A first advantage of this triple-well ESD power clamp is the elimination of the leakage amplification. A second advantage is the lack of parasitic interaction of adjacent elements due to the isolating sub-collector and DT structure. A third advantage is the ESD design layout density advantages. With the DT structure, the density between the successive stages are limited to DT to DT spacings. Additionally, the usage of DT limits the out-diffusion of the sub-collector, providing a denser triple-well ESD power clamp design. A disadvantage of the DT-bound ESD power clamp is the usage of a DT structure increases the substrate thermal impedance. Hence, the power-to-failure will be impacted by the self-heating in the surface region. This can be reduced by using multiple-finger STI-defined p^+ elements to widen the trench opening, reducing the impact of the trench structure.

Using a bias network, a new triple-well ESD power clamp can be formed [11,15]. The bias network can electrically connect to the *n*-type isolating structure but is electrically disconnected from the diode string current path through the diode elements. Using a separate voltage biasing network, the triple-well isolation region can be connected to a separate voltage condition (Figure 9.8). Wu and M. D. Ker showed that using a bias network, a higher blocking voltage and lower leakage current can be achieved (e.g., compared to the case of a ‘‘floating’’ *n*-band triple-well structure). Without biasing, excess substrate current is evident at voltage levels of 0.5 V. With biasing the *n*-band structure, the excess substrate current can be reduced to over 1.5 V conditions. Wu and Ker also showed that a lower turn-on voltage is

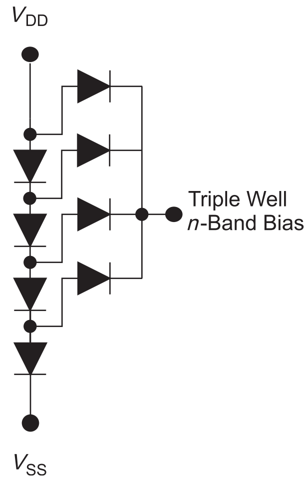

Figure 9.8 Triple-well ESD power clamp network with independent *n*-band voltage bias

present when the *n*-band network is not electrically biased in the triple-well ESD power clamp structure. Wu and Ker showed that as more diode elements are added, the series on-resistance increases [15]. But as the number of stages increases, the ESD robustness of the structure does not degrade [15]. An advantage of this *n*-band biased triple-well ESD power clamp is the reduction of the excess substrate current (compared to the floating *n*-band ESD power clamp). A second advantage is that by separating the isolation region from the series diode elements, the successive diode stages can be physically merged, reducing design area. The design area between successive stages of the diode elements is limited to the width of the edge isolation region (e.g., *n*-well width).

9.2.6 ESD Power Clamps: SOI Series Diodes ESD Power Clamps

In SOI, V_{DD} to V_{SS} ESD power clamps are needed between the power supply [16–19]. In SOI technology, there is no vertical *p–n* diode or vertical parasitic *pnp* element for discharging of ESD currents. Because of the lack of the vertical *p–n* diode element, lateral SOI gated diode structures, as discussed in Chapter 5, can be utilized for SOI ESD power clamps. The SOI lateral gated diode power clamp can consist of the following elements:

- Lateral SOI gated *p–n* diode element.
- SOI body- and gate-coupled diode-configured MOSFET element.

In the first case, the lateral SOI diodes are configured in a series configuration, with the gate electrode connected to the *n*-type cathode [16]. With a number of diode elements in series, the anode-to-cathode voltage is reduced, minimizing the concern for gate

over-voltage within the SOI diode structure. With the lack of the vertical *pnp* bipolar parasitic (as in bulk elements), there is no ideality concern with the turn-on voltage. Additionally, a second parallel series of elements are placed in the opposite direction to achieve bidirectional current flow.

In the case of the SOI body- and gate-coupled diode-configured MOSFET element, two electrical nodes exist [17–19]. The MOSFET body, source, and gate are electrically connected as one terminal, and the MOSFET drain is connected as the second terminal. In this configuration, elements can be configured in series between the two power supplies. Additionally, a second parallel series of elements are placed in the opposite direction to achieve bidirectional current flow.

9.3 ESD POWER CLAMPS: MOSFET-BASED

9.3.1 CMOS RC-Triggered MOSFET ESD Power Clamp

In CMOS technology, MOSFET-based ESD power clamps have become a standard ESD design practice in chip design. In early implementations, grounded-gate NMOS (GGNMOS) ESD network were utilized as ESD power clamps. When a MOSFET undergoes MOSFET second breakdown, non-uniform conduction occurs; this leads to inadequate predictability as well as lack of ESD protection scaling with the MOSFET width. RC-triggered MOSFET ESD power clamps introduced two concepts:

- Gate coupling.
- Frequency triggering.

There are a number of advantages which has lead to the widespread introduction of RC-triggered MOSFET ESD power clamps. These advantages are as follows:

- Frequency triggered.
- Compatibility with CMOS technology.
- Design integration with digital circuits.
- Use of supported MOSFET devices (e.g., non-use of parasitic devices).
- Circuit simulation.
- Scalable.
- Utilization of single-gate and dual-gate oxides.
- Latchup immune.

Frequency-triggered networks have the advantage that they are not dependent on the turn-on voltage. Voltage triggered ESD power clamps have a delay of operation until a certain dc voltage level is achieved. Frequency-triggered ESD power clamps are ac responsive instead of a dc voltage level.

RC-triggered MOSFETs are compatible with CMOS technology. The basic elements are scaled with every technology generation, and are compatible with digital CMOS circuitry. The compatibility with CMOS digital logic and memory prevents any additional integration issues (e.g., 1/*f* noise, voltage level incompatibility, scaling).

RC-triggered MOSFET ESD power clamps do not use parasitic elements. ESD solutions that utilize parasitic devices (e.g., parasitic *pnp*, *npn*, diodes, etc.) are typically not supported with characterization, device models, circuit simulation models, scalable, and are not well controlled in a manufacturing environment.

By using MOSFETs, in a low voltage regime, MOSFET device current models exist. As a result, the RC-triggered MOSFET ESD power clamps can be simulated using circuit simulation; in these ESD power clamps MOSFET device simulation (e.g., ambient and/or electro-thermal simulation) is not required to demonstrate operability of the ESD network. Electrical characterization, device models, and circuit models in the low-voltage regime (e.g., below avalanche breakdown) can be used to demonstrate operability of the MOSFET power clamp. In this fashion, the ESD design synthesis including the ESD network, the power bussing, and the ESD networks can be completed using circuit simulation. High-voltage, electro-thermal device simulation, and electro-thermal circuit simulation can be avoided.

Using RC-triggered MOSFET ESD power clamps, these structures scale with the technology generation. Many ESD power clamp solutions do not contain scalable trigger conditions (e.g., Zener diode, SCR, MLSCR ESD power clamps). With a scalable ESD design solution, design migration through technology generations or design ‘‘shrinks’’ is simplified.

With the MOSFET scaling and mixed-voltage interface environments, the gate dielectric scaling can be addressed by producing series cascode RC-triggered ESD power clamps, or utilize both single-gate and dual-gate oxides.

CMOS latchup is a concern in CMOS technology. RC-triggered MOSFET ESD power clamps typically are CMOS latchup immune and do not introduce CMOS latchup concerns in the digital segments of a semiconductor chip design.

RC-triggered MOSFET ESD power clamps consist of the following elements:

- RC-frequency discrimination circuit.
- Inverter drive circuit.
- MOSFET output clamp element.

In the RC-frequency discriminator circuit, resistor and capacitor elements are needed to form the RC discriminator network. The ‘‘resistor’’ elements can be supported resistor elements (e.g., *p*-type, *n*-type, polysilicon) or MOSFETs in an ‘‘on’’ state. Capacitor elements can be MOSFET capacitors (MOSCAP), metal-insulator-metal (MIM) capacitor, varactors, hyper-abrupt varactors, or other capacitor structures.

The inverter drive circuit is formed using a series of inverter elements between the RC-discriminator circuit and the MOSFET output clamp element. The role of the inverter drive circuit has two roles; first, it isolates the frequency discrimination circuit from the MOSFET output clamp, and second, it drives the MOSFET output clamp MOSFET gate voltage level. In the first issue, without the inverter drive stage, the output capacitance of the MOSFET clamp would be in parallel with the capacitor element; this would change the frequency response of the network as the MOSFET output clamp MOSFET width was varied. In the ideal implementation, the RC-trigger discriminator is

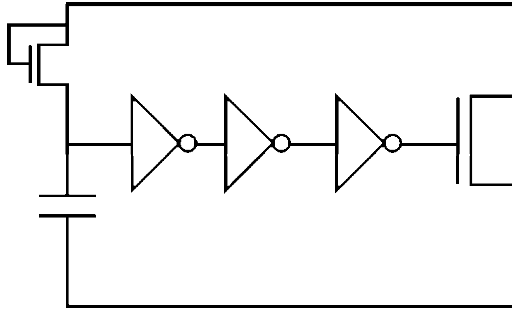

Figure 9.9 RC-triggered MOSFET ESD power clamp

isolated from the output. Second, to drive the MOSFET output clamp, the size of the inverter stages increases to provide adequate drive strength for the MOSFET output clamp gate capacitance.

In this circuit, using additional MOSFET device elements, the operability of the RC-triggered MOSFET clamp can be further improved. Additional design objectives include the following:

- Desensitize inverter stage during ESD events due to power bus voltage drops, noise triggering, power-up, and oscillations.
- Improved triggering and logic control.
- Improve the stand-by power consumption and leakage.

In this network, it is desirable to prevent false triggering, noise triggering, and power supply reduction can be prevented by using resistive elements in the inverter stage. These elements serve as a means to desensitize to noise, and provide a level-shift element (e.g., shifts the inverter switching condition).

To improve the triggering and logic control during ESD events, feedback elements can be used in the inverter drive stage. One solution is to use resistor feedback elements between the input and output of alternating inverter stages. A second solution is to use feedback "keeper" network (e.g., half-latch network) in the inverter stages to improve inverter stage response. Additionally, MOSFETs can be placed between the driven signal node and the power rails which hold the logic state during chip operation.

Since the RC-triggered MOSFET power clamp is large, it can contribute to semiconductor "off" state power consumption. This can be addressed using isolated well structures, triple-well, or dynamic threshold control of the MOSFET body.

Figure 9.9 shows an RC-triggered MOSFET power clamp. A MOSFET and capacitor element are used as the RC-discriminator circuit. The RC discriminator is activated by the ESD pulse. This signal is transmitted to the inverter stages that drive the MOSFET to discharge the ESD current. In this design, the size of the inverters are designed to avoid false triggering of the RC-triggered network.

Table 9.1 shows the HBM and MM ESD results as a function of MOSFET width. When the correct RC time is established, the circuit ESD response improves with structure size. In this structure, the design was increased in MOSFET total width by the addition of parallel

Table 9.1 RC-triggered MOSFET ESD results as a function of MOSFET width

Type	Size (μm)	HBM (kV)	MM (kV)
RC MOSFET			
	1000	2.3	0.3
	2000	3.8	0.6
	4000	10.00	1.15
	8000	>10	1.75

MOSFET fingers. As the MOSFET width increased, the HBM and MM ESD failure levels increased.

In the optimization of the RC-triggered ESD power clamp, the correct resistor–capacitor value is required to observe the increase in the ESD results with the MOSFET width. Figure 9.10 shows an example where the capacitor element size was varied. In both cases, the ESD power clamp results increased with MOSFET width. The RC-triggered MOSFETs were optimized to find the best point of operation. From these results, the MOSFET achieves less than 2.5 V/μm.

9.3.2 Mixed-Voltage Interface RC-Triggered ESD Power Clamp

In a mixed-voltage interface environment, the peripheral power supply rail can exceed the native power supply voltage. In the case that two or multiple power supply voltages exist on a common semiconductor chips, the ESD power clamps must be able to withstand the voltage conditions without degradation. For CMOS or BiCMOS applications that utilize MOSFET-based ESD power clamps, MOSFET device dielectric breakdown, or MOSFET hot electron degradation must not occur. In an RC-triggered power clamp, all elements are potentially subject to electrical overstress. For example, the resistor, the capacitor, the inverter stages, and the output clamp must avoid electrical overstress from the functional

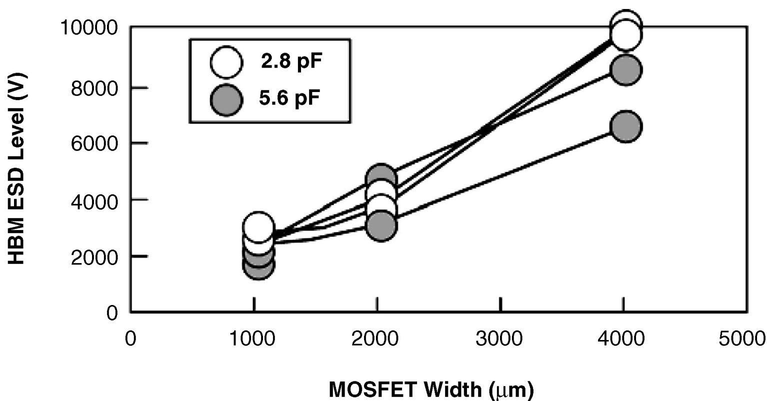

Figure 9.10 RC-triggered MOSFET ESD clamp with different RC values

voltage conditions, reliability-accelerated voltage stress, and ESD conditions. To provide RC-triggered MOSFET ESD power clamps in a mixed-voltage environment, two ESD design strategies can be incorporated:

- Additional ESD device elements are to be placed between the peripheral power supply voltage conditions, and the native power supply voltage V_{DD} to "level shift" the voltage state on the RC-triggered MOSFET network rail clamp.
- Utilization of "ESD Dummy Power Rails" within the ESD current path to avoid electrical connection to the higher power supply voltages.
- Utilization of dual-gate MOSFET (e.g., thick oxide MOSFETs) and triple-gate MOSFET devices in the RC-clamp and inverter structures.

In the first case, the use of additional elements in series with the RC-triggered MOSFET power clamp allows for the utilization of the native power supply RC-triggered network that is used in the core networks. The use of the additional elements serve the purpose as a voltage level shifting element during normal functional conditions. The type of elements that can be utilized can be series diode elements or MOSFET elements.

Figure 9.11 shows an example of a mixed voltage interface RC-triggered MOSFET ESD power clamp using a MOSFET in an "on" state to lower the voltage stress. In this implementation, the MOSFET gate is connected to the MOSFET drain. The MOSFET drain is connected to the higher power supply voltage and the MOSFET source is connected to the RC-triggered MOSFET power clamp power rail. In this configuration, the MOSFET level-shifting element serves a means to provide a voltage drop between the higher voltage power supply node and the power rail of the RC-triggered MOSFET. The level-shifting MOSFET is an "on-state" and provides a voltage drop to lower the voltage on the RC-triggered MOSFET power rail. In this implementation, the level-shifting element reduces the voltage stress on the RC-trigger discriminator network, the inverter drive network, and the output clamp device. Another perspective is that the element serves as a transmission gate whose gate is tied to the input voltage (e.g., whose transmission is the $V_{DD} - V_T$). Without the "level-shifting" element (e.g., or transmission gate), the power rail

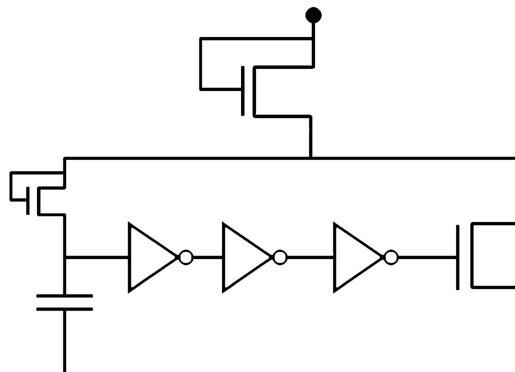

Figure 9.11 Mixed-voltage interface RC-triggered MOSFET ESD power clamp using a MOSFET level-shifting element

of the RC-triggered clamp can be integrated with the core V_{DD} power supply. In this fashion, the power rail is separated, and serves as a pseudo-V_{DD} dummy rail for the ESD power clamp network. Another perspective of this network is that the two MOSFETs output clamp device are in a series-cascode configuration, where the first MOSFETs gate is set to an ‘‘on’’ state and the second element is RC-triggered (e.g., akin to a mixed voltage *n*-channel MOSFET pull-down segement of an OCD). This network was first implemented into CMOS logic ASIC environment which supported both 3.3 and 2.5 V power rail conditions (D. Stout, J. Sloan, J. Pequignot, and S. Voldman).

In order for this ESD network to provide good ESD protection, the ESD level-shifting element must not limit the ESD robustness of the network as the size of the MOSFET output clamp width increases. Experimental results show that if the MOSFET output clamp width is increased, while the MOSFET level-shifting element remains fixed in width, the ESD results do not increase with increasing MOSFET output clamp width. But, if the MOSFET level-shifting element width increases with the MOSFET output clamp width, the ESD results are not limited by the MOSFET level-shifting element and the ESD results are as good as the RC-triggered clamp without a MOSFET level-shifting element. Hence, an ESD design practice for this network is that the MOSFET level-shifting element must scale with the MOSFET output clamp element in order to achieve improved results with MOSFET output clamp width.

T. J. Maloney and S. Dabral provided an alternative implementation that used two *p*-channel MOSFETs in a series-cascode configuration. In this implementation, both series MOSFETs were gate-coupled and initiated by an RC-discriminator circuit [31]. In the implementation, the MOSFET gate structures are turned ‘‘on’’ by the ESD pulse. *p*-Channel MOSFETs have the advantage of avoiding MOSFET snapback during over-voltage conditions, but have the disadvantage of a lower current drive and decreasing threshold voltage at higher temperatures (Figure 9.12).

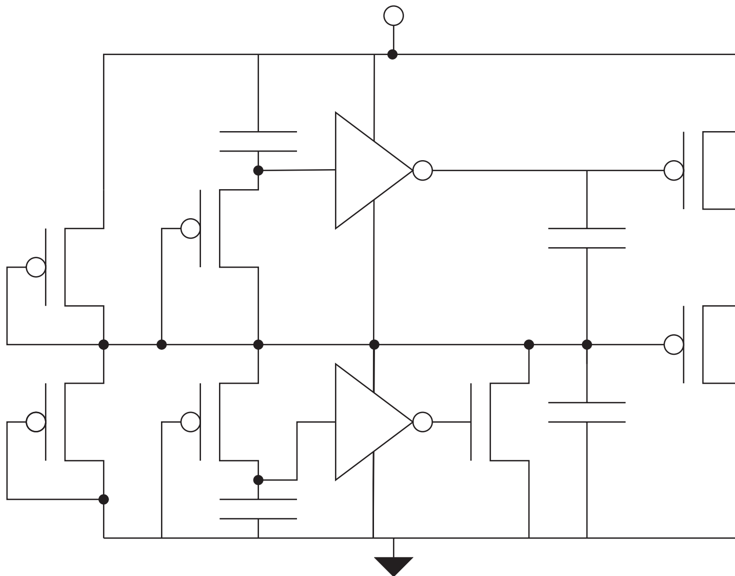

Figure 9.12 Series cascode RC-triggered *p*-channel MOSFET ESD power clamp

Another alternative implementation is the use of dual-gate MOSFET devices in the RC-triggered MOSFET ESD power clamp. The dual-gate MOSFET device can be integrated into the RC-discriminator network, the inverter stages, and the MOSFET output clamp. Typically, the dual-gate MOSFET device has a longer MOSFET channel length. The dual-gate MOSFET channel length decreases the MOSFET output clamp current drive as well as increasing the MOSFET channel on-resistance. Experimental results show that the ESD HBM voltage per unit MOSFET width is lower for the dual-gate MOSFET compared to the single-gate oxide MOSFET in an RC-triggered MOSFET ESD power clamp. Hence, there is a tradeoff between the single-gate oxide MOSFET RC-triggered implementation with level-shifting element as opposed to a dual-gate oxide MOSFET RC-triggered MOSFET clamp network.

9.3.3 Voltage-Triggered MOSFET ESD Power Clamps

ESD power clamps can be triggered by either frequency or the voltage or current conditions. In some applications, frequency-triggered networks are not preferred. Applications where voltage triggering is preferred as follows:

- RF applications which do not desire an RC frequency pole in the circuit network.
- Applications with inductive loads on the power grid structure.

In the first example, RF designers may not want additional frequency poles in the signal response. RC networks can modify the stability of an RF circuit. With the additional RC response, the frequency response of the power grid and the semiconductor chip may be influenced in small circuit number and small chip applications. The RC network can influence the stability criteria in a circuit network.

In the second case, inductive loads in peripheral circuits can interact with RC trigger network leading to chip and peripheral circuit LRC oscillations that impact functionality, or LC oscillations that affect the operability of the ESD power clamp.

A voltage-triggered MOSFET ESD-triggered power clamp does not have the concerns of the RC-triggered ESD power clamp. In these implementations, the voltage triggering can be established by different trigger networks:

- Resistor divider trigger network.
- Diode string-resistor trigger network.

Figure 9.13 shows an example of a voltage-triggered MOSFET ESD power clamp. In the second case, a diode string is placed in series with a resistor element placed between the V_{DD} and V_{SS} power rails. The center node of the trigger network is electrically connected to a series of inverters; the output of the inverters is connected to the MOSFET gate electrode which initiates the ESD discharge between V_{DD} and V_{SS}. When an over-voltage condition is established, the diode string trigger element is initiated leading to the increase in the voltage at the first inverter input; this initiates the inverter stage, leading to gate coupling of the MOSFET power clamp element.

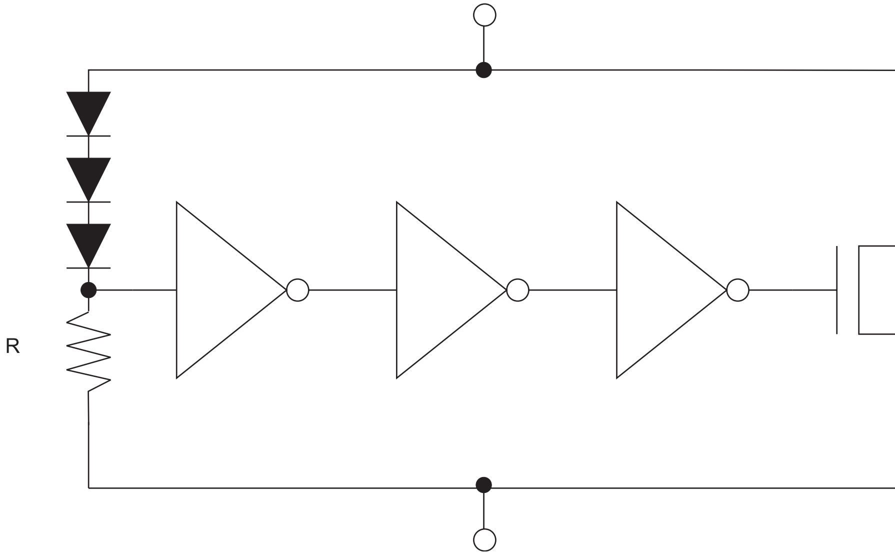

Figure 9.13 Voltage-triggered MOSFET ESD power clamp

9.3.4 Modified RC-Triggered MOSFET ESD Power Clamps

ESD power clamps must insure during functional operation to introduce false triggering during power-up, power sequencing, or power-down of the power supply rails, chip, or system. Additionally, during functional operation of the semiconductor chip or system, it must be insured that the MOSFET output clamp is in an ‘‘off’’ state or a state that introduces leakage currents and off-state power consumption. Additionally, the rise in the gate potential can lead to MOSFET gate over-voltage. ESD design practices to reduce false triggering, introduce gate modulation, or reduce ‘‘off’’ state leakage are as follows:

- Half-latch keeper network in the inverter stage.
- Resistor feedback between successive inverter stage.
- Gate modulation element.
- MOSFET substrate body biasing.

Using MOSFET half-latch networks (e.g., also referred to as ‘‘keeper’’ networks), the feedback voltage states between the input and output stages can be improved. J. Smith and G. Boselli introduced half-latch concepts into the inverter stages of the RC-triggered MOSFET network [32]. J. Smith used a *p*-channel MOSFET pull-up keeper and an *n*-channel MOSFET pull-down keeper devices for the last inverter stage, establishing feedback between the output and the input of the inverter stage; this introduces a full ‘‘latch’’ prior to the MOSFET output transistor element. J. Smith and G. Boselli demonstrated a reduction in

the ESD power clamp leakage, a reduction in the total design area, and developed an ESD power clamp which is tolerant to fast power supply ramp rates.

T. J. Maloney, S. Poon, and L. Clark also addressed the issue of leakage reduction introduced in the ESD power clamps by controlling the output clamp element body bias [38]. By using a MOSFET body-bias network, the output MOSFET power clamp body potential is modulated during off-state to reduce sub-threshold leakage currents. Maloney, Poon, and Clark demonstrated that this solution reduces sub-threshold leakage at high temperature and application voltage corners [38].

9.3.5 RC-Triggered MOSFET ESD Power Clamps Placement

A second ESD design practice focus area is the placement and synthesis of the RC-triggered MOSFET power clamps into a semiconductor chip [33–36]. It has been well known that as the distribution of ESD power clamps are placed with an increased frequency, the ESD input distribution improves in terms of the mean and the width of the distribution; not only does the total ESD pin Gaussian mean increase, but also the ESD pin Gaussian standard deviation. C. Torres [33], M. Stockinger [34], and P. Juliano [36] demonstrated the value of distribution of ESD power clamps, and the influence of bus resistance. From this work, an ESD design practice can be defined as follows:

- Distribution of ESD power clamps leads to a lower input pin-to-power clamp resistance.
- Distribution of ESD power clamps leads to a lower input pin-to-power clamp resistance distribution.

9.4 ESD POWER CLAMPS: BIPOLAR-BASED

9.4.1 Bipolar ESD Power Clamp: Voltage-Triggered ESD Power Clamps

Bipolar ESD power clamps can be initiated using different triggering methods [39–49]. These can include frequency-triggering, capacitance-coupling triggering, and voltage-triggering. Voltage-initiated triggered ESD power clamps can utilize the forward biased networks or reverse biased voltage breakdown networks. Voltage-triggered Bipolar ESD power clamps typically contain a bipolar transistor between the first and second power rail where the first power rail is electrically connected to the bipolar transistor collector, and the second power rail is electrically connected to the bipolar transistor emitter. A bias resistor element is electrically connected to the base of the output clamp device. The bias resistor sets the base to a low potential to prevent the ‘‘turn-on’’ of the output clamp. Examples of a voltage-triggered Bipolar ESD power clamps can consist of the following trigger networks:

- Forward bias diode series configured voltage trigger.
- Forward bias diode Schottky diode configured voltage trigger.

- Zener breakdown voltage trigger.
- Bipolar collector-to-emitter breakdown voltage (BV_{CEO}) trigger.

In all these cases, the output clamp takes advantage of the current-carrying capability of a bipolar output clamp element that can discharge the current from a first to a second power rail. Additionally, when the voltage condition is reached, the trigger current serves as base current to the bipolar output clamp element, initiating the discharge of the ESD event.

9.4.2 Bipolar ESD Power Clamp: Zener Breakdown Voltage-Triggered

For a voltage-triggered Bipolar ESD power clamp, where the voltage trigger is associated with a breakdown voltage of a Zener diode structure, the conditions for triggering the circuit are different from the grounded-base ESD power clamp (Figure 9.14). In this implementation, the current flowing through the Zener diode structure must be taken into account in the voltage and current equations.

Expressing the current through the structure and the Zener diode structure

$$I = MI_C + I_D$$

The bipolar output clamp collector current can be represented by the product of the collector-to-emitter transport efficiency and the emitter current, and the generation current. The total current through the structure can be represented as

$$I = M\left(\alpha I_E + I_{gen}\right) + I_D$$

Zener-triggered ESD networks have a high trigger voltage. This is an advantage for high-voltage applications, but has limited value for an advanced CMOS technology, a BiCMOS technology, or an advanced bipolar technology. Given the scaling of the bipolar output transistor, the triggering of the Zener diode must be below the avalanche breakdown

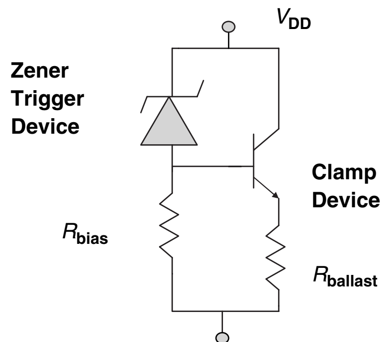

Figure 9.14 Zener-triggered ESD power clamp

of the output device when utilized as an ESD power clamp. Given the Zener trigger breakdown voltage is above the avalanche condition of the ESD output clamp device, the ESD power clamp will not scale with the output clamp total perimeter. As a result, this network has value in high voltage applications, or ESD networks that have bipolar transistors with high avalanche conditions (e.g., BV_{CER} or BV_{CEO} exceeds the Zener trigger voltage).

9.4.3 Bipolar ESD Power Clamp: BV_{CEO} Voltage-Triggered ESD Power Clamps

A bipolar-based ESD power clamp that utilizes the breakdown of a bipolar transistor in a collector-to-emitter configuration can be synthesized using a first transistor for the trigger element and a second transistor as the output clamp device. A BV_{CEO} voltage-triggered bipolar ESD power clamps contains an output bipolar transistor between the first and second power rail where the first power rail is electrically connected to the bipolar transistor collector, and the second power rail is electrically connected to the bipolar transistor emitter. A bias resistor element is electrically connected to the base of the output clamp device. The bias resistor sets the base to a low potential to prevent the ‘‘turn-on’’ of the output clamp.

Bipolar BV_{CEO} breakdown voltage-triggered ESD power clamp in bipolar and BiCMOS technology have ESD advantages as follows:

- Low trigger voltages conditions.
- Scalable.
- Compatibility and design integration with analog and radio frequency (RF) circuits.
- Compatibility with bipolar transistors.
- Use of supported bipolar transistor (e.g., non-use of parasitic devices).
- Circuit simulation.
- Utilization of multiple transistors.
- Low noise source.
- Use for positive or negative polarity power supplies.

The BV_{CEO} breakdown voltage-triggered ESD power clamp can utilize a transistor in a common-emitter mode and initiates the output clamp at this voltage condition. A unique aspect of this implementation is by using the BV_{CEO} condition, there is an inherent inter-relation with the unity current cutoff frequency of the transistor. From the Johnson Limit relationship, in its power formulation is given as

$$(P_m X_c)^{\frac{1}{2}} f_T = \frac{E_m v_s}{2\pi}$$

where P_m is the maximum power, X_C is the reactance $X_c = 1/2\Pi f_T C_{bc}$, f_T is the unity current gain cutoff frequency, E_m is the maximum electric field, and ν_s is the electron saturation velocity. Expressing as the product of the maximum voltage, V_m, and the cutoff frequency

$$V_m f_T = \frac{E_m v_s}{2\pi}$$

Hence from the Johnson Limit equation

$$V_m^* f_T^* = V_m f_T = \frac{E_m v_s}{2\pi}$$

where $V_m^* f_T^*$ is associated with a first transistor and $V_m f_T$ is associated with a second transistor. The ratio of breakdown voltages can be determined as

$$\frac{V_m^*}{V_m} = \frac{f_T}{f_T^*}$$

Using this Johnson relationship (Figure 9.15), an ESD power clamp can be synthesized where a trigger device with the lowest breakdown voltage can be created by using the highest cutoff frequency (f_T) transistor and a clamp device with the highest breakdown device will have the lowest cutoff frequency (f_T).

As shown in the Chapter 7, a BV_{CEO} breakdown voltage-triggered bipolar power clamp can be synthesized from this relationship between the power supplies. In this configuration, ESD power clamp is in a common-collector configuration. For this configuration to be suitable as an ESD power clamp, we can take advantage of the inverse relationship between the BV_{CEO} breakdown voltage and the unity current gain cutoff frequency, f_T, of the device. For an ESD power clamp, the ESD output clamp device must have a high breakdown voltage

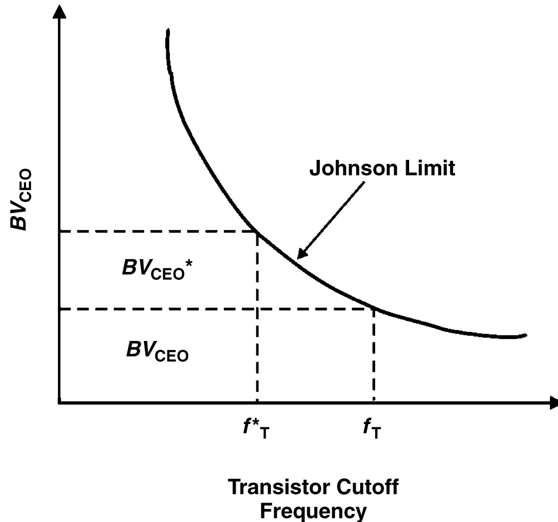

Figure 9.15 Johnson Limit relationship of BV_{CEO} versus f_T relationship

in order to address the functional potential between the V_{CC} power supply and ground potential. This ESD power clamp requires an f_T value above the ESD pulse frequency to discharge the current effectively. For the Bipolar trigger device, a low BV_{CEO} breakdown voltage device is needed in order to initiate base current into the clamp device at an early enough voltage.

This circuit can be constructed in a homo-junction silicon bipolar junction transistor (BJT), or a silicon germanium, silicon germanium carbon, or gallium arsenide hetero-junction bipolar transistor (HBT) technologies. The bipolar-based BV_{CEO}-triggered ESD power clamp trigger network consists of a high f_T SiGe HBT with a bias resistor (Figure 9.16). When the transistor collector-to-emitter voltage is below the breakdown voltage, no current is flowing through the trigger transistor. The bias resistor holds the base of the SiGe HBT clamp transistor to a ground potential. With no current flowing, the output clamp can be visualized as a "grounded base" *npn* device between the power supplies. When the voltage on V_{CC} exceeds the collector-to-emitter breakdown voltage, BV_{CEO}, in the high f_T SiGe HBT, current flows into the base of the SiGe HBT high breakdown device. This leads to discharging of the current on the V_{CC} (or V_{DD}) power rail to the V_{SS} ground power

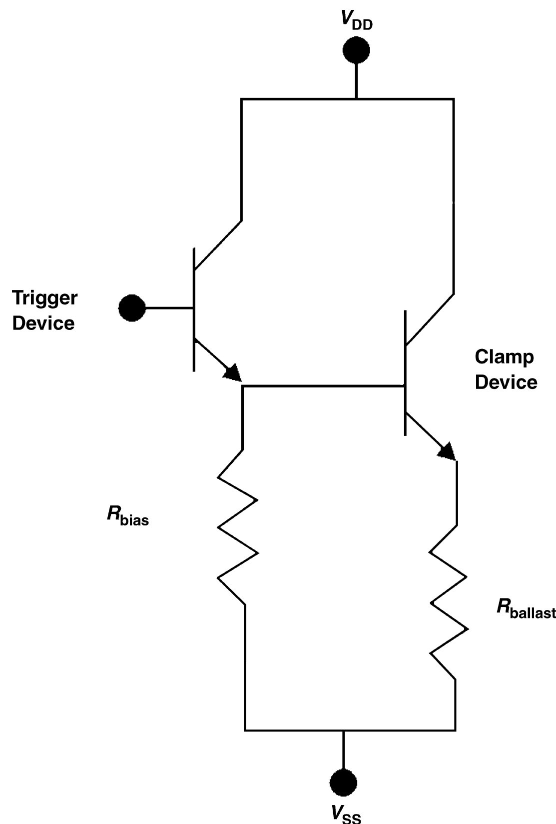

Figure 9.16 SiGe HBT ESD power clamp

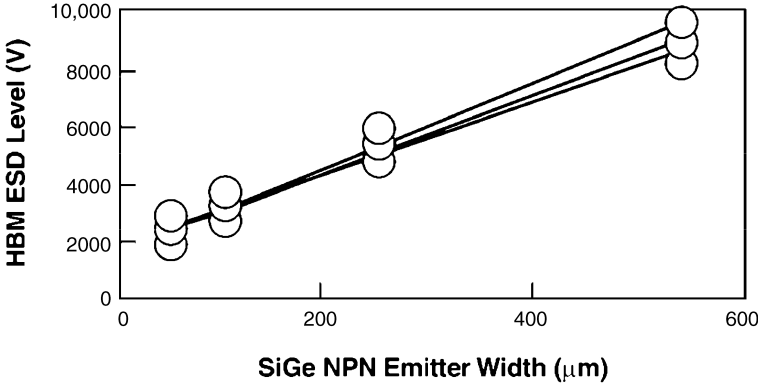

Figure 9.17 BV_{CEO} breakdown triggered SiGe HBT Darlington clamp with a low-voltage BV_{CEO} trigger and high clamp element as a function of structure size

rail. Without the initiation of the trigger element, the circuit will trigger at the BV_{CER} condition,

$$BV_{\mathrm{CER}} = BV_{\mathrm{CBO}} \sqrt[n]{1 - \frac{\alpha}{1 + \frac{kT}{q}\frac{1}{R_{\mathrm{bias}}}\frac{1}{I_{\mathrm{E}}}}}$$

As the bias resistor value increases, eventually, the clamp voltage will begin to appear as an "open-base" type condition. Applying the development of M. Reisch [44] for open-base common-emitter configuration, for our open-base trigger element, the collector current equals the emitter current with the condition of

$$I_{\mathrm{C_{Trigger}}} = I_{\mathrm{E_{Trigger}}} = \frac{MI_{\mathrm{co}}(1+\beta)}{1-\beta(M-1)}$$

where the current gain is the current gain of the trigger device. This current serves as the base current to the bipolar power clamp output transistor. In the condition that the clamp is not in an avalanche state, and the trigger device is the current through the clamp is

$$I_{\mathrm{C_{Clamp}}} = \beta_{\mathrm{Clamp}} \frac{MI_{\mathrm{co}}(1+\beta_{\mathrm{TR}})}{1-\beta_{\mathrm{TR}}(M-1)}$$

Figure 9.17 and Table 9.2 show HBM experimental of this network implemented in a BiCMOS SiGe technology as a function of structure size.

Resistor ballasting was introduced into this breakdown trigger by adding a resistor element between the bipolar output clamp emitter and the lower power rail. The introduction of ballasting resistors improves the thermal stability and the current distributions between the segments of the ESD power clamp. Table 9.3 compares the 216 μm SiGe HBT device with and without ballasting resistors. These results show that although the ballast resistors add more resistance in series with the SiGe HBT clamp device, the resistors improve the ESD stability from HBM pulses.

Table 9.2 HBM test results of two stage Darlington circuit with low breakdown trigger and high breakdown clamp device

Trigger	Clamp	Size (μm)	HBM (kV)
47 GHz	27 GHz		
		53.9	1.7
		108	3.1
		216	5.3
		532	8.5

Table 9.3 SiGe HBT high f_T trigger ESD power clamp w and w/o emitter ballasting resistor elements

Trigger	Clamp	HBM (kV)	HBM (kV)
47 GHz	27 GHz	Ballast resistor	No ballast resistor
		5.3	4.0
		5.4	4.2
		5.3	4.1

TLP measurements do show that the added ballast resistance does change the on-resistance slope.

Alternative ESD power clamps can be formed using the different bipolar transistors in a BiCMOS technology. For example, it is possible to use a higher BV_{CEO} trigger element in the Bipolar BV_{CEO}-triggered network. Using a high-BV_{CEO} trigger and a high-BV_{CEO} clamp device, the trigger circuit can be delayed for peripheral voltage conditions below BV_{CEO} of the SiGe HBT device (Figure 9.18). As the trigger device breakdown voltage approaches the

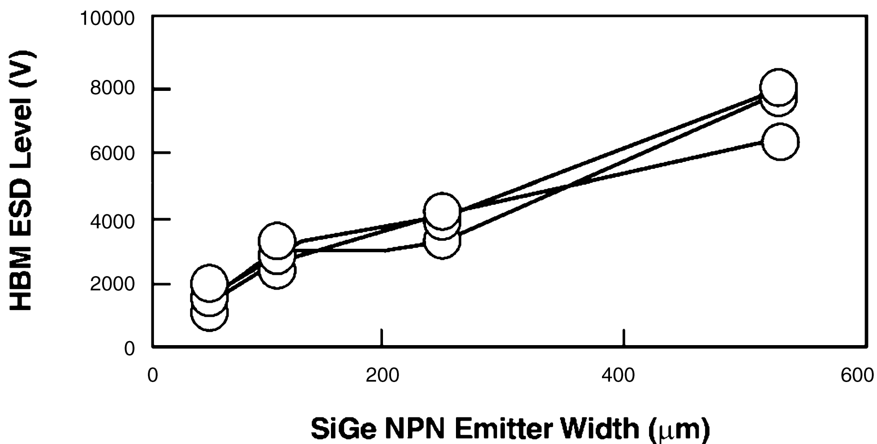

Figure 9.18 SiGe HBT Darlington clamp with a high voltage trigger and high BV_{CEO} clamp element with the emitter–base trigger open

Table 9.4 MM test results of the BV_{CEO}-triggered ESD power clamp with low breakdown trigger and high breakdown clamp device (base trigger floating)

Trigger	Clamp	Size (μm)	MM (kV)
47 GHz	27 GHz		
		53.9	0.2
		108	0.35
		216	0.60
		532	1.20

output device breakdown voltage, the trigger element may be less effective and more inconsistent in initiating a base current in the bipolar output clamp element.

These experimental results show as the trigger voltage approaches the clamp breakdown voltage BV_{CER}, the site-to-site variation increases with less assurance of the response of the trigger network. Hence, an ESD design practice in this implementation to insure ESD power clamp operation consistency is to increase the voltage margin between the trigger element and the breakdown of the clamp as large as possible in the given application.

Table 9.4 shows the MM ESD results for the BV_{CEO}-triggered SiGe HBT ESD power clamp with the high frequency/low breakdown trigger and high breakdown/low frequency clamp network with the base floating.

Figure 9.19 shows the TLP measurement of the 532 μm SiGe HBT ESD power clamp. From the TLP characteristic, the ESD power clamp trigger voltage is dependent on the BV_{CEO} of the 47 GHz SiGe HBT at approximately 4 V. In this structure, the leakage increased from 1.7 to 27 pA prior to the significant increase in the leakage current. TLP

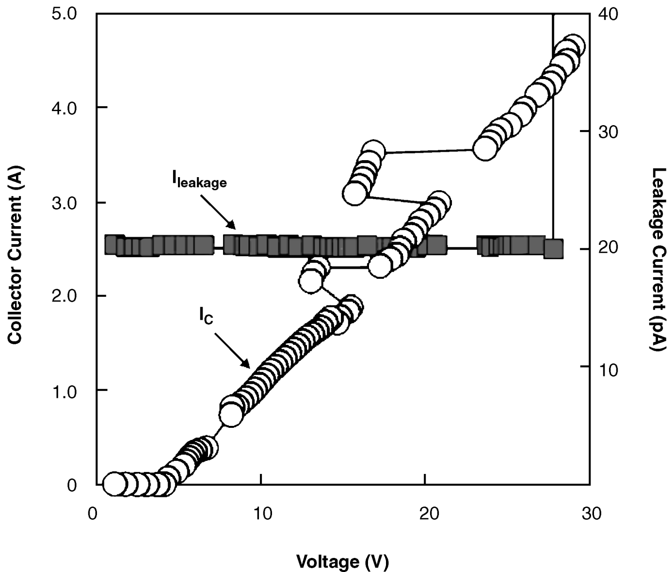

Figure 9.19 TLP *I–V* and leakage measurements of 532 μm BV_{CEO}-triggered SiGe HBT Darlington ESD power clamp

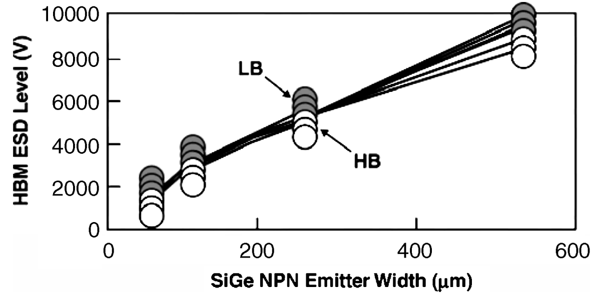

Figure 9.20 HBM results of a BV_{CEO} voltage-triggered SiGe HBT power clamp comparing a low BV_{CEO} and high BV_{CEO} clamp element with a low BV_{CE}

failure current increased with the size of the SiGe HBT device. The largest SiGe HBT multi-finger power clamp achieved is 4.4 A.

Low breakdown BV_{CEO}-triggered ESD power clamps can be used for internal core power grids or low voltage applications where a low breakdown power clamp may provide ESD advantage. Since the core power supply voltage may be significantly less than the peripheral circuitry, it is possible to lower the trigger condition and the clamp voltage prior to avalanche breakdown.

Using a high f_T SiGe HBT device for both the trigger element and the clamp element in a bipolar BV_{CEO} triggered Darlington configuration, a low-voltage ESD power clamp can be constructed. Figure 9.20 shows the SiGe HBT power clamp with the two different SiGe HBT clamp device and identical trigger elements.

9.4.4 Bipolar ESD Power Clamp: Mixed-Voltage Interface Forward-Bias Voltage and BV_{CEO}-Breakdown Synthesized Bipolar ESD Power Clamps

Bipolar ESD power clamps can consist of voltage-initiated trigger networks to initiate the ESD power clamp network. Voltage-trigger networks can be a forward-bias voltage initiated network, or a breakdown-initiated network. Given that the application voltage exceeds the breakdown voltage of a trigger element, new voltage-trigger networks can be established that synthesize both the forward-bias trigger elements and the breakdown trigger elements. Examples of ESD networks that integrate both forward-bias trigger elements and breakdown-voltage trigger elements can be as follows:

- Forward bias: Schottky diodes.
- Forward bias: p^+/n-well diodes.
- Forward bias: Polysilicon-gated diodes.
- Forward bias: Bipolar base–collector varactor.
- Reverse bias: Bipolar in collector-to-emitter configuration with base-floating (BV_{CEO}).

- Reverse bias: Bipolar in collector-to-emitter configuration with a base resistor (BV_{CER}).
- Reverse bias: Zener Diode.

When a Bipolar ESD power clamp is BV_{CEO}-initiated, the network is constrained to the Johnson Limit. The limitation of this network is that the trigger condition is constrained to the unity current gain cutoff frequency, f_T, and not suitable for I/O, mixed power supply applications or non-native implementations.

For mixed-voltage applications, the peripheral voltage is typically higher than the native voltage power supply. A new variable trigger implementation is developed where additional elements are placed in series with the trigger element. Placing diodes or varactors in series, the trigger condition can be level-shifted to a higher breakdown condition. In a diode string implementation where each element is of equal area, the turn-on condition is

$$V_T = NV_f - (kT/q)(N-1)(N/2)\ln(\beta+1)$$

where N is the number of *pnp* elements, V_f is the forward diode voltage, and β is the *pnp* current gain of the "diode" element. Various implementations can be used for the forward bias diode element

- CMOS-based p^+/n-well diode.
- Bipolar-based bipolar transistor in base–collector mode.
- Silicon–Germanium-based base–collector varactor.

For example, a SiGeC varactor structure is used in a forward-bias mode of operation. The varactor structure consists of a SiGe selective epitaxial p^+ anode and collector/sub-collector n^{++} cathode. By placing the SiGe HBT device (used in a BV_{CEO}-breakdown mode) in series with a SiGeC varactor diode string (used in a forward-bias mode), a new trigger condition is established for the circuit

$$V_T = E_m \nu_s / 2\Pi f_T + NV_f - (kT/q)(N-1)(N/2)\ln(\beta+1)$$

This trigger condition provides a set of design contours of trigger values where the number of elements and the cutoff frequency are the trigger parameters (Figure 9.21). In the

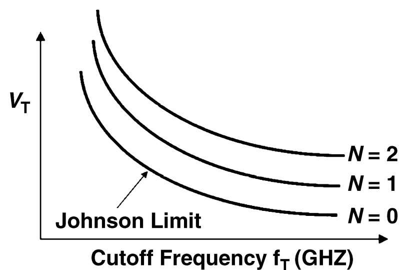

Figure 9.21 Trigger design contours as a function of series varactors and cutoff frequency

case of no extra series diode elements ($N = 0$) case, the turn-on voltage is the Johnson Limit characteristic of the relationship of BV_{CEO} and the unity current gain cutoff frequency, f_T. As the number of series diode elements increases, the ESD trigger network turn-on voltage shifts the Johnson Limit curve on the *y*-axis. In the case of an ideal diode string, the turn-on voltage would shift along the *y*-axis in equal increments associated with the ideal diode forward bias condition. But, as a result of the vertical parasitic *pnp* non-linearity factor, the net increase with each successive element is less than the ideal diode forward voltage value (e.g., $V_{be} = 0.7\,\text{V}$ at ambient temperature).

To evaluate the non-ideality factor, we can evaluate the trigger condition as a function of the number of diode elements

$$\frac{\partial}{\partial N} V_T = \frac{\partial}{\partial N}\{(E_m \nu_s / 2\Pi\, f_T) + NV_f - (kT/q)(N-1)(N/2)\ln(\beta+1)\}$$

where differentiating with respect to the number of series elements, the change in the turn-on voltage as a function of element number can be evaluated as

$$\frac{\partial}{\partial N} V_T = \left\{ V_f - \left(\frac{kT}{q}\right)\left(\frac{2N-1}{2}\right)\ln(\beta+1)\right\}$$

This expression shows that as the number of diode elements increases, there is a correction factor from the ideal which is a function of the number of elements. To evaluate the trigger voltage sensitivity as a function of the bipolar gain characteristic

$$\frac{\partial}{\partial \beta} V_T = \frac{\partial}{\partial \beta}\{(E_m \nu_s / 2\Pi\, f_T) + NV_f - (kT/q)(N-1)(N/2)\ln(\beta+1)\}$$

Differentiating with respect to the bipolar current gain

$$\frac{\partial}{\partial \beta} V_T = -\left(\frac{kT}{q}\right)\left(\frac{1}{\beta+1}\right)\frac{(N-1)N}{2}$$

As the frequency of the transistor increases, the turn-on voltage sensitivity is

$$\frac{\partial}{\partial f_T} V_T = \frac{\partial}{\partial f_T}\{(E_m \nu_s / 2\Pi f_T) + N\,V_f - (kT/q)(N-1)(N/2)\ln(\beta+1)\}$$

or the sensitivity of the trigger condition as a function of the frequency is the following

$$\frac{\partial}{\partial f_T} V_T = -\frac{E_m \nu_s}{2\pi f_T^2}$$

Figure 9.22 shows the bipolar ESD clamp, where the trigger network is represented as a series of diode elements in parallel with the bipolar trigger transistor in a collector-to-emitter configuration with the base electrode floating. For the network to be operable, the bipolar ESD clamp network must have a breakdown voltage that exceeds the trigger voltage condition. With the presence of the trigger element, the output clamp element will breakdown at the BV_{CER}-voltage condition, where the bias resistor serves as the base resistance.

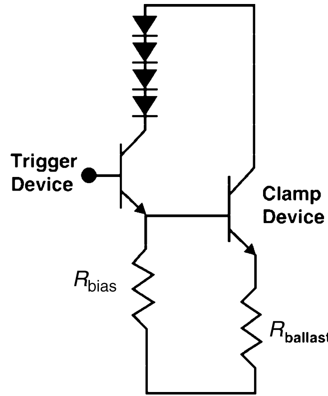

Figure 9.22 BiCMOS forward bias and BV_{CEO}-initiated trigger network bipolar ESD power clamp

The ballast resistance also establishes a base–emitter debiasing voltage state as current flows through the ballast elements.

For analysis of the operation of this mixed-voltage BiCMOS SiGe ESD power clamp, a matrix of studies varied the SiGe varactor number, the size of the output clamp, and the role of emitter ballasting resistors. To understand the operation of the circuit, HBM, MM, and TLP measurements are first taken with the case of no additional varactors. The varactor number was modified to study the variation of the ESD results with varactor number. Table 9.5 shows the HBM and MM ESD results as a function of the clamp size (emitter width). As the size of the structure increases, both HBM and MM ESD results increase. In a first observation, the comparison of a 120 GHz f_T SiGeC trigger circuit to a prior generation technology 47 GHz f_T trigger network, we find that there is no scaling impact with successive technology generation of this clamp design (Figure 9.23). Various trigger element sizes were used to evaluate the ESD robustness of the trigger networks. Evaluation of the HBM and MM results for the Bipolar ESD power clamp network trigger provided insight to the operation of the circuit. A first key discovery in the HBM, MM, and TLP experimental work of the network is that as the trigger voltage value is increased (utilizing additional ‘‘diode’’ elements), HBM and MM ESD results decrease for a fixed output clamp size. With the increased voltage turn-on of the trigger network, the ESD robustnesss of the network decreases.

Table 9.5 HBM and MM ESD results with a 120 GHz SiGeC transistor and 90 GHz SiGeC clamp device

Trigger	Clamp	Clamp length (μm)	HBM (V)	MM (V)
120 GHz	90 GHz			
		50	2500	240
		100	3100	390
		150	4700	480
		200	5000	600
		250	5900	630

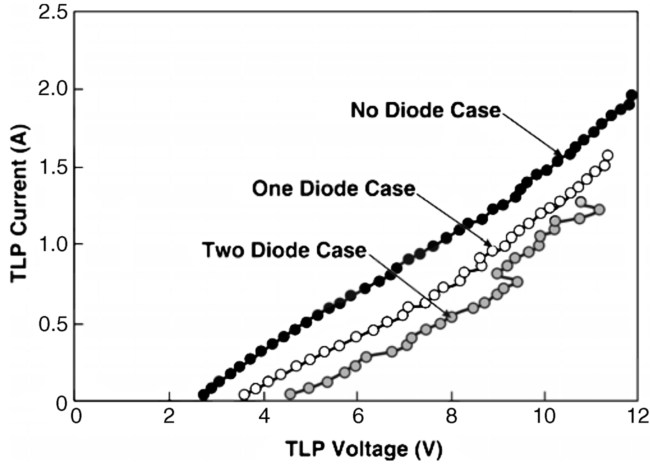

Figure 9.23 Variable trigger ESD power clamp TLP *I–V* characteristics as a function of trigger condition

Table 9.5 demonstrates the relationship between the trigger voltage condition and the HBM and MM ESD result.

Table 9.6 shows the TLP measurement of the failure current as a function of structure size and the number of SiGeC varactors in series. From the table, it can be seen that the bipolar power clamp current-to-failure decreases with the increase in the trigger voltage condition.

Figure 9.23 shows the TLP *I–V* characteristic of the bipolar ESD power clamp. Figure 9.23 shows the change in the TLP *I–V* characteristic as the trigger voltage condition is varied. The data show as the number of successive trigger elements increase, the TLP *I–V* charateristic shifts along the voltage axis (e.g., x-axis). From the data, it can also be observed that the last measurement decreases with the increasing number of series diode elements.

As the Bipolar ESD power clamp trigger voltage increases, the margin between the breakdown voltage of the output clamp and the trigger network decreases. Hence, an ESD metric of interest in this bipolar ESD power clamp circuit is the following equation, where BV_{CER} is the output clamp breakdown voltage

$$BV_{CER} - V_T = BV_{CER} - \left\{ \frac{E_m \nu_s}{2\pi f_T} + NV_f - \left(\frac{kT}{q}\right)\left(\frac{N(N-1)}{2}\right) \ln(\beta + 1) \right\}$$

Table 9.6 TLP current-to-failure of the SiGe HBT ESD power clamp as a function of the SiGe NPN clamp size and number of varactors

Clamp length (μm)	Failure current (0 Var)	Failure current (1 Var)	Failure current (2 Var)
50	0.7 A	0.72 A	0.58 A
100	1.25	1.05	1.0
150	1.7	1.5	1.3
200	1.8	1.6	1.3
250	2.1	1.6	

where

$$BV_{\mathrm{CER}} \cong BV_{\mathrm{CBO}}\left(1-\frac{I_{\mathrm{co}}R_{\mathrm{B}}}{V_{\mathrm{be}}}\right)^{\frac{1}{n}}$$

9.4.5 Bipolar ESD Power Clamp: Ultra Low-Voltage Forward-Biased Voltage-Trigger

As the faster transistors are produced in bipolar, BiCMOS SiGe, and GaAs technology, low-voltage trigger ESD networks will be required to achieve good ESD protection. It is only recently that SiGe hetero-junction bipolar transistors (HBT) devices achieved unity current gain cutoff frequency (f_{T}) levels of 120 GHz [46]. ESD solutions for the RF input nodes and ESD power clamps are key for success in RF applications. As the BiCMOS SiGe transistor is scaled, the power supply voltage is scaled, allowing for scaling of the ESD power clamp trigger condition. With the rapid scaling of the BJT and HBT devices to higher cutoff frequencies, low trigger voltage devices whose trigger condition is not limited to the Johnson limit, and can be used for power supply V_{CC} voltage may be required. In this section, the usage of bipolar-based HBT ESD power clamps whose trigger condition are not limited to, and lower than, the Johnson limit is explored.

To avoid the Johnson limit bottleneck, a forward-bias diode trigger network instead of a reverse-bias BV_{CEO} breakdown trigger network allows for the lowering of the trigger condition. Eliminating the open-base bipolar HBT BV_{CEO}-configured device trigger, and replacing the trigger circuit with a forward-bias diode voltage triggered network, the ESD design box is increased, and allows for lower trigger conditions. Figure 9.24 shows a forward-bias diode voltage-triggered bipolar ESD power clamp. In this implementation, the trigger condition can be raised by the addition of more diode elements.

In a diode string implementation where each element is of equal area, the turn-on condition reduces to

$$V_{\mathrm{T}} = N\,V_{\mathrm{f}} - (kT/q)(N-1)(N/2)\ln(\beta+1)$$

where N is the number of *pnp* elements, V_{f} is the forward diode voltage, and β is the *pnp* current gain of the "diode" element. For example, in a BiCMOS SiGeC technology, a SiGeC varactor structure can be used in a forward bias. The varactor structure can consists of a SiGe selective epitaxial p^{+} anode and collector/sub-collector n^{++} cathode. By replacing the breakdown BV_{CEO} HBT trigger device with N elements of a SiGeC varactor, a new trigger condition can be established for the circuit, where the diode string voltage is less than the breakdown voltage initiated trigger network [47]

$$NV_{\mathrm{f}} - \left(\frac{kT}{q}\right)\frac{N(N-1)}{2}\ln(\beta+1) \leq \frac{E_{\mathrm{m}}\nu_{\mathrm{s}}}{2\pi f_{\mathrm{T}}}$$

This expression can be stated in the following form

$$N\,V_{\mathrm{f}} \leq \left(\frac{kT}{q}\right)\frac{N(N-1)}{2}\ln\left(\beta_{pnp}+1\right) + \frac{E_{\mathrm{m}}\nu_{\mathrm{s}}}{2\pi f_{\mathrm{T}}}$$

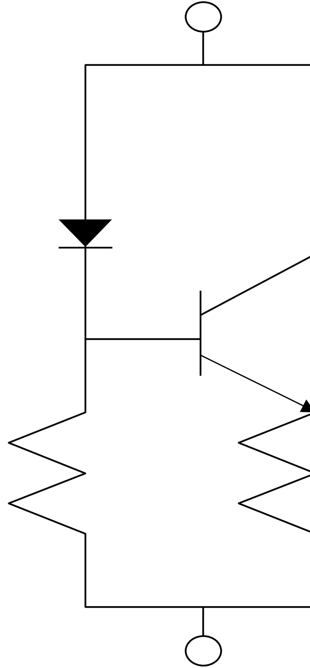

Figure 9.24 Ultra-low forward-bias diode voltage-triggered ESD power clamp

where the desired condition is a trigger circuit where the trigger is lower than the Johnson limit of the bipolar BV_{CEO} reverse breakdown trigger element. In the case of a heavily doped sub-collector, the vertical parasitic *pnp* current gain is low. In this case, the *pnp* term of the expression is small, and the inequality can be expressed as

$$V_T \approx NV_f \leq \frac{E_m \nu_s}{2\pi f_T}$$

Figure 9.25 shows a set of design curves where the new trigger condition is plotted against the Johnson condition. This trigger condition provides a set of design contours of trigger values where the number of elements and the cutoff frequency are the trigger parameters (Figure 9.25).

In the design plot, each horizontal line represents an additional diode overlaid on the Johnson limit curve. At some number of diode elements, the diode-trigger network will exceed the Johnson limit of the SiGe HBT device. Hence, the desired design space on the V_T–f_T plot is the space below the Johnson limit characteristic. The number of diodes that fulfill this relationship is the integers from zero to N where

$$N \leq \frac{E_m \nu_s}{2\pi f_T V_f}$$

For the forward-bias voltage trigger element to initiate before the output clamp element, the trigger voltage must be less than the breakdown voltage of the output clamp. The output

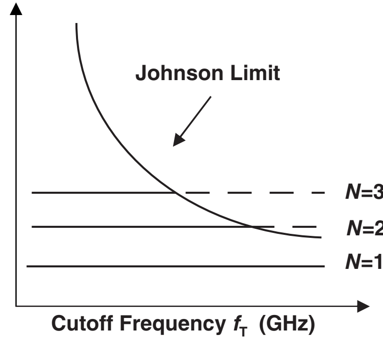

Figure 9.25 ESD power clamp design curve: trigger voltage versus unity current gain cutoff frequency (f_T) plot highlighting frequency independent design contours diode-configured implementation to the Johnson limit BV_{CEO} contour condition

clamp device is in a common-emitter configuration. For bipolar transistors, the ordering of the breakdown voltages can be expressed as

$$BV_{CEO} \leq BV_{CER} \leq BV_{CBO}$$

where we can express BV_{CEO} from BV_{CBO} as

$$BV_{CEO} = BV_{CBO}(1 - \alpha_{npn})^{\frac{1}{n}}$$

where α_{npn} is the collector-to-emitter current transport factor for the *npn* output transistor. This can be also expressed as a function of the vertical bipolar gain β_{npn},

$$BV_{CEO} = BV_{CBO}\left(\frac{1}{\beta_{npn}}\right)^{\frac{1}{n}}$$

In our network, a base resistance exists, decreasing the trigger condition below the BV_{CBO} voltage condition, known as BV_{CER}

$$BV_{CER} \cong BV_{CBO}\left(1 - \frac{I_{co}R_B}{V_{be}}\right)^{\frac{1}{n}}$$

where I_{co} is the reverse collector-to-base current, R_B is the effective base resistance. Hence, we can define the condition for a forward-bias diode triggered bipolar ESD power clamp as

$$V_T \leq \frac{E_m \nu_s}{2\pi f_T} \leq BV'_{CEO} \leq \frac{E_m \nu_s}{2\pi(f'_T)} \leq BV'_{CER}$$

where the cutoff frequency f'_T is the clamp cutoff frequency, and the clamp breakdown voltage with a resistor element is

$$BV'_{CER} \cong BV'_{CBO}\left(1 - \frac{I_{co}R_B}{V'_{be}}\right)^{\frac{1}{n}}$$

and the trigger voltage is defined as

$$V_{\mathrm{T}} = N\,V_{\mathrm{f}} - \left(\frac{kT}{q}\right)\frac{N(N-1)}{2}\ln\left(\beta_{pnp}+1\right)$$

As the transistor is scaled, the unity current gain cutoff frequency increases, leading to lower breakdown voltages of the SiGe *npn* transistor. From the expression

$$V_{\mathrm{T}} \approx N\,V_{\mathrm{f}} \leq \frac{E_{\mathrm{m}}\nu_{\mathrm{s}}}{2\pi f_{\mathrm{T}}}$$

we can anticipate that the number of series diode elements, N, must be scaled in future generations. Hence, the cutoff frequency scaling, $f_{\mathrm{T}}' = f_{\mathrm{T}}\ \alpha$, will drive the value for the scaled number of elements, N'.

As an example implementation, the forward-bias trigger ESD network was constructed in a BiCMOS SiGe technology. The structures tested in this technology contain a 200/280 GHz ($f_{\mathrm{T}}/f_{\mathrm{MAX}}$) SiGe HBT device with Carbon (C) incorporated in the raised extrinsic base region. Diode-configured SiGe HBT trigger elements are used in a SiGeC HBT power clamp network in a 200/285 GHz $f_{\mathrm{T}}/f_{\mathrm{MAX}}$ SiGe HBT technology in a 0.13-μm CMOS technology base. Voldman and Gebreselasie demonstrated the operation of the forward-bias voltage trigger diode ESD power clamp network using a 200/285 GHz ($f_{\mathrm{T}}/f_{\mathrm{MAX}}$) clamp element [47]. Figure 9.26 is a TLP *I–V* characteristic for the forward-bias diode-configured trigger SiGe ESD power clamp with two different size output clamp elements. The turn-on voltage of the ESD power clamp does not change with the size of the output clamp, but is determined by the trigger network. The ESD structure demonstrates a low-voltage turn-on at approximately 1.8 V. The turn-on voltage will be the sum of the forward-bias base-collector voltage and on-resistance of the trigger element, the forward bias emitter-base voltage and base resistance of the clamp element, as well as the voltage drop across the emitter ballasting resistor elements.

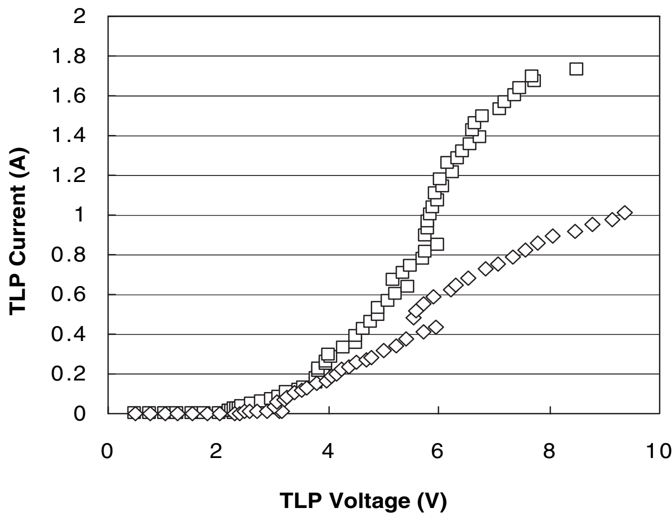

Figure 9.26 TLP *I–V* characteristic for forward-biased voltage-triggered SiGe ESD power clamp with emitter ballast resistor for a first and second structure size

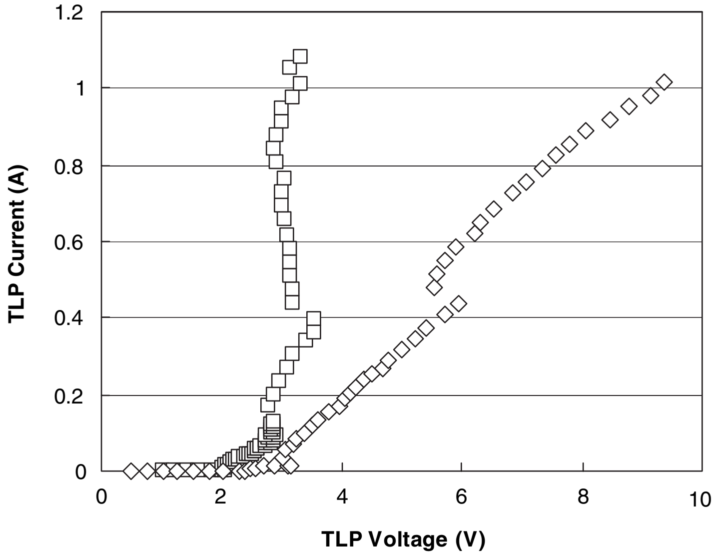

Figure 9.27 TLP *I–V* characteristic for forward-bias voltage-triggered SiGe ESD power clamp with and without emitter ballast resistor

The TLP on-resistance decreased with the larger ESD power clamp. The TLP current-to-failure increased from approximately 1.0–1.7 A as the size of the output device doubled in size, using the same size trigger element [47].

Figure 9.27 is a TLP *I–V* characteristic for the forward-biased voltage-triggered SiGe power clamp with and without the emitter ballast resistors; this demonstrates that the external emitter ballast resistor leads to a high on-resistance, and requires a higher voltage for discharging an equivalent source current from the unballasted elements. At low currents, the voltage drop across the ballast resistor is small, hence the turn-on voltage is not significantly influenced. When the bipolar ESD power clamp turn-on voltage is exceeded, the on-resistance is significantly lower [47].

9.4.6 Bipolar ESD Power Clamp: Capacitively-Triggered

In advanced RF technologies, additional ESD power clamp design considerations are required to prevent the ESD power clamps from impacting circuit characteristics. ESD power clamps that do not impact dc characteristics, such as leakage, and RF characteristics, such as gain, bandwidth, linearity, and circuit stability criteria are desired for Silicon Germanium, GaAs, and InP technologies. Additionally, these power clamps must be effective in providing improved ESD protection to the input circuitry by providing a low impedance path through the ESD current loop.

Bipolar ESD power clamps that establish a current path either through the trigger network or the output clamp element will impact the total leakage in a RF semiconductor chip. This will be significant if the total number of circuit elements in the chip is small. In high-density high-circuit count CMOS logic chips, the percentage of leakage associated with the ESD

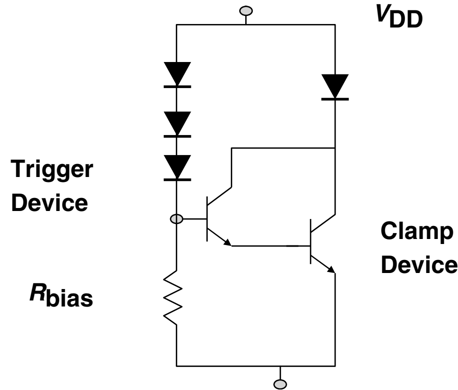

Figure 9.28 Darlington-configured ESD bipolar power clamp with a forward-bias diode trigger network

power clamps is small compared to the entire core logic leakage. In a small BiCMOS or RF semiconductor chip, where the number of total circuit elements may be small, the ESD power clamp can be a significant part of the total dissipated power.

One technique is to utilize a capacitor in series with the trigger network to prevent a direct current (dc) path through the trigger network. Using a reverse-breakdown element, or a capacitor, no current will flow through the trigger network until the breakdown voltage is achieved. In the case of a capacitor element, where the capacitance breakdown is significantly higher, the capacitor will serve as a capacitive coupling to activate the ESD bipolar network.

Y. Ma and G. P. Li compared a capacitor-triggered Darlington-configured ESD power clamp to a forward-bias diode triggered Darlington-configured ESD power clamp [48,49]. Instead of a forward-bias diode voltage trigger ESD bipolar power clamp, a capacitor element was used to replace the voltage-trigger diode string between the top node and the trigger initiation. These ESD bipolar ESD networks were constructed in a InGaP/GaAs technology.

Figure 9.28 shows a Darlington-configured ESD bipolar power clamp, with a voltage-triggered forward bias diode string network. In this ESD bipolar power clamp, when the turn-on voltage of the diode string is achieved, current will flow to the base of the first stage of the Darlington ESD power clamp. In the network, a diode is placed in series with the first and second stage Bipolar elements.

Figure 9.29 shows a capacitor-triggered Darlington ESD power clamp. The forward-bias voltage trigger diode string is replaced with a capacitor element. A capacitor is placed between the upper power rail and the base of the first stage of the Darlington ESD power clamp. In this case, when a pulse is applied, the capacitor increases the base potential leading to turn-on of the first stage of the Darlington-configured network. Y. Ma showed that the dc leakage current remains low for high levels of RF power [48,49]. As the RF power increases, the diode-string trigger network dissipates current whereas the capacitor-trigger network does not dissipate leakage current. RF simulation shows that the 3rd Order Intermodulation Product (3rd OIP) was also shown to have a larger negative value for the capacitor-triggered networks compared to the forward-bias voltage diode trigger network. From the TLP *I–V* characteristics, the capacitor-trigger network Darlington bipolar ESD power clamp was

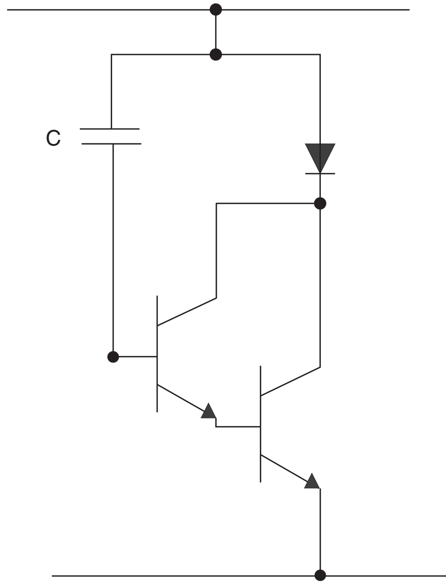

Figure 9.29 Capacitor-triggered Darlington ESD power clamp

shown to have a turn-on voltage lower than 4 V, whereas the diode-triggered Darlington maintained over 10 V. Although the trigger conditions were modulated by the trigger network type, the TLP current-to-failure was approximately equal in all cases. Hence, the trigger network influenced the RF and loading effects and the trigger voltage, but had minor influence on the net ESD robustness of the bipolar power clamp network. In this comparison, it is noted that the capacitance loading effect of the capacitor-trigger network is higher than that of the diode-triggered network; this impacts the insertion loss RF characteristic and loading effect. In the case of a ESD power clamp, this capacitive loading effect is not an issue. It was noted by Y. Ma and G. P. Li that the capacitor-triggered ESD network can be distributed within a network forming a LC transmission line, reducing the capacitive impact to a signal pin [48,49].

As an ESD design practice, the utilization of a capacitor-triggered bipolar ESD network provides the following advantages for low leakage, good linearity, and ESD protection capability. The loading effect of the capacitance can be addressed by distribution of the network and utilizing ‘‘distributed load’’ circuit design techniques.

9.5 ESD POWER CLAMPS: SILICON CONTROLLED RECTIFIER-BASED

9.5.1 Silicon Controlled Rectifier (SCR) ESD Power Clamps

Silicon controlled rectifiers (SCR) (e.g., also known as a *pnpn* device) are used as ESD power clamps between the V_{DD} power supply and ground potential. SCR devices are four

region structures; these devices can be formed from intentional devices, or parasitic devices. SCR devices can serve as good ESD power clamps because of the following features:

- High current capability (e.g., per unit micron of SCR width).
- Fast switching characteristics.
- Low capacitance.
- Voltage trigger conditions above a power supply.

SCRs serve as good ESD power clamps in the technologies whose features are as follows:

- Low doped p^- substrates or non-epi technologies.
- Single-well technology.
- Low doped *p*-well technology.
- LOCOS isolation or highly scaled shallow trench isolation (STI).
- Diffused well or low doped retrograde wells.

In CMOS technology, it is an objective to provide good CMOS latchup protection. The objective of providing a latchup robust technology was in the opposite direction of construction of an effective SCR structure. As a result, this structure was suitable for the 1980s [50–54]. During the 1980s, technology began to transition to heavily doped substrates, retrograde *n*-wells, *p*-wells, and STI. The effectiveness of these SCRs were reduced as the emphasis of technologies to eliminate CMOS latchup. New techniques were required to utilize SCRs, such as low-voltage triggering and gate-coupling ESD design techniques. But, in recent years, there is a return of the value as advanced technologies have gone to high-resistance substrates, and highly scaled isolation structures. As the CMOS latchup robustness of mainstream CMOS is decreasing, the ability to utilize SCR structures is returning with a renewed interest.

In CMOS technology, L. Avery introduced the concept of using SCR structures as ESD protection schemes [50]. R. Rountree constructed an SCR using the parasitics of a CMOS process; an SCR structure was constructed comprising a network of p^+ diffusion, an *n*-well, a *p*-substrate, and n^+ diffusion region in a LOCOS isolation technology [51]. SCR triggering was established by avalanche breakdown of the *n*-well-to-substrate junction; hence, the trigger condition was set by the *n*-well breakdown voltage. These voltages typically were in the 30–70 V range [53,54]. With the introduction of retrograde *n*-wells and p^{++} substrates, these breakdown voltages were lowered to 40 V. Unfortunately, for mainstream CMOS, these trigger voltage conditions are too high above the power supply value.

Medium-level SCR (MLSCR) structures were used to lower the triggering condition [54]. To lower the breakdown voltage of the SCR, the n^+ source/drain diffusion can be extended outside of the *n*-well region. The extension in conjunction with a second LOCOS-defined n^+ diffusion a lateral ‘‘thick oxide’’ parasitic *npn* element [54]. MLSCR trigger condition is a function of the *n*-diffusion breakdown voltage. *n*-Diffusion breakdown voltages can range from 10 to 25 V, depending on the CMOS technology. In STI, typical MOSFET source/drain breakdown voltages can be 12–18 V. Hence, MLSCR can be used in 10 V power supply applications, and have significant margin to a sub-5 V power supply.

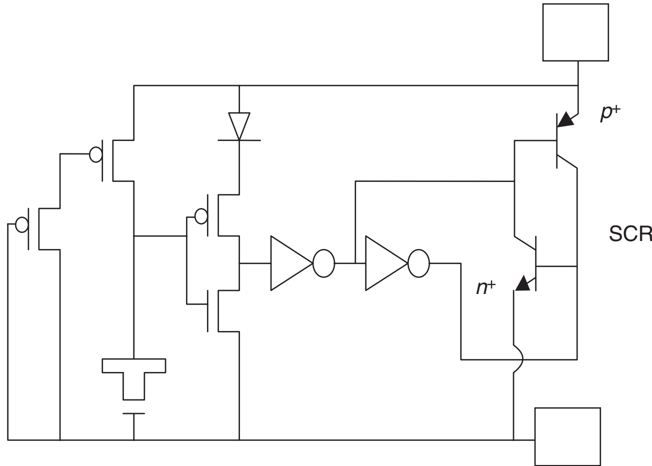

Figure 9.30 Silicon controlled rectifier ESD network using CMOS-based switching networks

To provide a lower trigger condition for low-voltage power supplies, a low-voltage trigger SCR structure (LVTSCR) is desirable. In an LVTSCR, the LOCOS isolation is removed, and a MOSFET structure is formed between the n^+ diffusion and the n^+ extension region [54]. The LVTSCR is triggered by MOSFET snapback voltage; the MOSFET drain region (e.g., also the *n*-well region) undergoes MOSFET snapback when the voltage on the drain/well structure rises [54]. The MOSFET snapback voltages in L_{DD} MOSFET structures can range from 5 to 10 V levels, depending on the MOSFET source/drain design. An advantage of the LVTSCR is that trigger scales with the MOSFET technology; additionally the LVTSCR can be modified by changing the MOSFET channel length.

As technologies are scaled, the desire to have a low voltage turn-on clamp that scales with the power supply voltage is desirable. C. Diaz demonstrated the use of a RC-trigger network to initiate the LVTSCR gate electrode. This initiates the turn-on voltage at a lower trigger condition [56]. Additional techniques have been developed to lower the trigger condition of the SCR structure. G. Croft [57,58], B. Keppens [59], and P. Y. Tan [60] produced examples of new SCR structures and new ESD design techniques. B. Keppens [59], and P. Y. Tan, and I. Manna [60] demonstrated techniques to initiate the SCR for ESD protection by electrical connections to the center nodes of the SCR which are involved in the SCR switching. Figure 9.30 is an example of a SCR which utilizes CMOS electrical circuits to initiate the switching transition of the SCR network [60]. As technologies scale, the ability to use SCR structures on the power supply, or input protection will be pursued because of the high current discharge efficiency, low capacitance, and high switching characteristics of the SCR structure.

9.6 SUMMARY AND CLOSING COMMENTS

In Chapter 9, ESD power clamps for digital, analog, and RF applications were shown. The chapter included a wide range of ESD power clamps which are suitable for advanced CMOS, bipolar, and BiCMOS technologies. The structures shown are examples used in CMOS, Silicon Germanium, and Gallium Arsenide applications.

PROBLEMS

9.1. Given an RC-triggered MOSFET ESD power clamp, derive the resistance value for when the resistor is a MOSFET of length L and width W whose gate is connected to the V_{DD} power supply.

9.2. Given an RC-triggered MOSFET ESD power clamp, given there are three successive stages, show the inverter transfer characteristics for each inverter stage, assuming each inverter stage width increases as $W' = \alpha W$.

9.3. Assuming a output clamp size of W_{Clamp}, given a gate capacitance per unit width, derive the size of the inverter stages to drive the output clamp capacitive load. Solve for the parameter α.

9.4. In an RC-triggered MOSFET ESD power clamp, a resistor is placed between the output of the first inverter stage and the output of the third inverter stage. Derive the feedback relationship from this resistor element in the network response.

9.5. In an RC-triggered MOSFET ESD power clamp, an *n*-channel MOSFET whose gate is connected to V_{DD} is placed in series with the first inverter stage between the V_{DD} and the inverter. Show the transfer characteristics of the inverter. What is the circuit response?

9.6. In an RC-triggered MOSFET ESD power clamp, adding *p*-channel MOSFET keeper networks can improve the circuit stability. Draw a new circuit schematic where MOSFET keeper feedback elements are placed to improve the MOSFET ESD power clamp stability.

9.7. In an RC-triggered MOSFET ESD power clamp, the output clamp body can utilize dynamic threshold MOSFET (e.g., DTMOS) techniques to lower the leakage on the output. Show how the I_{on}/I_{off} ratio of the power clamp can be improved.

9.8. Latchup can occur between a *p*-channel MOSFET power clamp output transistor and the *n*-type resistor element or *n*-type MOS capacitor in the RC trigger network. Which is more likely? Derive the equation for the *pnpn* network formed in the ESD power clamp.

9.9. Guard rings are used in MOSFET inverter circuits to prevent latchup. Does an RC-triggered MOSFET ESD power clamp require guard rings within the inverter stages? Why or why not?

9.10. Given a Zener breakdown triggered ESD bipolar power clamp, it was shown that the following results of the TLP *I–V* characteristic are obtained [43]. Calculate the power at the trigger point. Calculate the power at the holding point.

V_{BR} (V)	V_{on} (V)	V_{t1} (V)	I_{t1} (mA)	V_H (V)	I_H (A)
27	27.5	37.5	750	27	0.4
32	33	41	600	27	0.6
36	37	42	500	27	0.65
45	43	47	400	27	0.8

9.11. Derive the equations for an ESD Darlington-configured power clamp with a forward-bias diode string-trigger network in series with a resistor element. The last trigger diode element is electrically connected to the base of the first Darlington stage, and the emitter of the first stage is electrically connected to the base of the second output Darlington stage. The first and second stages have a diode in series with the collector node. The second-stage Darlington emitter is electrically connected to the lower power rail.

9.12. Derive the equations for an ESD Darlington-configured power clamp with a capacitor-trigger network in series with a resistor element. The capacitor element is electrically connected to the base of the first Darlington stage, and the emitter of the first stage is electrically connected to the base of the second output Darlington stage. The first and second stages have a diode in series with the collector node. The second-stage Darlington emitter is electrically connected to the lower power rail.

9.13. Derive the equations for an ESD Darlington-configured power clamp with a capacitor-trigger network where the capacitor is electrically connected to the base of the first Darlington stage, and the emitter of the first stage is electrically connected to the base of the second output Darlington stage. The first and second stages have a diode in series with the collector node. The second-stage Darlington emitter is electrically connected to the lower power rail. Note that no resistor element is in series with the capacitor trigger element.

9.14. From the capacitor-triggered ESD bipolar Darlington power clamp, in the above problem, draw a set of ESD power clamps separated by an incremental inductor L between each successive power clamp. Represent the network as an LC transmission line.

9.15. From the capacitor-triggered ESD bipolar Darlington power clamp, in the above problem, draw a set of ESD power clamps separated by an incremental inductor L between each successive power clamp. Represent the network as an LGC transmission line, where the diode and Darlington network is represented as a conductance, G. Solve for G.

9.16. Assume a triple-well diode string, with a p^+ diffusion in the p-well, an n^+ diffusion in the p-well and a separate n-band region for each successive stage. Show all parasitic *pnp* and *npn* transistor elements. Derive a relationship, assuming the n-band is serving as a cathode element in the network.

9.17. Assume a triple-well diode string, with a p^+ diffusion in the p-well, an n^+ diffusion in the p-well and a separate n-band region for each successive stage. Show all parasitic *pnp* and *npn* transistor elements. Derive a relationship, assuming the n-band is electrically biased to a separate potential.

9.18. Assume a triple-well diode string, with a p^+ diffusion in the p-well, an n^+ diffusion in the p-well and a the n-band region for each successive stage is electrically connected together. Show all parasitic *pnp* and *npn* transistor elements. Derive a leakage current model for this implementation.

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